82576
REFERENCE DESIGN
(SERDES/FIBER/SFP)

REVISION HISTORY
0.1 ORIGINAL VERSION
1.0 UPDATED BASED ON THE LATEST PRODUCT REQUIREMENTS.
2.0 RELEASED VERSION
2.1 UPDATED NC-SI NOTE

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FUNCTIONAL BLOCK DIAGRAM

ETHERNET
NOT SHOWN IN SERDES VERSION

SFF APPLICATION FOR SERDES
APPLICATION FOR BOTH PORTS.

OPTION A - SERDES
BACKPLANE APPLICATION
FOR BOTH PORTS.

OPTION B - SERDES
SFF APPLICATION FOR
BOTH PORTS.

OPTION C - SERDES
PORT AS
PORT B.

SERDES
FUNCTIONAL BLOCK DIAGRAM
BOTH PORTS.

82576 LAN
CONTROLLER

SMPUS/I2C/NCSI
JTAG

POWER SUPPLY DELIVERY

CUSTOMER IS RESPONSIBLE FOR DELIVERING A +3.3V
SUPPLY THAT IS DERIVED FROM THE PLATFORM MAIN ON
AN SUPPLY RAILS.

THE +1.8V AND +1.0V
SUPPLY'S CAN BE DERIVED
FROM THE +3.3V SUPPLY
UTILIZING EITHER LINEAR OR
SWITCHING REGULATOR
TECHNOLOGIES.

FOR REFERENCE POWER SUPPLY
IMPLEMENTATION OPTIONS
PLEASE REFER TO THE DESIGN
GUIDE.

SPI
EEPROM
SPI
FLASH

+3.3V MAIN

+3.3V AUX

+3.3V LAN
(SFPV_LAN)
FOR SCHEMATIC

+1.8V LAN
(1P8V_LAN)
FOR SCHEMATIC

+1.0V LAN
(1P0V_LAN)
FOR SCHEMATIC

PCI-EXPRESS X4

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ROUTE AS DIFFERENTIAL PAIRS. TRACE LENGTHS SHOULD BE EQUAL WITHIN 0.005 INCHES FOR A PAIR IN EACH SEGMENT.

FOR MORE DETAILED REQUIREMENTS PLEASE REFERENCE THE DESIGN GUIDE.

STUFF IF AUX POWER IS NOT AVAILABLE.

ROUTE AS DIFFERENTIAL PAIRS.
TRACE LENGTHS SHOULD BE EQUAL WITHIN 0.005 INCHES

STUFF IF AUX POWER IS NOT AVAILABLE.

PLATFORM CONNECTIONS REQUIRED.

PC CENTER TO TRANSMITTER.

REQUIRED.

REFERENCES THE DESIGN GUIDE.

82576 PCI EXPRESS RESET CONNECTIONS SHOULD BE GENERATED BY THE PLATFORM.

5 - 82576 PCI EXPRESS, JTAG, AUX POWER, LAN DISABLE, MAIN POWER OK AND DEVICE OFF

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321785-001

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POWER SAVE AT WOL DIS MODE

PLACED C69 CLOSE

OPTIC POWER OPTION - A

NO POWER SAVE

OPTIC POWER OPTION - B

FOR REFERENCE. THIS CONFIGURATION IS VALID FOR BOTH OPTION A AND B.

OPTIONAL PORT 0 OR PORT 1 SHOWN FOR OPTION A.

DNP CAPACITOR IMPLEMENTATION SHOWN

OPTIONAL LINK0 LED

SERDES FIBER OPTIC SOLUTION FOR BOTH WITHIN 1 INCH OF THE BALL SUPPLY FILTER COMPONENTS ORIGIN LOCATION ON THE BGA.

AS A GENERAL RULE PLACING FILTERING FERRITE BEAD AND DECOUPLING CAPACITORS AS CLOSE AS POSSIBLE TO IC IS OPTIMAL.

TO Q1

6 - SERDES FIBER OPTIC OPTION A - SHOWS IMPLEMENTATION FOR BOTH PORT 0 AND 1.
SERDES BACKPLANE CONNECTIONS SHOWN FOR BOTH PORT 0 AND PORT 1 FOR OPTION B.
OPTIONAL CAPACITOR DNP ORIGIN LOCATION ON THE BGA.

DECOUPLING CAPACITORS AS OPTIMAL. CLOSE AS POSSIBLE TO IC IS FILTERING FERRITE BEAD AND SHOULDN'T BE DETERMINED PULL-UP RESISTORS ARE WHEN THESE PINS ARE POPULATED.

8 - SERDES SFP OPTION C - SHOWS IMPLEMENTATION FOR BOTH PORT 0 AND 1.

2.1 02/15/2009 82576 Reference Design (SERDES/FIBER/SFP) Schematics 321785-001