(intel®)

Intel® 82583V Gigabit Ethernet Controller

Single-Port PCI-Express* 10/100/1000 Network Connectivity

- Ideal for consumer electronics and other small form-factor embedded applications

- Low power: < 750 mW GbE and < 300 mW 10/100

- Compact 9mm x 9mm quad flatpack no-lead (QFN) package

- Operating System Support: Linux*, FreeBSD*, Windows* CE, Windows XP Embedded, and Windows Home Server

- Extended life cycle support provides seven-year manufacturing availability for customers

PCI-Express* (PCIe*) x1 Connectivity

The Intel® 82583V Gigabit Ethernet Controller uses a PCIe one lane (x1) interface operating at 2.5 GHz and provides a pathway from legacy PCI*/PCI-X* designs to higher performing PCIe-based designs. The Intel 82583V Gigabit Ethernet Controller provides fully integrated Gigabit Ethernet Media Access Control (MAC) and Physical-Layer (PHY) capabilities. Some optional PCIe extensions are also supported in the controller to enhance platform capabilities for specific usage modes. The controller provides an MDI (copper) standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The Intel 82583V Gigabit Ethernet Controller also enables a quick migration from custom interconnects to Ethernet.

Architected for Small-Footprint Embedded Designs

The Intel 82583V Gigabit Ethernet Controller is a small 9 mm x 9 mm, 64-pin, QFN silicon package that is ideal for GbE implementations on small form-factor embedded designs. The Intel 82583V Gigabit Ethernet Controller consumes less than 750 mW in GbE mode and less than 300 mW in 10/100 mode. The robust design also incorporates optional internal voltage regulation that can reduce the number of voltage supplies required from the platform to power the core and I/O functions. Support of D0 and D3 power states is provided as well as smart power-down at S0 no link and Sx no link. Support of PCIe power management wake-up and advanced power management (APM) wake-up using special packets is provided as well as a LAN disable function. Some performance-enhancing features include IPv4 and IPv6 checksum offload, TCP/UDP checksum offload, extended Tx descriptors for additional off-load capabilities, up to 256 KB TCP segmentation (TSO v2), and header splitting. The Intel 82583V Gigabit Ethernet Controller is completely lead-free and halogen-free in the silicon and package design to reduce the potential for environmental impact.

Features

Benefits

PCI Express* (PCIe*) Features

Features	Benefits
PCIe x1 Interface	• High-bandwidth density per pin • Less-congested board routing compared to PCI* and PCI-X* architectures
PCIe v.1.1 (2.5 GT/s)	• PCI-SIG* conformance and standards interoperability • Supports GbE at wire speed
PCIe advanced extensions	• Extended error reporting and serial number for desired usage modes

Low Power

Features	Benefits
<750 mW S0-Typ (state) 1000Base-T Active 90° C (mode) and <300 mW S0-Typ (state) 100Base-T Active (mode)	• Low power consumption
Smart power-down at S0 no link/Sx no link	• Power management
LAN disable function	• Power management
Full wake-up support: advanced power management (formerly Wake on LAN), Advanced Configuration and Power Interface (ACPI), and Magic Packet* wake-up enable with unique MAC address	• Power management

Features

Benefits

Features	Benefits
ACPI register set and power down functionality supporting D0 and D3 states	• Power management

Gigabit Ethernet Media Access Control (MAC) and Physical-Layer (PHY) Performance Features

Features	Benefits
Integrated PHY for 10/100/1000 Mbps (megabits per second) for multi-speed, full, and half-duplex operation	• Smaller footprint and lower power dissipation compared to multiple discreet MAC and PHY solutions
Descriptor ring management hardware for transmit and receive	• Optimized descriptor fetch and write-back mechanisms for efficient system memory and PCIe bandwidth usage
Legacy and message signal interrupt modes	• Interrupt mapping
64-bit address master support for systems using more than 4 GB of physical memory	• Efficient use of PCIe bus and system memory
Programmable host memory receive buffer per queue (256 bytes to 16 KB) and cache line size (64 bytes to 128 bytes)	• Efficient use of PCIe bus and system memory
Configurable Rx and Tx data FIFO programmable in 1 KB increments	• FIFO size adjustable to the application
Compliant with 1 Gbps (gigabits per second) Ethernet IEEE 802.3, 802.3u, 802.3ab PHY specifications	• Robust operation over installed base of Category-5 twisted-pair cabling
IEEE 802.3x- and 802.3z-compliant flow control support with software-controllable Rx thresholds and Tx pause frames	• Local control of network congestion levels • Reduce receive buffer overflows • Frame loss reduced from receive overruns

Host Offloading Features

Features	Benefits
TCP/UDP, IPv4, and IPv6 checksum offloads; extended Tx descriptors for more offload capabilities	• Improved processor utilization
TCP segmentation/transmit segmentation offloading	• Improved processor utilization
IEEE 802.1q virtual local area network (VLAN) support with VLAN tag insertion, stripping and packet filtering for up to 4096 VLAN tags	• Adding (for transmits) and ping (for receives) of VLAN tags • Filtering packets belonging to certain VLANs
IEEE 802.1q advanced packet filtering	• 16 exact-matched packets (unicast or multicast) • 4096-bit hash filter for multicast frames • Lower processor utilization • Promiscuous (unicast and multicast) transfer mode support • Optional filtering of invalid frames
Header/packet data split in receive	• Helps the driver to focus on the relevant part of the packet without the need to parse it

Additional Device Features

Features	Benefits
IEEE 1588 protocol and 802.1 as implementation (pre-standard)	• Time-stamping enables precision synchronization of time-sensitive applications • Distributes common time to networked media and industrial automation devices
Three output drivers on the single port to drive external LED circuits	• Allows event, state, or activity indication for the port • Configurable for output polarity and blinking indicator
Flash interface support	• Enables system remote boot in legacy BIOS environments via preboot eXecution environment (PXE) • Enables local storage of 64-bit uEFI drivers for network operation in uEFI environment • Flash interface for PXE 2.1 option ROM
MAC/PHY control and status	• Enhanced control capabilities through PHY reset, PHY link status, PHY duplex indication, and MAC Dx power state indication
Watchdog timer	• Defined by the FLASHT register to minimize flash update

Features	Benefits

Characteristics

Electrical	
Typical targeted power dissipation	▪ 750 mW at 1000Base-T active ▪ 300 mW at 100Base-T active

Environmental	
Operating temperature	▪ 0˚ C to 85˚ C
Storage temperature	▪ -40˚ C to 125˚ C
Package	▪ Lead-free and halogen-free

Physical	
Implemented in 90nm lower power, complementary metal-oxide semiconductor process	▪ Minimizes power and size while maintaining quality and reliability
Package	▪ 9 mm x 9 mm silicon package typically provides better thermal characteristics and electrical performance

Network Operating Systems Software Support

Windows* XP Service Pack 2 (SP2)
Windows Vista SP1
Windows Home Server
Windows* CE 6.0 (available post-production)
Windows XP Embedded (available post-production)
Red Hat Enterprise Linux* (RHEL) 4.7
Red Hat Enterprise Linux* (RHEL) 5.2
Linux* Stable Kernel version 2.6
SUSE* Linux Enterprise Server (SLES) 9 SP4
SLES* 10 SP2
DOS-NDIS2
FreeBSD* 7.0
Supports PXE

Order Codes

WG82583V	T&R: MM – 903008 Tray: MM – 903072

To see the full line of Intel® Ethernet Controllers, visit www.intel.com/go/ethernet.

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