PCI Express* 3.0 Technology: PHY Implementation Considerations for Intel Platforms

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Agenda

• Problem Statement
• Existing Usage of K-Code in 8b/10b
• Encoding Scheme
• Transmitter Equalization and training
• Implementation Considerations
• Summary
PCI Express* (PCIe*) Technology Roadmap

- **PCIe Gen1 @ 2.5GT/s**
- **PCIe Gen2 @ 5GT/s**
- **Gen3: 8GT/s Signaling**
- **Atomic Ops, Caching Hints**
- **Lower Latencies, Improved PM**
- **Enhanced Software Model**

Continuous Improvement: Doubling Bandwidth & Improving Capabilities Every 3-4 Years!

<table>
<thead>
<tr>
<th>Year</th>
<th>Raw Bit Rate</th>
<th>Link BW</th>
<th>BW/lane/way</th>
<th>BW x16</th>
</tr>
</thead>
<tbody>
<tr>
<td>1999</td>
<td>2.5GT/s</td>
<td>2Gb/s</td>
<td>~250MB/s</td>
<td>~8GB/s</td>
</tr>
<tr>
<td>2001</td>
<td>5.0GT/s</td>
<td>4Gb/s</td>
<td>~500MB/s</td>
<td>~16GB/s</td>
</tr>
<tr>
<td>2003</td>
<td>8.0GT/s</td>
<td>8Gb/s</td>
<td>~1GB/s</td>
<td>~32GB/s</td>
</tr>
</tbody>
</table>

Based on x16 PCIe channel

Note: Dotted Line is For Projected Numbers
Problem Statement

• PCI Express* (PCle*) 3.0 data rate decision: 8 GT/s
  - High Volume Manufacturing channel for client/ servers
    • Same channels and length for backwards compatibility
    • Low power and ease of design
      - Avoid using complicated receiver equalization, etc.

• Requirement: **Double Bandwidth from Gen 2**
  - PCle 1.0a data rate: 2.5 GT/s
  - PCle 2.0 data rate: 5 GT/s
    • Doubled the data rate/ bandwidth from Gen 1 to Gen 2
  - Data rate gives us a 60% boost in bandwidth
  - Rest will come from **Encoding**
    • Replace 8b/10b encoding with a scrambling-only encoding scheme when operating at PCle 3.0 data rate

• Double B/W: Encoding efficiency 1.25 X data rate 1.6 = 2X

**Challenge:** New Encoding Scheme to cover 256 data plus 12 K-codes with 8 bits
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Review of K-Code Usage

- Each K-codes is a unique 10-bit value
  - Distinct from data and other K-codes

- Two flavors for K-code use
  - Packet Stream (independent of link width)
  - Lane Stream (per-lane)

- Packet Stream relates to Packet Framing (Link-Wide)
  - STP - Start of Transaction Layer Packet (TLP)
  - END - End (Good) of TLP
  - EDB - End Bad of TLP
  - SDP - Start of Data Link Layer packet (DLLP)

- Lane Stream relates to Ordered Sets:
  - Training Set #1 & #2: Training/ retraining
  - SKP Ordered Sets: clock compensation and byte realignment
  - Electrical Idle Start/ Exit sequence: Power Management

- New encoding scheme accommodates these existing usages

Functionality of K-Code needs to be preserved
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Requirements and Capabilities

- **Basic Fault Model:**
  - Guaranteed error detection against random bit flips in any packet or Ordered Set

- **Eventual recovery from bit slip/add**

- **Handle killer packets**
  - Send a different bit stream on retry of a packet

- **Low bandwidth overhead (1-2%)**

- **Low L0s/L1 exit latency overhead**
  - Preserve aggressive power management with performance

- **Changes mostly limited to physical layer**

- **Protocol development concurrent with analysis / simulation done by Intel Pathfinding team**

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*New encoding scheme: Better Performance and Reliability than PCI Express* 2.0 Technology*
LTSSM Speed Change: Example

LTSSM in Device A

L0 (2.5 G)
L0 -> Recovery (directed_speed_change)
Recovery.RcvrLock
Recovery.RcvCfg
Recovery.Speed
Recovery.RcvrLock
L0 (8 G)

8b/10b Encoding

LTSSM in Device B

L0 (2.5 G)

TS1 w/ speed_change = 1
TS1 w/ speed_change = 0
TS1 w/ speed_change = 1
(Gen 2 data rate advertised in TS1/TS2)
TS2 w/ speed_change = 1

Recovery.RcvrLock
Recovery.RcvCfg
Recovery.Speed
Recovery.RcvrLock
L0 (8 G)

Successful Speed Increase initiated by A

Speed Changed to 8GT/s and Encoding switches to 128b/130b

Link goes from Recovery.RcvrLock to L0 in 8 G

Source: Intel Corporation

Both Encoding Schemes Co-exist

Source: Intel Corporation
Two levels of encapsulation

- **Lane Level: Blocks**
  - Data vs Ordered Sets
  - 2-bit Sync Header identifies Data Block vs OS (not scrambled)
  - 128-bit payload
  - Rationale:
    - Redundancy helps separate Data from OS
    - 128-bit payload chosen to match OS payload. 2-bit is low overhead for Sync header is low

- **Data Block: Link wide with Framing preamble identifying packet boundary up-front**
  - Multiple packets within a Data Block and one packet can straddle multiple Blocks
  - Framing preamble same overhead as in 8b/10b
  - Payload scrambled

**Scrambling with two levels of encapsulation**

Source: Intel Corporation
Data Block

- Packets: Logical IDL (LIDL), DLLP, TLP, etc.
- Various sizes from 8b/10b time: 1 Symbol for LIDL, DLLP: 8 Symbols, TLP: Multiple of 4 Symbols
- Everything other than TLP is fixed size
- Need to ensure triple bit flip detection ability while keeping the sizes the same
  - New encoding: One Symbol becomes 8bit rather than 10bit in 8b/10b
- TLP and DLLP body is LCRC protected which provides triple bit flip detection ability
  - Framing preamble itself needs to ensure triple bit flip detection ability as it is used to determine packet boundary
- Challenge: Framing preamble itself has to be of variable length
- Solution: Use first Symbol encoding between different entities to be at a Hamming distance of 4 to ensure triple bit flip detection ability
  - Subsequent Symbols, if any, use some form of CRC protection itself
- Robustness features confirmed by analysis/simulations in Intel path finding
Example of TLP Transmission in a X4

(TLP Transmitted: 3 DW Header (h0 .. h11) + 1 DW Data (d0 .. D3).
1 DW LCRC (L0 .. L3) and Q[11:0]: Sequence No from Link Layer)

[Framer O/P: STP S[3:0] = f h; length l[10:0] = 006h;
Length CRC C[3:0] = f h; Parity P = 0b]
Ordered Sets

- Used for Link training, power management, clock compensation
- Additional usage: Block alignment
  - Can not be scrambled
  - Must reset scrambler (so that both sides start at same point)
  - Can not do this during Data Blocks
    - Unlike 8b/10b where COM can never be aliased to between any two 10-bit Symbols, one can easily alias to any bit pattern when two Data Blocks are looked at consecutively for a fixed pattern
    - Must be done when all permutations are not possible (i.e., during Recovery)
    - Choice of Ordered Set encoding to be such that one can always correctly do block alignment
    - Another challenge is bit slip initially, based on past observation
    - Solution: Continuously do block alignment in Recovery while Ordered Sets are on
- Ordered Set for Clock compensation
  - Can not be scrambled (e.g., repeaters)
  - Need to carry information such as LFSR value to help trace tools
- Link training needs a spectrally rich pattern for better bit lock
  - Solution: Most of TS1/TS2 are scrambled; Rest are not
  - Problem scenarios and their solutions created and verified in analysis / simulation in Intel pathfinding
Sync Header Protection

- Challenge: Sync Header is 2-bits: so even a two bit flip can potentially change a Data Block to an Ordered Set and vice-versa. Even worse the LFSR can be out of sync between the Tx and the Rx and introduce massive errors as a result and cause data corruption.

- Solution: Define a “marker” of the appropriate type whenever there is a transition from Data Block to Ordered Set and vice-versa
  - Pre-notification of the Block type change – that itself is adequately protected
  - Data Block to OS: In last Data Block as a CRC-protected packet
  - OS to Data Block: As an additional 130-bit marker OS
  - Protects more than triple bit flip
  - Problem scenario as well as solution created and validated through analysis/simulation (Intel path finding)
Error Recovery

• Framing error detected by PHY
  – Helps identify cases where the physical layer can either have its scrambler out of sync or fails to ascertain the next packet’s framing preamble location

• Any framing error directs LTSSM to Recovery
  – Stop processing any received TLP/DLLP after Recovery to avoid data corruption
    • The CRC within these packets become ineffective when the packet boundary is lost – random data can always alias to a good CRC
  – Block lock and scrambler reset happens through Recovery prior to packet being accepted
  – Link layer detected errors can be recovered through packet retry

• Error Detection Guarantees maintained
  – Triple bit flip detection within each TLP/DLLP/IDL/OS

Source: Intel Corporation

Robust Error Detection and Recovery Mechanism required with PHY Framer
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Transmitter Equalization

• 2.5 GT/s: Same de-emphasis for all
• 5 GT/s: Introduced platform dependent de-emphasis selection on a per-Link basis
  – -3.5 dB and -6 dB
• 8 GT/s: Our analysis shows that a static selection does not work for all channels due to variations in the receiver design, channel, as well as PVT
• Solution: Need to adjust each transmitter at the by its corresponding receiver in a fine-grain fashion (coefficients)
  – Need to do it once and store it for use on every entry to 8GT/s
  – Must start with some predefined value set by platform characteristics
  – Dynamic adjustment after that
  – Our analysis shows this approach results in working silicon
The eye diagram on the left was the result of using the best pre-set Tx EQ values.
The eye diagram on the right was same channel with optimized Tx EQ coefficients.
The green contour shows the BER eye at $1e^{-12}$.
Eye width opening increased from 7ps to 16ps (over 50% more Eye Width)
  - Both assumed a Tx EQ step size resolution of 1/32
  - Channel: 2 connector topology 18” pin-pin
  - Both used same Rx EQ that was re-optimized for each case.

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Sample Transmitter and Receiver

Link Layer

- Framing Logic
- Lane Reversal/ Degradation
- LFSR & OS Generator
  - Encoder (8b/10b, 128/130)
  - Mux
  - P2S, Driver
- LFSR & OS Generator
  - Encoder (8b/10b, 128/130)
  - Mux
  - P2S, Driver

Other Sources

- Gen 3 Framing Check & Alignment
- Lane Reversal/ Degradation
- LFSR & OS Detector
  - Lane Decoder (8b/10b, 128/130)
- Elastic Buffer
- Rx, DRC, S2P

Direct Recovery

Source: Intel Corporation

Considerations: 1 byte offset to Link Layer for TLPs (EDB). Seq # aligned to LCRC
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Summary & Call to Action

• Overview of Logical PHY based on Intel analysis, simulations, and experience
• 128b/130b Encoding definition
• Equalization mechanism needed
• 25% bandwidth advantage with new encoding over 8b/10b encoding with enhanced reliability
• Track the PCI Express* (PCIe*) 3.0 Spec development in the PCI-SIG and at www.pcisig.com
• Track the PCIe PIPE Spec development at www.intel.com/technology/pciexpress/devnet
  - Plan for products accordingly
Additional Sources of Information on This Topic

• Other Sessions / Chalk Talks / Labs:
  – TCIQ002 Q&A: PCI Express* 3.0 Technology
  – TCIS006 PCI Express* 3.0 Technology: Device Architecture optimizations on Intel Platforms
  – TCIS008 Electrical requirements for designing PCIe* 3.0 ASICs on Intel platforms
  – USBS002 USB 3.0 Architecture and PHY Interface (PIPE) Specification Updates

• Demo/Booths:
  – PCI Express* Technology Community

• Additional Web-based Info:
  – www.pcisig.com
  – www.intel.com/technology/pciexpress/devnet
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