PCI Express* 3.0 Technology: Electrical Requirements For Designing ASICs on Intel Platforms

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TCIS008
Agenda

• Background
• Silicon TX Architecture
  – Jitter
  – PLL Bandwidth
  – TX Equalization
• Silicon RX Test
• Form Factor Considerations
• Intel Enabling
  – Channel Test Tool
  – PCI Express* 3.0 Phy/Mac Interface (PIPE) Specification
  – Electrical Test Tools
• Summary

Disclaimer: Information contained herein is derived from Intel technology path finding and is Work In Progress and is subject to change.
PCI Express* (PCIe*) 3.0 Electrical Requirements

- Compatibility with PCIe* 1.x, 2.0
- Up to 2x performance bandwidth over PCIe 2.0
- Similar cost structure (i.e. no significant cost adders)
- Preserve existing data clocked and common clock architecture support
- Maximum reuse of HVM ingredients
  - FR4, reference clocks, etc.
- Strive for similar channel reach in high-volume topologies
  - Mobile: 8”, 1 connector
  - Desktop: 14”, 1 connector
  - Server: 20”, 2 connectors
Statistical Analysis Methodology

Method relies on LTI characteristics of transmitter, channel and receiver

Impulse response permits superposition of all possible data patterns weighted statistically to capture ISI effects

Statistical Analysis Needed To Gain Margin For High Rate Jitter Specs

Source: Intel Corporation
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**Jitter Definitions**

- **PCI Express* (PCIe)* 2.0**
  - Phase Jitter
    - $T_j$, $D_j$

- **Next generations**
  - Uncorrelated (to data pattern) Phase Jitter
    - $T_j$, $D_j$.
  - Correlated (to data pattern) Phase Jitter
    - $D_j$.
  - Pulse Width Jitter
    - $T_j$
    - $D_j$.
    - F/2 Jitter

Source: Intel Corporation
Jitter Changes from PCI Express* 2.0

- Jitter amplification becomes more significant.

Source: Intel Corporation
Results from Jitter Tolerance Simulation

- CDR can be bounded by simple transfer function.
- CDR is compliant to the jitter tolerance mask
- Use compliant CDR in PLL BW analysis

Source: Intel Corporation
Jitter Tolerance Simulation Setup to Determine CDR Compliance

- **Testboard**
  - RX DUT
    - RX Clock Recovery
    - RX Clock
    - Noise
    - BER target of $1e^{-12}$

- **Test Channel**
  - Low jitter Ref Clk
  - Clk
  - Mod
  - Out
  - Generator

- **Source:** Intel Corporation

- **Parameters:**
  - $R_j = 2.1\text{ps rms (10-1000MHz)}$
  - Sinusoidal Jitter ($S_J$) (defined by jitter tolerance mask)
Determining PLL Characteristics

BER eyes represent the link margin
- Includes worst case RX/TX jitter
- Includes worst case RX voltage uncertainty
- Includes real reference clock with PCIe 2.0 jitter limit
- Includes worst case 20” server channel
- Sweep PLL bandwidth
Any positive eye margin at 1e-12 BER is considered passing

Source: Intel Corporation
Simulation Results

Eye Margin Plot
(PLL peaking = 1dB)

Eye Margin Plot
(PLL peaking = 2dB)

Eye Width (UI)
@ BER=1e-12

~1/3 of the bandwidths
have no positive margin

Source: Intel Corporation

= 2-4MHz PLL BWs

= 5-10MHz PLL BWs
Measured refclk vs. Synthesized refclk

Eye Margin Plot (PLL peaking = 1dB)

Eye Margin Plot (PLL peaking = 1dB)

Eye Width (UI) @ BER=1e-12

Eye Width (UI) @ BER=1e-12

Measured refclk

Synthesized 3ps rms (Gaussian) refclk

Source: Intel Corporation

Optimal PLL Bandwidth Depends On Reference Clock Assumptions
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Tx EQ coefficient optimization vs. Pre-set example

- The eye diagram on the left was the result of using the best pre-set Tx EQ values.
- The eye diagram on the right was the same channel with optimized Tx EQ coefficients.
- The green contour shows the BER eye at 1e-12.
- Eye width opening increased from 7ps to 16ps (over 50% more Eye Width)
  - Both assumed a Tx EQ step size resolution of 1/32
  - Channel: 2 connector topology 18" pin-pin
  - Both used the same Rx EQ that was re-optimized for each case.

Source: Intel Corporation
Rx Stressed Eye and Jitter Tolerance test

• The Rx test can be split into two tests
  – Stressed Eye Test
  – Jitter tolerance test.

• Stressed eye test:
  – Test the Rx under similar EH/EW conditions to a real system.
  – Test can be done with different channel losses to stress the Rx EQ training.

• Jitter tolerance test
  – Test the CDR bandwidth of the Rx
  – Swept Sj.

Separate Tests To Simplify Testing
RX Stressed Eye Derivation

Worst case TX parameters
- Jitter
- Package
- TX EQ

Reference RX structure and Reference Equalization

Worst case channel across all targeted form factors.

Pass/Fail Stressed Eye Mask For Receiver Test
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PCI Express* (PCIE*) 3.0 Form Factor Goals

- Backwards compatibility
- No required changes to the connectors, card form factors, or material.
- Minimal or no changes to the measurement methodologies from those used in the PCIE* 1.x/2.0 specifications.
  - Use eye diagrams (jitter/voltage margin requirements). Minimize additional new requirements.
Form Factor Simulation Method Under Investigation - Step 1: End to End (E2E) Simulations

- Perform E2E simulations
  - Use target 1 connector and 2 connector solutions
  - Eye height (EH) and eye width (EW) examined after first order CTLE at die pad
  - Statistical tools used for all simulations
- Fix MB parameters and determine pass/fail conditions across expected add-in card solution space
- Repeat with many motherboard parameters

Create a statistically significant number of MB descriptions. (Vary channel lengths, Tx params, etc.)
Form Factor Simulations - Worst Case Eye Height

- Worst case Add-in card (AIC) parameters for given MB
- Repeat simulation with different MBs and find worst case for each
- THE ONLY POINT OF INTEREST FOR EACH SET OF MB PARAMETERS IS THE AIC PARAMETERS THAT GIVES WORST CASE

E2E eye height of DOE 48 cases

Source: Intel Corporation
Form Factor Simulation Method Under Investigation - Step 2: Test Fixture Simulations

- Choose a test fixture
  - 2.0 CLB Test Fixture Used For Initial Investigation
  - No receiver equalization applied (eye is open)
- Repeat previous MB simulations with test fixture
  - Determine an eye mask at compliance Test Point
  - Find correlation between EH (and EW) at Test Point vs. end to end results
- No False Passes and a minimum of False Fails

Text fixture with SMP Connectors to ‘scope (CLB 3.0)

Statistically significant number of MB Descriptions (same as E2E simulations)

Source: Intel Corporation
Preliminary Client Simulation Results (Intel CLB 2.0 Test Fixture)

Source: Intel Corporation

Difficult To Differentiate Marginal Cases With Simple Passive Test Fixture
Package Test Fixture Topology

- 2” Strip line test fixture

Varying parameters \{C_{pad}, C_{pin}, Z_0\} to mimic package behavior in e2e simulation

- WC AIC with the mother board combinations with Rx. to correlate test fixture

- Via on test fixture maybe used to mimic reflection from riser and AIC

Estimated Parameters

- \(C_{pad} \leq \sim 1.0 \text{ pf (max)}\)
- \(C_{pin} \sim 0.5 \text{ pf (max)}\)
- 50 mils \(\leq \text{Len} \leq 1500\) mils
- 75\(\Omega\) \(\leq Z_0 \leq 95\Omega\)

Source: Intel Corporation
Test Fixtures With RC Package Models

*Same methodology with 50 cases around pass/fail for 2 connector server also gives very close pass/fail numbers

Source: Intel Corporation

Test Fixture with Package Structure Helps Differentiate Marginal Cases
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## Channel Test Tool

### Technology and Test Type
- PCI Express* 3.0, USB* 3.0, etc.

### Step responses for test channel and two aggressors.

### Resulting eye with worst case jitter, equalization, etc. per relevant specification.

Source: Intel Corporation
Various protocols running over the common PIPE MAC/PHY interface.

PIPE interface differences minimized across protocols.

PCI Express* PIPE 3.0 Rev .7 targets PCI Express 3.0 only. Rev .9 will merge with all previous supported technologies.
PCI Express* PHY Interface (PIPE) 3.0

- Defines standard functions that must be present in PIPE 3.0 compliant PHY
- Defines standard interface between PIPE 3.0 compliant PHY and Media Access/Link Layer between PHY
- Major PCIe* 3.0 challenge is how to handle 130/128 encoding

Source: Intel Corporation
PCI Express* (PCIE*) PIPE 3.0

- PCIE* 3.0 PIPE extends PCIe 2.0 PIPE
  - Keeps PCIe 2.0 interface and clocking/width options
  - Adds 32 bit width and clocking options
  - Adds a new control signal for Mac to tell PHY to ignore 8 bits.
    - MAC uses control signal to handle 128/130 domain rate difference.
  - Adds TX/RX EQ signals to handle 3.0 3 tap equalization.

- 0.7 Draft available at:
  www.intel.com/technology/pciexpress/devnet
Summary

- Intel will enable the industry on PCI Express* (PCIe*) 3.0
  - PIPE Specification
  - Sigtest
  - Clock Analysis Tool
  - Channel Test Tool
  - Low Cost Receiver Test Device
Additional Sources of Information on This Topic

- Other PCI Express* Technology Sessions – TCIS006, TCIS007
- Visit the PCI Express* Technology Community on the showcase floor
- More Web-based info: www.pciexpressdevnet.org
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