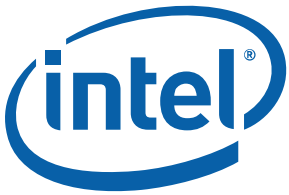

Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1

Design Guidelines

September 2009

Reference Number: 321736 Revision: 002

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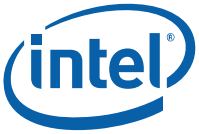

Figures

Tables

Revision History

Doc #	Rev #	Description	Rev. Date
321736	001	Initial public posting	March 2009
321736	002	Added Chapter 2.1.1: Max Load Step as function of Load Step Rep rate.	September 2009

§

1 Applications

1.1 Introduction and Terminology

This document defines the DC-to-DC converters to meet the processor power requirements of the following platforms:

Table 1-1. VRM/EVRD 11.1 Supported Platforms and Processors

Intel® Xeon® 5500 Platforms		
Intel® Xeon® Processor 5500 Series Performance WS Processor 130W	Intel Xeon Processor 5500 Series Performance Proc 95W	Intel Xeon Processor 5500 Series Volume Performance Processor 80W
Intel Xeon Processor 5500 Series Ultra Dense Processor 60W	Intel Xeon Processor 5500 Series Processor 38W	

Some requirements will vary according to the needs of different computer systems and processors. The intent of this document is to define the electrical, thermal and mechanical design specifications for VRM/EVRD 11.1.

VRM – The voltage regulator module (VRM) designation in this document refers to a voltage regulator that is plugged into a baseboard via a connector or soldered in with signal and power leads, where the baseboard is designed to support more than one processor. VRM output requirements in this document are intended to match the needs of a set of microprocessors.

EVRD – The enterprise voltage regulator down (EVRD) designation in this document refers to a voltage regulator that is permanently embedded on a baseboard. The EVRD output requirements in this document are intended to match the needs of a set of microprocessors. EVRD designs are only required to meet the specifications of a specific baseboard and thus must meet the specifications of all the processors supported by that baseboard.

'1' – In this document, refers to a high voltage level (V_{OH} and V_{IH}).

'0' – In this document, refers to a low voltage level (V_{OL} and V_{IL}).

'X' – In this document, refers to a high or low voltage level (Don't Care).

'#' – Symbol after a signal name in this document, refers to an active low signal, indicating that a signal is in the asserted state when driven to a logic low level.

The specification in the respective processors' Electrical, Mechanical, and Thermal Specifications (EMTS) documents always take precedence over the data provided in this document.

VRM/EVRD 11.1 incorporates functional changes from prior VRM/EVRD 11.0 design guidelines:

- Enhanced power-on sequence
- Support only for VR 11.0 VID 8-bit table and 6.25 mV resolution with a 0.5 V to 1.6 V VID range
- Fixed Load Line at 0.8 mΩ
- Several new I/O signals – introduced

- LL_ID, VR_ID# and VID_Select – signals eliminated
- Faster dVID spec.

Table 1-2. Guideline Categories

Guideline Categories	
REQUIRED:	An essential feature of the design that must be supported to ensure correct processor and VRM/EVRD functionality.
EXPECTED: (Recommended)	A feature to ensure correct VRM/EVRD and processor functionality that can be supported using an alternate solution. The feature is necessary for consistency among system and power designs and is traditionally modified only for custom configurations. The feature may be modified or expanded by system OEMs, if the intended functionality is fully supported.
PROPOSED: (Optional)	A feature that adds optional functionality to the VRM/EVRD and therefore is included as a design target. May be specified or expanded by a system OEMs.

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2 Output Voltage Requirements

2.1 Voltage and Current – REQUIRED

There will be independently selectable voltage identification (VID) codes for this VR. The VID code is provided by the processor to the VRM/EVRDs, which will determine a reference output voltage, as described in Section 5.3. The VR 11.1 controller will support one 8-bit VR11.0 linear table ranging from 0.03125 V to 1.6 V (usable range 0.5 V-1.6V). Therefore, each applicable processor will use all 8-bit VIDs.

The load line tolerance in Section 2.2 shows the relationship between Vcc and Icc at the die of the processor.

The VRM/EVRD 11.1 may be required to support a load up to the extent of the following (generic) limits:

- A maximum continuous load current (I_{CCTDC}) of **130 A**.
- A maximum load current (I_{CCMAX}) of **150 A** peak.
- A maximum load current step (ICCSTEP) of **120 A** (the exact number may be larger, it will be verified after power-on)
- A maximum current slew rate (dICC/dt) of **300 A/µs** at the lands of the processor.

Note: **Each VR11.1 compatible processor may and often does impose lower load limits, see Table 2-1 for the actual requirements, which are a subset of the above generic requirements.**

The continuous load current (**I_{CCTDC}**) can also be referred to as the Thermal Design Current (TDC). It is the sustained DC equivalent current that the processor is capable of drawing indefinitely and defines the current that is used for the voltage regulator temperature assessment. At TDC, switching FETs may reach maximum allowed temperatures and may heat the baseboard layers and neighboring components. The envelope of the system operating conditions, establishes actual component and baseboard temperatures. This includes voltage regulator layout, processor fan selection, ambient temperature, chassis configuration, and so on. To avoid heat related failures, baseboards should be validated for thermal compliance under the envelope of the system's operating conditions. It is proposed that voltage regulator thermal protection be implemented for all designs (Section 6.2).

The maximum load current (**I_{CCMAX}**) represents the maximum peak current that the processor is capable of drawing. It is the maximum current the VRM/EVRD must be electrically designed to support without tripping any protection circuitry.

The maximum step load current (**IccStep)** is the maximum dynamic step load that the processor is expected to impose on its Vcc power rail within the Iccmin and Iccmax range, where the Iccmin is the processor's minimum load, constituted by its leakage current.

The amount of time required by the VR to supply current to the processor is dependent on the processor's operational activity. As previously mentioned, the processor is capable of drawing I_{CCTDC} indefinitely; therefore, the VR must be able to supply (I_{CCTDC}) indefinitely. Refer to Figure 2-1 for the time durations required by the VR to supply current for various processor loads.

It is expected that the maximum load current (**ICCMAX**) can be drawn for periods up to 10 ms. Further, it is expected that the load current averaged over a period of 100 seconds or greater, will be equal to or less than the thermal design current (ICCTDC).

Figure 2-1. VRM/EVRD 11.1 Load Current versus Time

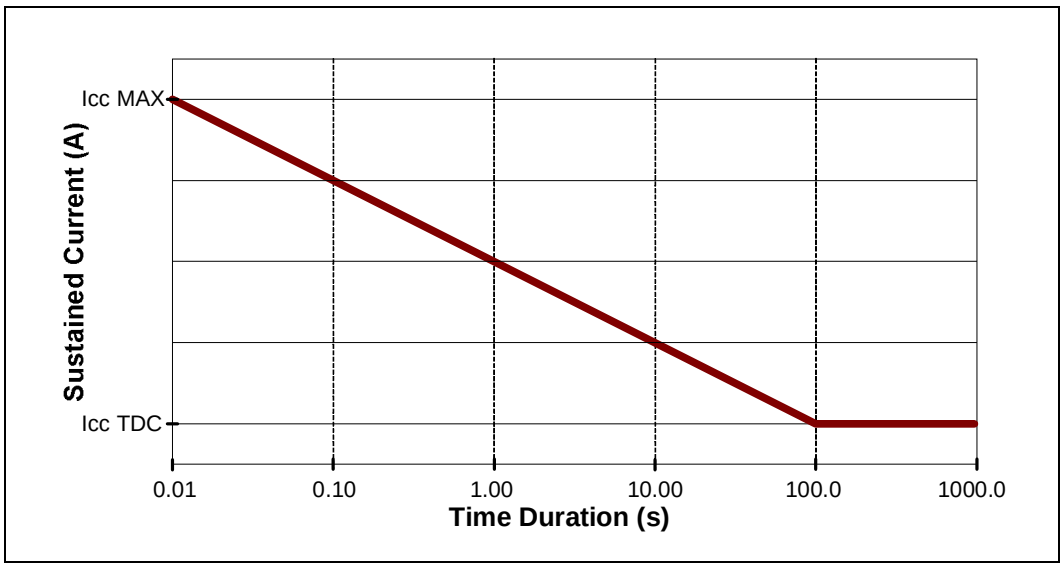


Table 2-1 shows the Icc guidelines for any flexible motherboard (FMB) frequencies supported by the VRM/EVRD 11.1 in Table 1-1. For designers who choose to design their VR thermal solution to the ICCTDC current, it is recommended that voltage regulator thermal protection circuitry be implemented (see Section 6.2).

Table 2-1. Icc Guidelines

Processor (Vcore)	ICCTDC (Atdc)	ICCMAX (Apk)	ICC STEP Max (App)	Notes
Intel Xeon Processor 5500 Series	**110**	**150**	**97**	
Intel Xeon Processor 5500 Series 95W SKU	**85**	**120**	**81**	
Intel Xeon Processor 5500 Series	**70**	**100**	**72**	1 – 4
Intel Xeon Processor 5500 Series	**60**	**80**	**59**	
Intel Xeon Processor 5500 Series	**25**	**40**	**26**	

Notes:
1. The values shown are either pre-silicon estimates or the latest known values and are subject to update. See the respective Processor's Electrical, Mechanical, and Thermal Specifications (EMTS) for the latest IccTDC and IccMAX specifications.
2. FMB = Planned Flexible Mother Board guideline for processor end-of-life.
3. Voltage regulator thermal protection circuitry should not trip for load currents greater than ICCTDC.
4. For platforms designed to support several processors, the highest current value should be used.

2.1.1 Max Load Step Size as function of Load Step Repetition Rate

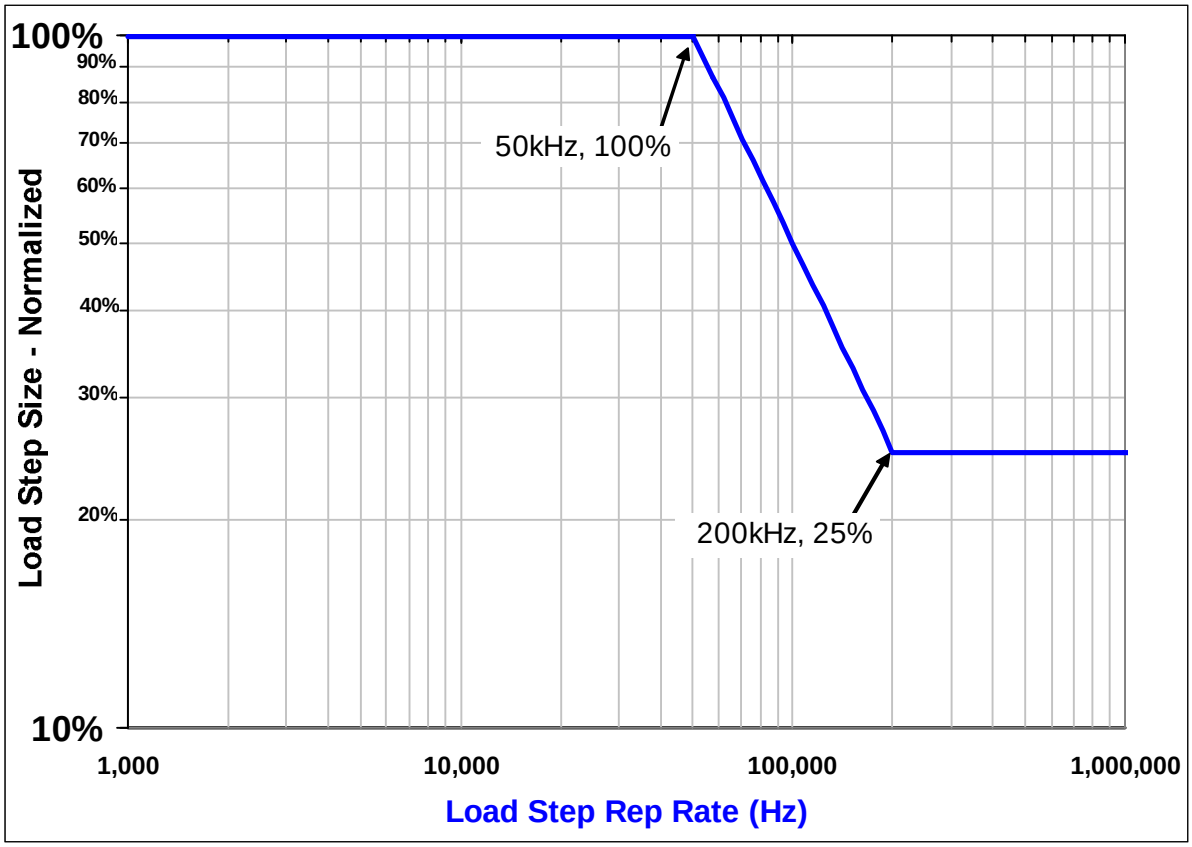
Based on live platform measurements, while running a majority of publicly available power stress SW applications, the following maximum step load size vs. step load rep rate relationship was developed for the VR11.1 bench validation.

Table 2-2. Vcc Load Step Size vs. Rep Rate

Rep Rate (RR)	Step Size	Notes
≤ 50 kHz	100%	VR test Min Rep Rate ~ 300Hz
50 kHz < RR < 200 kHz	(50kHz/RR)*100%	RR in kHz
≥ 200 kHz	25%	VR test Max Rep Rate ~ 1MHz

The 100% Load Step Size corresponds to the IccStep Max in Table 2-1.

Figure 2-2. Vcc Load step size vs load step rep rate graph



Note: Based on the available platform measurement data, this updated Max Step Load size vs. Load Step Rep Rate relationship applies to VR11.1 for CPU Vcore applications only, unless stated otherwise in the related Platform Design Guide (PDG).

2.2 Load Line Definitions – REQUIRED

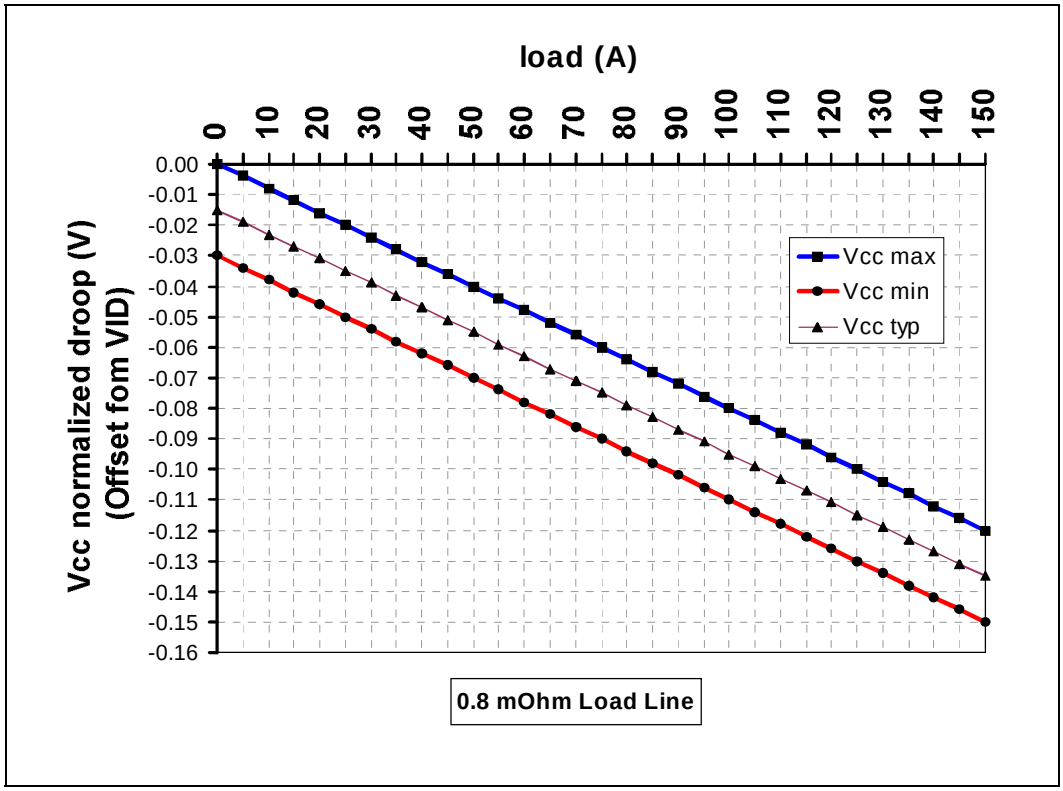
To ensure processor reliability and performance, platform DC and AC transient voltage regulation must be contained within the V_{CCMIN} and the V_{CCMAX} die load line boundaries, except for short burst transients above the V_{CCMAX} as specified in Section 2.4. Die load line compliance must be guaranteed across 3-sigma component manufacturing tolerances, thermal variation and age degradation. The following load line contains static and transient voltage regulation data as well as maximum and minimum voltage levels. It is required that the regulator's positive and negative differential remote sense pins be connected to both the V_{CC_SENSE}, V_{SS_SENSE}, pin pair of the processor socket, see Figure 5-1. The prefix V_{CC} is designated for the positive remote sense signal and the V_{SS} prefix for the negative remote sense signal.

The upper and lower load lines represent the allowable range of voltages that must be presented to the processor. The voltage must always stay within these boundaries for proper operation of the processor. Operating above the V_{CCMAX} load line limit will result in higher processor operating temperature, which may result in damage or a reduced processor lifespan. Processor temperature rise from higher functional voltages may lead to dynamic operation to low power states, which directly reduces processor performance. Operating below the V_{CCMIN} load line limit will result in minimum voltage violations, which will result in reduced processor performance, system lock up, "blue screens" or data corruption.

For load line validation information, please refer to the *LGA1366 Voltage Test Tool User's Guide*.

Figure 2-3 and Figure 2-4 shows the load line voltage offsets and current levels based on the VID specifications for this VR regulator.

Figure 2-3. Normalized 0.8 mOhm / 150 A Load Line with +0/-30 mVdc Tolerance Band – Example



Notes:
1. See Section 2.3 for the output voltage tolerance.
2. When the processors are not present, the OUTEN will not assert, as shown in Figure 2-6.

The Min / Max Load Line equations are:

VccMax = VID (V) – 0.8 mΩ * Icc (A)

VccTyp = VID (V) – 0.8 mΩ * Icc (A) – 15 mV

VccMin = VID (V) – 0.8 mΩ * Icc (A) – 30 mV

2.3 Output Voltage Tolerance – REQUIRED

The voltage ranges shown in Section 2.2 include the following tolerances:

- Total DC set point error (DAC set point +Error Amp +Rem Sense buffer amp, if applicable), typical **10 mVp-p** output ripple and noise, over full ambient temp range and warm up, component aging effect, no-load offset centering error, lot to lot variation.
- Initial DC output voltage set-point error.

- Dynamic output changes from minimum-to-maximum and maximum-to-minimum load should be measured at the point of regulation. When measuring the response of the die voltage to dynamic loads, use the VCC_DIE_SENSE and VSS_DIE_SENSE pins on the processor socket with an oscilloscope set to a DC to 20-100 MHz bandwidth limit (whichever is available) and with probes that are 1.5 pF maximum and 1 MΩ minimum impedance.
- Variations of the input voltage.

Regardless of the DAC tolerance, the Load Line tolerance budget cannot be violated at any VID setting and the DAC output must be monotonic.

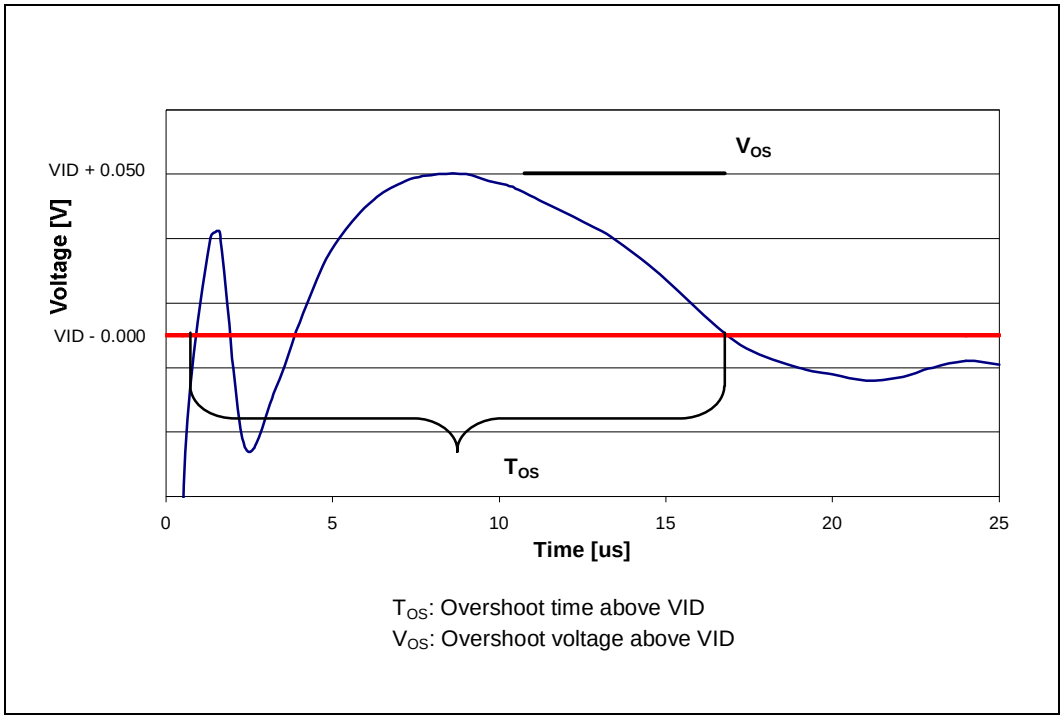
See the *VR11.1 PWM Specification*, *Revision 1.0* for the PWM IC requirements.

2.4 Processor VCC Max Allowed Overshoot – REQUIRED

The VRM/EVRD 11.1 is permitted short transient overshoot events where Vcc exceeds the VID voltage when transitioning from a high-to-low current load condition (Figure 2-4). This overshoot cannot exceed VID + VOS_MAX. The overshoot duration, which is the time that the overshoot can remain above VID, cannot exceed TOS_MAX. These specifications apply to the processor die voltage as measured across the remote sense points and should be taken with the oscilloscope bandwidth setting limited to 20 MHz or 100 MHz, depending what is supported by your particular scope (with 20 MHz preference).

- VOS_MAX = Maximum overshoot voltage above VID = 50 mV
- TOS_MAX = Maximum overshoot time duration above VID = 25 µs

Figure 2-4. Processor Vcc Overshoot Example Waveform



2.5 Impedance versus Frequency – EXPECTED

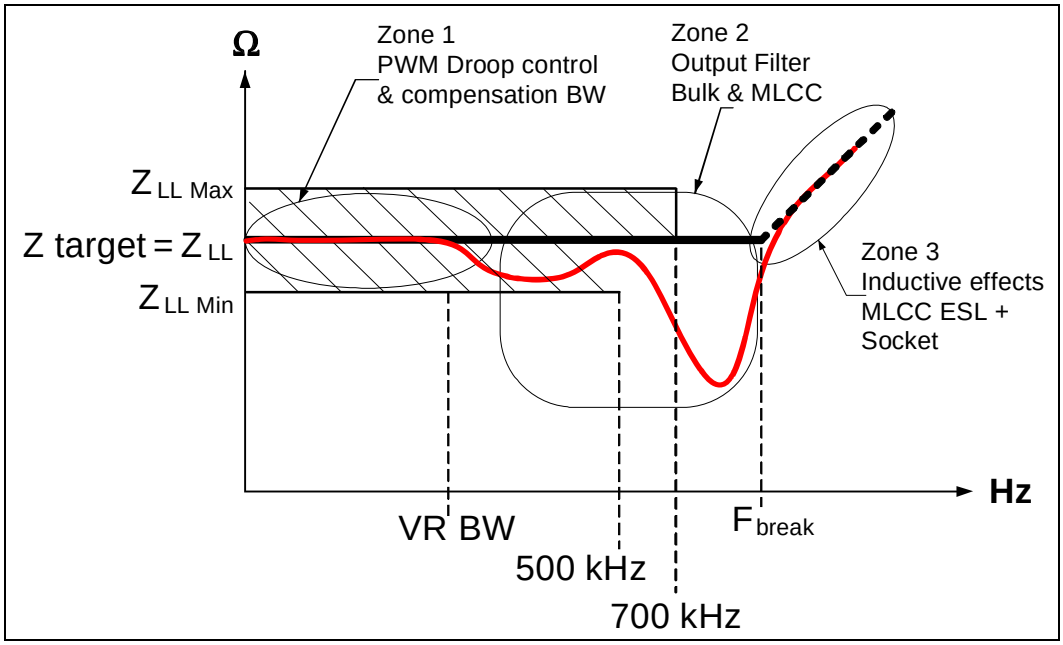
Vcc power delivery designs can be susceptible to resonance phenomena capable of creating droop amplitudes that violate the load line specification. This is due to the frequency varied PCB, output decoupling and socket impedances from the power plane layout structures. Furthermore, these resonances may not be detected through standard time domain validation and require engineering analysis to identify and resolve.

Impedance versus Frequency, Z(f) performance simulations of the power delivery network is a strongly recommended method to identify and resolve these impedances, in addition to meeting the time domain load line in Section 2.2 and Section 2.3. The decoupling selection needs to be analyzed to ensure that the impedance of the decoupling is below the load line target up to the FBREAK (2 MHz) frequency as defined in Figure 2-5. Frequency domain load line and overshoot compliance is expected across the 0 Hz to FBREAK bandwidth. The power delivery frequency response is largely dependent upon the selection of the bulk capacitors, ceramic capacitors, power plane routing and the tuning of the PWM controller's feedback network. This analysis can be done with LGA1366_VRTT tool impedance testing or through power delivery simulation if the designer can extract the parasitic resistance and inductance of the power planes on the motherboard along with good models for the decoupling capacitors.

Measured power delivery impedance should be within the tolerance band shown in Figure 2-5. The tolerance band is defined for the VRTT impedance measurement only. For load line compliance, time domain validation is required and the VR tolerance band must be met at all times. Above 500 kHz, the minimum impedance tolerance is not defined and is determined by the MLCC capacitors required to get the ESL low enough to meet the load line impedance target of the FBREAK frequency. At 700 kHz, the ZMAX tolerance drops to the load line target impedance. Any resonance point that is above the ZMAX line needs to be carefully evaluated with the time domain method by applying transient loads at that frequency and looking for VMAX or VMIN violations. Maintaining the impedance profile up to FBREAK is important to ensure the package level decoupling properly matches the motherboard impedance. After FBREAK, the impedance measurement is permitted to rise at an inductive slope. The motherboard VR designer does not need to design for frequencies over FBREAK as the Intel Microprocessor package decoupling takes over in the region above FBREAK.

Each of these design elements should be fully evaluated to create a cost optimized solution, capable of satisfying the processor requirements. Experimental procedures for measuring the Z(f) profile will be included in near future in the next revision of the EVRD_VRM11_1_LL_dVID LGA1366_VRTT Tester-UG.pdf test methodology user's guide using the LGA1366 VRTT. Additional background information regarding the theory of operation is provided in Appendix A.

Figure 2-5. Power Distribution Impedance versus Frequency



Notes:
1. Zone 1 is defined by the VR closed loop compensation bandwidth (VR BW) of the voltage regulator. Typically 30-40 kHz for a 300 kHz voltage regulator design
2. Zones 2 & 3 are defined by the output filter capacitors and interconnect parasitic resistance and inductance. The tolerance is relaxed over 500 kHz allowing the VR designer freedom to select output filter capacitors. The goal is to keep Z(f) below Z_{LL} up to F_{BREAK} (2 MHz) and as flat as practical, by selection of bulk cap values, type and quantity of MLCC capacitors. The ideal impedance would be between Z_{LL} and Z_{LLMin}, but this may not be achieved with standard decoupling capacitors.
3. See Section 2.5 and Table 2-3, Impedance Measurement parameters and definitions

Table 2-3. Impedance Measurement Parameters

Processor, Vcore VR	Z_{LL}[1]	Z_{LLMAX}[2]	Z_{LLMIN}[3]	Fbreak	Notes
Intel Xeon Processor 5500 Series	0.8 mΩ	1.0 mΩ	0.6 mΩ	2.0 MHz	1,2,3
Intel Xeon Processor 5500 Series	0.8 mΩ	1.05 mΩ	0.55 mΩ		
Intel Xeon Processor 5500 Series	0.8 mΩ	1.1 mΩ	0.5 mΩ		
Intel Xeon Processor 5500 Series	0.8 mΩ	1.175 mΩ	0.425 mΩ		
Intel Xeon Processor 5500 Series	0.8 mΩ	1.55 mΩ	0.05 mΩ		

Notes:
1. Z_{LL} is the target Z(f) impedance for each processor and it's value coincides with it's Load Line slope.
2. Z_{LLMAX} is the maximum allowed Z_{LL} tolerance, which still fits within the VccMax and VccMin Load Line limits listed in Table 2-1; Z_{LLMAX} is specific for each processor due to a specific combination of its Load Line value and IccMax.
3. Z_{LLMIN} is the minimum allowed Z_{LL} tolerance, which still fits within the VccMax and VccMin Load Line limits listed in Table 2-4; Z_{LLMIN} is specific for each processor due to a specific combination of its Load Line value and IccMax.

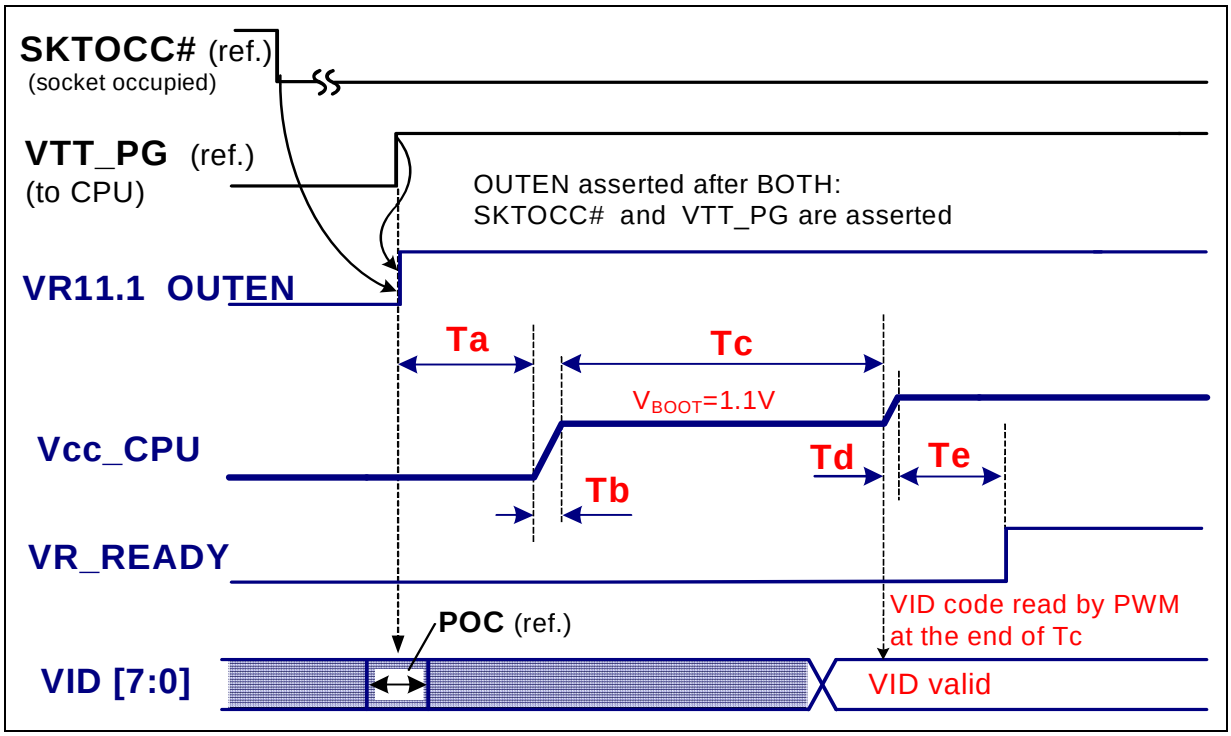
2.6 Stability – REQUIRED

The VRM/EVRD needs to be unconditionally stable under all specified output voltage ranges, current transients of any duty cycle, and repetition rates of up to 2 MHz. The VRM/EVRD should also be stable under a no load condition.

2.7 Processor Power Sequencing – REQUIRED

The VRM/EVRD 11.1 must support platforms with defined power-up sequences. Figure 2-6 shows a timing diagram of the power-on sequencing requirements. Timing parameters for the power-on sequence are listed in Table 2-4.

Figure 2-6. Power-On Timing Sequence Diagram, Intel Xeon Processor 5500 Series Example



Notes:
1. Tb and Td voltage slopes are determined by soft start logic of the PWM controller.
2. Vboot is a default power-on Vcc (Core) value. Upon detection of a valid Vtt supply, the PWM controller is to regulate to this value until the VID codes are read. The Vboot voltage is 1.1 V.
3. Vtt is the processor termination regulator's output voltage and the VTT_PG is the VTT regulator's power good status indicator.
4. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
5. This specification requires that the VID signals be sampled no earlier than 10 µs after VCC (at VCC_BOOT voltage) and VTT are stable.
6. Parameter must be measured after applicable voltage level is stable. "Stable" means that the power supply is in regulation as defined by the minimum and maximum DC/AC voltage regulation specifications for all components being powered by it.
7. The maximum PWRGOOD rise time specification denotes the slowest allowable rise time for the processor, measured between (0.1 * VTT) and (0.9 * VTT).

Table 2-4. Power-On Sequence Timing Parameters

Timing	Min	Default	Max	Remarks
Ta = OUTEN to Vcc_CPU rising – delay time	0		5.0 ms	
Tb = Vboot rise time	0.05 ms[1]	0.5 ms	10.0 ms	Programmable soft start ramp; Measured from 10-90% of slope
Tc = Vboot to VID Valid delay time	0.05 ms[1]		3.0 ms	Vboot duration
Td = Vcc_CPU rise time to final VID	0	0.25 ms	3.5 ms	Programmable soft start ramp; Measured from 10-90% of slope
Te = VccCPU to VR_READY assertion – delay time	0.05 ms		3.0 ms	

Note: 1. Minimum delays must be selected in a manner which will guarantee compliance to voltage tolerance specifications.

2.7.1 Power-Off Timing Sequence – REQUIRED

There can be a normal or an abnormal power-off, the typical cases are:

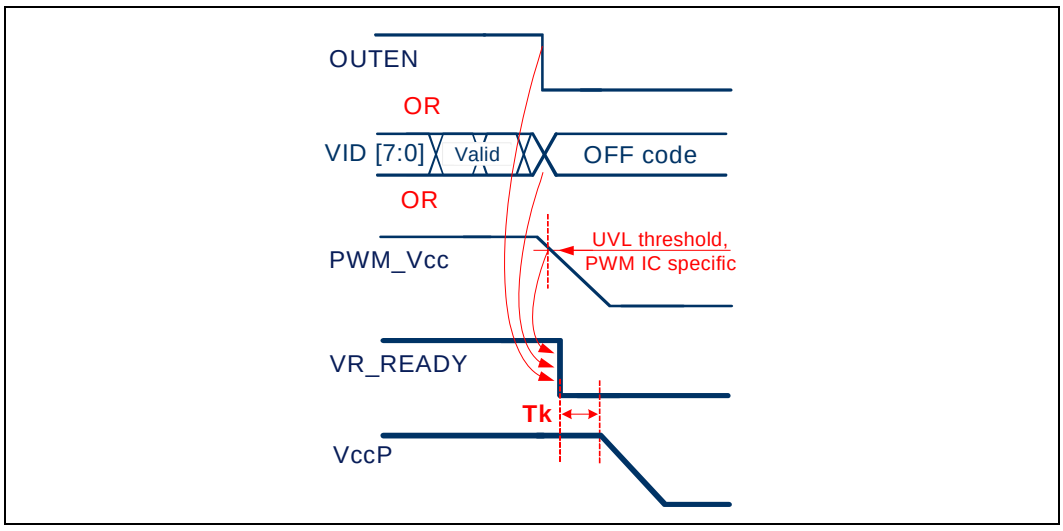
1. **Normal power-off** by de-asserting OUTEN (non-latching)

2. **Abnormal power-off** due to:

- PWM _Vcc falling out of regulation, below its UVLo threshold (latching, able to unlatch by Vcc off/on toggle)
- VID Off-code sent by CPU, implies CPU failure (normally non-latching, re-boots when Vcc>UVLO and OUTEN asserted)
- OVP condition (see also Section 4.1)
- OCP condition (see also Section 4.2)

In each of those power-off cases the VR_Ready should de-assert immediately (with no additional build-in delay, propagation delay only) and following it, after Tk delay, VccP should fall and latch off, where **Tk = 0-500 ms**, as depicted below.

Figure 2-7. Power-Off Timing Diagram



For detailed information about VID Off-Codes see Section 5.3.

2.8 Dynamic Voltage Identification (dVID) – REQUIRED

VRM/EVRD 11.1 supports dynamic VID across the entire usable VID table (0.5 V-1.6 V). The VR must be capable of accepting voltage levels transitioning from a standard operational VID levels to the minimum VID=0.5 V by stepping down or up sequentially through the table, as follows:

- **6.25 mV** VID steps every **1.25 µs**
- **12.5 mV** VID steps every **2.5 µs**
- Vout slew rate response to a single (>25 mV) dVID step upwards / downwards =**10 mV/µs minimum**
- settle within **±5 mV** of final value (nominal Vdroop LL including no load offset from VID) within **15 µs** for dVID event ≥ **50 mV**

- settle within < **5 µs** for dVID event **< 50 mV**
- Skew on each VID line ≤ **200 ns Max**

Note: The proper trace routing of the 8 VID lines from the CPU socket to the VR PWM IC is critical and the meeting of the 200 ns maximum skew spec will depend on it.

Downward dVID jumps should decay with the CPU load current, the VR is not required to pull down the output voltage. The VID inputs should contain circuitry to prevent false tripping of OCP or OVP or latching of VID codes during the settling time.

During a transition, the output voltage must be between the maximum voltage of the high range ("A" in Figure 2-8) and the minimum voltage of the low range ("B"). The VRM/EVRD must respond to a transition from VID-low to VID-high by regulating its Vcc output to the range defined by the new final VID code, within 15 µs of the final step. The time to move the output voltage from VID-high to VID-low will depend on the PWM controller design, the amount of system decoupling capacitance, and the processor load.

Figure 2-8 shows operating states as a representative processor changes levels. The diagram assumes steady state, maximum current during the transition for ease of illustration; actual processor behavior allows for any dIcc/dt event during the transitions, depending on the code it is executing at that time. In the example, the processor begins in a high-load condition. In transitions 1-2 and 2-3, the processor prepares to switch to the low-voltage range with a transition to a low load condition, followed by an increased activity level. Transition 3-4 is a simplification of the multiple steps from the high-voltage load line to the low-voltage load line. Transition 4-5 is an example of a response to a load change during normal operation in the lower range.

Figure 2-8. Processor Transition States

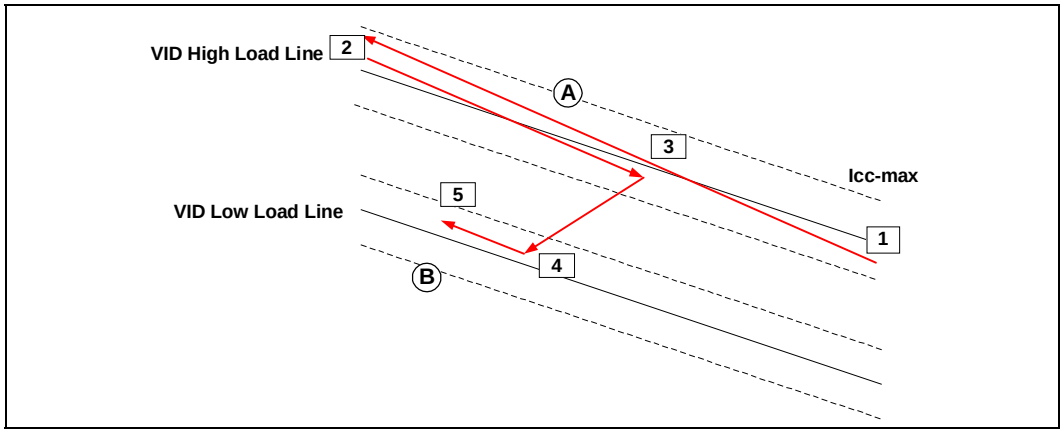
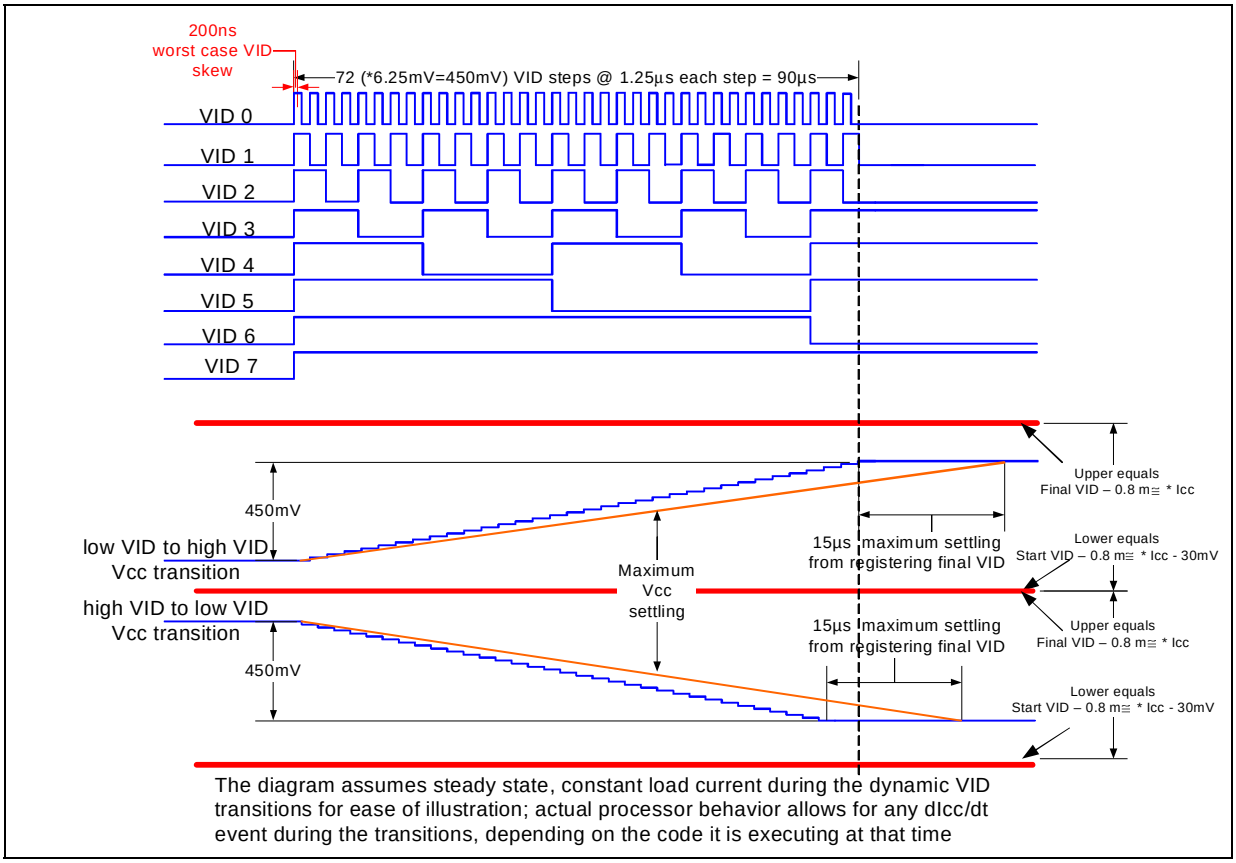


Figure 2-9 is an example of dynamic VID. The diagram assumes steady state, constant current during the dynamic VID transition for ease of illustration, actual processor behavior allows for any dIcc/dt during the transitions, depending on the code it is executing at that time. Note that during dynamic VID, the processor will not output VID codes that would disable the voltage regulator output voltage.

Figure 2-9. Dynamic VID Transition States Illustration – Example



The processor load may not be sufficient to absorb all of the energy from the output capacitors on the baseboard, when VIDs change to a lower output voltage. The VRM/EVRD design should ensure that any energy transfer from the capacitors does not impair the operation of the VR, the AC-DC supply, or any other parts of the system.

2.9 Overshoot at Turn-On or Turn-Off – REQUIRED

The core VRM/EVRD output voltage should remain within the load-line regulation band for the VID setting, while the VRM/EVRD is turning on or turning off, with no over or undershoot out of regulation. No negative voltage below **–100 mV** may be present at the VRM/EVRD output during turn-on or turn-off.

2.10 VR Vcc Under-Voltage Lockout (UVLo) – EXPECTED

The VR should detect its own Vcc input and remain in the disabled state until valid Vcc level is available or reached; However, the PWM and driver chips should coordinate start up such that both the PWM Vcc and power conversion rail (typically +12 V) of the buck converter are both up and valid prior to enabling the PWM function. The PWM and Driver combination need to be tolerant of any sequencing combination of 3.3 V, 5 V or 12 V input rails. If either the Vcc or power conversion rail fall below the UVLo thresholds, the PWM should shut down in an orderly manner and restart the start up sequence.

2.11 Output Filter Capacitance – REQUIRED

The output filter capacitance for the VRM/EVRD 11.1 based designs will be located on the baseboard around the CPU socket and inside the socket's cavity. The system design must ensure that the output voltage of the VR is stable under all load conditions and it conforms to the load line of Figure 2-3 and with the baseboard and processor loads. Refer to the latest revision of your Platform Design Guide for the latest information regarding the Vcc load characteristic such as:

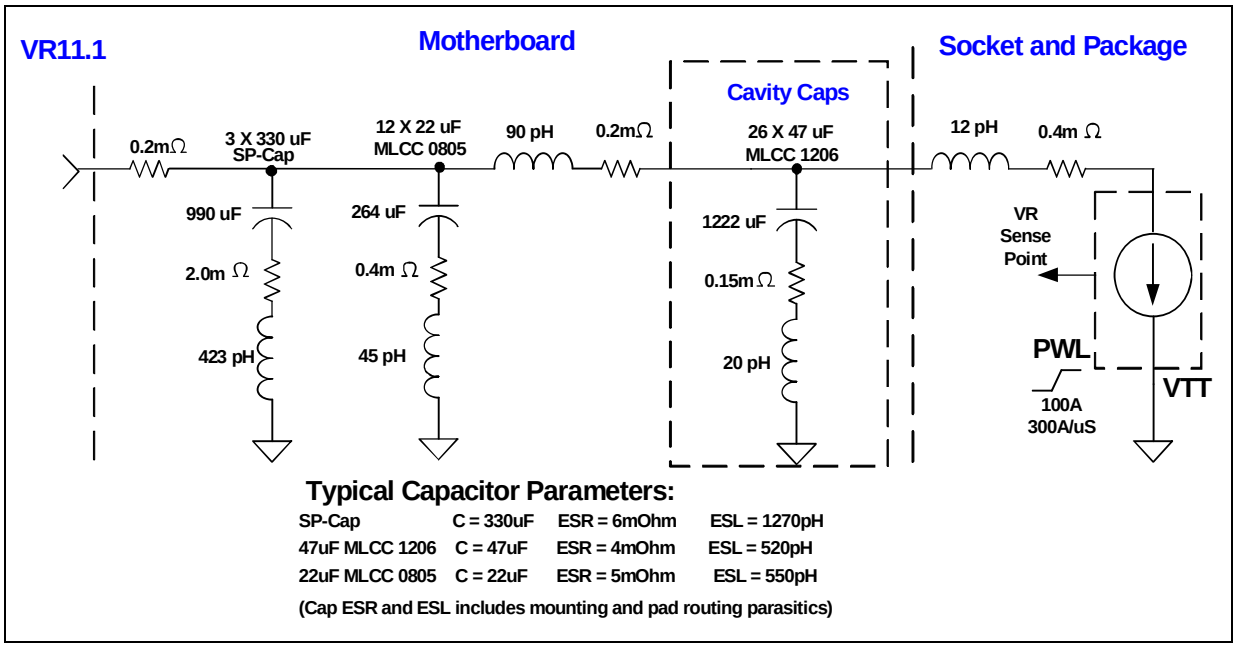
1. VccP Power Delivery lumped impedance model w/ output filter caps description

2. VccP and Ground power layers example layouts.

Table 2-5 shows the number of decoupling caps recommended and other related specifications based on updated processor power requirements supported by VRM/ EVRD 11.1.

Figure 2-10 is the recommended example of Intel Xeon 5500 Platform CRB baseboard decoupling solutions and processor loads. The number of capacitors needed could change based on updated processor power requirements. The type and number of bulk decoupling required is dependent on the voltage regulator design and it is highly recommended that the OEM work with the VR supplier for an optimal decoupling solution for their system and in accordance to the processor's design requirements.

Figure 2-10. 8-Layer Intel Xeon Processor 5500 Series-Based Intel Xeon 5500 Platform VccP Power Delivery Impedance Model Path – Example



The Intel Xeon 5500 Platform processor decoupling design includes large bulk caps and MLCC high-frequency capacitors and they are distributed per Table 2-5. The parasitic board values are extracted from Intel Xeon 5500 Platform design using an 8-layer board with 4 oz total of copper for Vcc and 6 oz total of copper for ground. Consult the latest *Intel® Xeon® 5500 Platform Design Guide* for more details about the board stackup.

Table 2-5. Intel Xeon 5500 Platform Processor Bulk/Decoupling Capacitors – CRB Examples

CPU Vcore VR	Cap type	Quant	ESR (mΩ)	ESL (nH)	Step Load maximum Slew Rate (A/µs)	Notes
Intel Xeon Processor 5500 Series	330 µF/2V/20%/Tant 3018LF	3	6	1.27	300	bulk caps
	22 µF/6.3V/20%/X5R/0805	12	5	0.55		place close to the socket
	47 µF/6.3V/10%/X6S/1206	26	4	0.52		socket cavity

For VRM11.1 (module) applications, it is recommended that the system designer should work with the VRM supplier to ensure proper implementation of the VRM converter.

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3 Input Voltage and Current

3.1 Input Voltages – EXPECTED

The power source for the VRM/EVRD is **12 V +5% / –8%**. This voltage is supplied by a separate power supply. For input voltages outside the normal operating range, the VRM/EVRD 11.1 should either operate properly or shut down.

3.2 Load Transient Effects on Input Current – EXPECTED

The design of the VRM/EVRD, including the input power delivery filter, must ensure that the maximum slew rate of the input current does not exceed **0.5 A/µs**, or as specified by the separate power supply.

Note: In the case of a VRM design, the input power delivery filter may be located either on the VRM or on the baseboard. The decision for the placement of the filter will need to be coordinated between the baseboard and VRM designers.

It is recommended that the bulk input decoupling (with series **0.1-1 µH** inductor) be placed on the baseboard by the VRM input connector and high frequency decoupling on the VRM module. Expected baseboard decoupling should be between **1000µF to 2240µF** depending on VRM design and system power supply.

§

4 Vcc Output Voltage Protection

These are features built into the VRM/EVRD 11.1 to prevent fire, smoke, or damage to itself, the processor, and/or other system components.

4.1 Over-Voltage Protection (OVP) – EXPECTED

The OVP circuit monitors the processor core voltage (Vcc) for an over-voltage condition. If the VR output's momentary overshoot is more than **200 mV** above the VID level, in steady VID condition, the VRM/EVRD 11.1 should shut off its output and latch off. OVP circuit should allow for a normal dVID change conditions. Un-latching may be performed by toggling off/on the VR's input power.

4.2 Over-Current Protection (OCP) – EXPECTED

The core VRM/EVRD should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the unit. Output current under this condition will be limited to no more than **130%** of the maximum peak rated output load of the VR at thermal equilibrium under the specified ambient temperature and airflow. An OCP event should result in either of:

shutting down the VR's output and latching off

or

going into a hick-up mode for duration of the OCP event.

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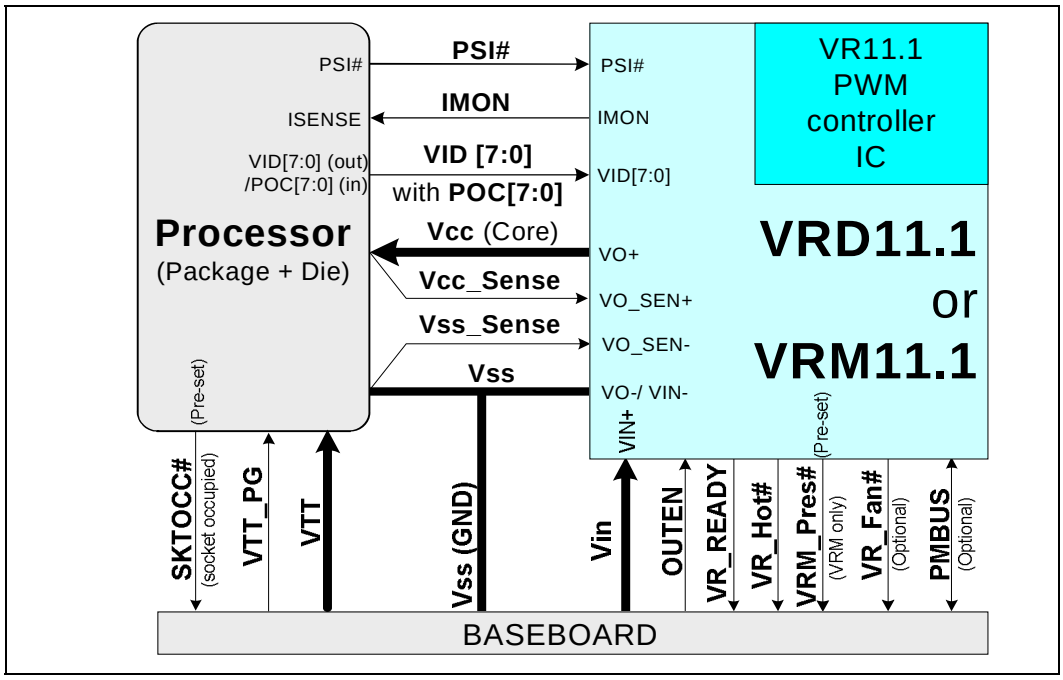
5 Control Input Signals

5.1 I/O Signals Overview

Figure 5-1. VR11.1 I/O Signals and Power Overview (Intel Xeon Processor 5500 Series Example)



Note: Future non-core applications are possible, to be edited in the next revision of this document.

5.2 Output Enable (OUTEN) – REQUIRED

The VR must accept an OUTEN input signal to enable its output voltage. When disabled, the VR's output should go to Hi-Z state and should not sink or source current. When OUTEN is pulled low during the shutdown process, the VR must not exceed the previous voltage level regardless of the VID setting during the shutdown process. Once operating after power-up, it must respond to the SM.

Table 5-1. OUTEN Specifications

Symbol	Parameter	Min	Max	Remarks
VIH	Input Voltage High	0.8V	3.465V	asserted, VR On
VIL	Input Voltage Low	0V	0.4V	de-asserted, VR Off, output in Hi-Z state

5.3 Voltage Identification VID [7:0] – REQUIRED

The VRM/EVRD 11.1 PWM controller must accept an 8-bit code, VID [7:0], from the processor to set the Vcc operating voltage. The VID bus interface should be designed as a 1.0 V logic compliant for pull-up to Vtt voltage rails (typically 1.0 to 1.2 V). See Table 5-2 for signaling levels. The VID bus will be driven by the CPU with push-pull CMOS drivers. The VR 11.1 standard code is listed in Table 5-4. There are four VID off states:

VID [7:0] = **00000000b (=00h), 00000001b (=01h), 11111110b (=FEh), or 11111111b (=FFh).**

as shown in Table 5-4 and Table 5-5. Once the VR is operating after power-up, and a specific VID off-code is received from the CPU, the VR must turn off its output (the output should go to Hi-Z) within Tk time and latch off until power is re-cycled, see Figure 2-7.

These Off states may only be sent by the CPU. The VR's PWM is responsible for avoiding false turn-off by off-code tripping. This can be accomplished by various known technics to prevent false turn off conditions due to noise, and so on. During normal operation a VID off code indicates a catastrophic failure condition from the CPU.

Because the VID lines are designed to serve dual function: VID coding and POC pre-setting (during startup), there are no default pull-up or pull-down resistors placed on each VID line which could automatically force an Off-code in absence of the CPU (as was the case in VR11.0). During startup, CPU output signal SKTOCC# (*socket occupied*) must be used as sole CPU presence detector, see Figure 2-6.

During the turn-on sequence, the VR should ramp to Vboot. If an off code is issued, the VR should not turn off until the end of Td. If the VID has changed to a normal VID code, then the VR should ramp to that voltage as normal. PWM controller should not load the VID lines during UVLO, Tb-Td time periods.

VID lines need to be routed as matched length traces to ensure **<200 ns** skew at PWM VID input pins.

Table 5-2. Interface Input Signal Logic Levels Specifications

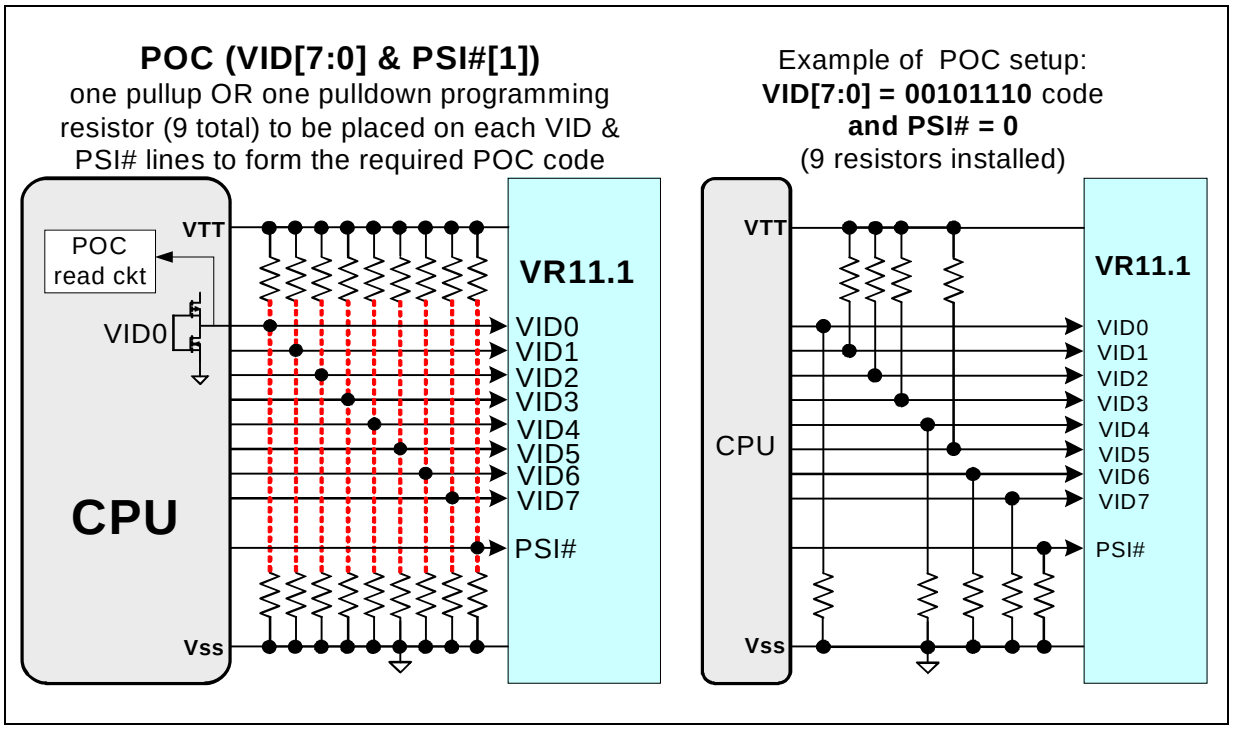
Symbol	Parameter	Min	Max	Notes
V_{IH}	Input Logic High	0.8 V	Vtt max	1
V_{IL}	Input Logic Low	0	0.3 V	1
Vtt	Pull-Up voltage		1.2 V [3]	typ 1.05 V-1.2 V [3]
Ileak [3]	CPU's CMOS driver leakage current	20 µA	200 µA	

Notes:
1. Pull-up resistors must not be integrated into the PWM controller (values may be adjusted on the system board for dynamic VID signal integrity and CPU compatibility). Processor damage could result if the PWM IC drives the VID line with an internal pull-up supply.
2. PWM controller must not load VID lines prior to the end of Td in the start up sequence.
3. The pull-up voltage, typically Vtt=1.1 V-1.2 V, see your Platform Design Guide for specific data on it.

5.3.1 Power-On Configuration (POC) Signals on VIDs (For Reference Only)

All 8 VID lines will serve a second function: the Power On Configuration (POC) logic levels are MUX-ed onto the VID lines with 1k-5k/5% range pull-ups and pull-downs and they will be read by the CPU during the time – as shown in Figure 2-6. The POC configuration programs the CPU as to the platform VR capabilities. **The VR does not read POC configuration resistors.** After OUTEN is asserted the CPU VID CMOS drivers override the POC pull-up / pull-down resistors. See Figure 2-6 and Figure 5-2 for more information. The following POC information is provided here for reference only.

Figure 5-2. POC Pull-up and Pull-down Resistors Placement



The CPU POC bits (MUX-ed with 8 VID lines) are allocated as follows (for reference only):

- **POC_{VID}[7]** = see respective PDG and/or EMTS.
- **POC_{VID}[6]** = see respective PDG and/or EMTS.
- **POC_{VID}[5:3]/CSC[5:3]** = Current Sense Config bits/ IMON slope gain setting, see Table 6-4.
- **POC_{VID}[2:0]** = see respective PDG and/or EMTS

5.4 Power State Indicator (PSI#) – EXPECTED (2)

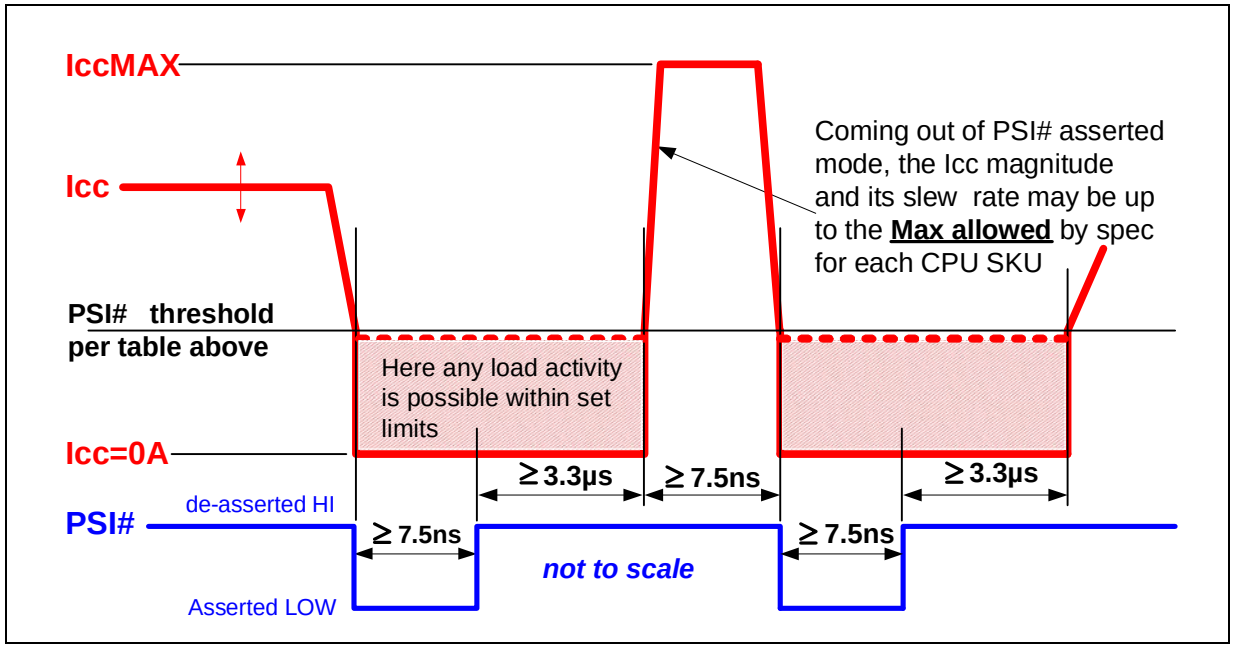
PSI# is an **input logic signal** (active Low) to the VR controller, sent by the CPU, which indicates when the CPU is in a low power state, as follows:

Table 5-3. PSI# Signal Function

PSI# Logic State	CPU IccCore for Nehalem-EP CPUs	VR Min. Efficiency / Max power dissipation	Notes
	-EP all SKUs		
1 = De-asserted (CPU normal power state)	> 20 A	> 80%	1
0 = Asserted (CPU low power state)	**4A** to **20A**	≤ 5W total VR power dissipation	1, 2
	< 4 A	N/A	

Notes:
1. Consult the latest revision of the respective CPU EMTS document for the updated PSI# threshold limit values.
2. The target efficiencies are platform specific and may be set higher by the VR/platform designer, depending on the design objectives.
   For applications with high efficiency VR11.1 design, it is acceptable to ignore the PSI# signal (and leave it open), while still meeting the low power mode max VR power dissipation recommended limit.
3. For future compatibility, in PSI# asserted mode, the VR11.1 has to be able to accept min load at 0A.
4. PSI# is 1 V CMOS logic compliant signal, driven by a push-pull gate (no pull-up / pull down resistors) as described in Table 5-2.

Figure 5-3. PSI# Assertion / De-Assertion Timing (worst case)



Notes:
1. The CPU is capable of this very short min PSI# assertion (dwell) time, which is too fast to be useful to the VR, so the VR's PSI# input may need to have installed a low-pass filter circuit (analog or digital, external or internal, as recommended by the PWM maker).
2. PSI# will de-assert for any positive dVID transition 12.5 mV or higher, even if the Icc remains below the PSI# set threshold limit.

The VR PWM controller may use this signal to change its operating state to maximize energy efficiency at light loads or flatten out its efficiency curve for idle power reduction. Per Intel Xeon Processor 5500 Series CPU spec, PSI# min asserted dwell time is 7.5 ns and the CPU's worst case, max assert / de-assert frequency is 133 MHz.

Therefore, for the VR to be able to take advantage of it, its PSI# input low-pass filter's equivalent cutoff frequency may need to be set in 1 kHz ~ 10 kHz range. Many VR11.1 PWM ICs already have some sort of PSI input analog and/or digital filtering in place. Consult your PWM IC spec sheet (or its manufacturer's FAE) for the optimal PSI filter value that will maximize VR energy efficiency in low power state.

It's critical to ensure that during Low to High power mode state transitions, the VR's OCP will never be triggered, as this would be a catastrophic VR failure.

While under PSI# asserted mode the Vcc output Pk-Pk ripple voltage is allowed to increase by up to additional ±**5 mV pp**.

Measurement of the VR's light load efficiency under PSI# asserted will be taken 1 minute after assertions of PSI# with a 12 V nominal input voltage and nominal VID setting. See the applicable platform design guidelines for additional details.

Note: During VR bench testing in PSI# asserted mode, the following spec limits may be used:

- dVID estimate: ~ 1.0 V, may vary by ±12.5 mV max
- Icc Step Max / Slew Rate Max estimate: 16Ap-p with 32 A/µs slew rate with up to 1 MHz rep rate.
- overshoot allowance during PSI# Hi-to-Low or Low-to-Hi transitions: use limits described in Section 2.4
- Load Line: the same LL as in full power mode, but with TOB enlarged from +0/-30 mV to: +10 mV/-30 mV.

Table 5-4. VR 11.1 Voltage Identification (VID) Table – Part 1 of 2

Hex	VID 7 800mV	VID 6 400mV	VID 5 200mV	VID 4 100mV	VID 3 50mV	VID 2 25mV	VID 1 12.5mV	VID 0 6.25mV	Vcc_Max (V)	Hex	VID 7 800mV	VID 6 400mV	VID 5 200mV	VID 4 100mV	VID 3 50mV	VID 2 25mV	VID 1 12.5mV	VID 0 6.25mV	Vcc_Max (V)
00	0	0	0	0	0	0	0	0	OFF*	40	0	1	0	0	0	0	0	0	1.21250
01	0	0	0	0	0	0	0	1	OFF*	41	0	1	0	0	0	0	0	1	1.20625
02	0	0	0	0	0	0	1	0	1.60000	42	0	1	0	0	0	0	1	0	1.20000
03	0	0	0	0	0	0	1	1	1.59375	43	0	1	0	0	0	0	1	1	1.19375
04	0	0	0	0	0	1	0	0	1.58750	44	0	1	0	0	0	1	0	0	1.18750
05	0	0	0	0	0	1	0	1	1.58125	45	0	1	0	0	0	1	0	1	1.18125
06	0	0	0	0	0	1	1	0	1.57500	46	0	1	0	0	0	1	1	0	1.17500
07	0	0	0	0	0	1	1	1	1.56875	47	0	1	0	0	0	1	1	1	1.16875
08	0	0	0	0	1	0	0	0	1.56250	48	0	1	0	0	1	0	0	0	1.16250
09	0	0	0	0	1	0	0	1	1.55625	49	0	1	0	0	1	0	0	1	1.15625
0A	0	0	0	0	1	0	1	0	1.55000	4A	0	1	0	0	1	0	1	0	1.15000
0B	0	0	0	0	1	0	1	1	1.54375	4B	0	1	0	0	1	0	1	1	1.14375
0C	0	0	0	0	1	1	0	0	1.53750	4C	0	1	0	0	1	1	0	0	1.13750
0D	0	0	0	0	1	1	0	1	1.53125	4D	0	1	0	0	1	1	0	1	1.13125
0E	0	0	0	0	1	1	1	0	1.52500	4E	0	1	0	0	1	1	1	0	1.12500
0F	0	0	0	0	1	1	1	1	1.51875	4F	0	1	0	0	1	1	1	1	1.11875
10	0	0	0	1	0	0	0	0	1.51250	50	0	1	0	1	0	0	0	0	1.11250
11	0	0	0	1	0	0	0	1	1.50625	51	0	1	0	1	0	0	0	1	1.10625
12	0	0	0	1	0	0	1	0	1.50000	52	0	1	0	1	0	0	1	0	1.10000
13	0	0	0	1	0	0	1	1	1.49375	53	0	1	0	1	0	0	1	1	1.09375
14	0	0	0	1	0	1	0	0	1.48750	54	0	1	0	1	0	1	0	0	1.08750
15	0	0	0	1	0	1	0	1	1.48125	55	0	1	0	1	0	1	0	1	1.08125
16	0	0	0	1	0	1	1	0	1.47500	56	0	1	0	1	0	1	1	0	1.07500
17	0	0	0	1	0	1	1	1	1.46875	57	0	1	0	1	0	1	1	1	1.06875
18	0	0	0	1	1	0	0	0	1.46250	58	0	1	0	1	1	0	0	0	1.06250
19	0	0	0	1	1	0	0	1	1.45625	59	0	1	0	1	1	0	0	1	1.05625
1A	0	0	0	1	1	0	1	0	1.45000	5A	0	1	0	1	1	0	1	0	1.05000
1B	0	0	0	1	1	0	1	1	1.44375	5B	0	1	0	1	1	0	1	1	1.04375
1C	0	0	0	1	1	1	0	0	1.43750	5C	0	1	0	1	1	1	0	0	1.03750
1D	0	0	0	1	1	1	0	1	1.43125	5D	0	1	0	1	1	1	0	1	1.03125
1E	0	0	0	1	1	1	1	0	1.42500	5E	0	1	0	1	1	1	1	0	1.02500
1F	0	0	0	1	1	1	1	1	1.41875	5F	0	1	0	1	1	1	1	1	1.01875
20	0	0	1	0	0	0	0	0	1.41250	60	0	1	1	0	0	0	0	0	1.01250
21	0	0	1	0	0	0	0	1	1.40625	61	0	1	1	0	0	0	0	1	1.00625
22	0	0	1	0	0	0	1	0	1.40000	62	0	1	1	0	0	0	1	0	1.00000
23	0	0	1	0	0	0	1	1	1.39375	63	0	1	1	0	0	0	1	1	0.99375
24	0	0	1	0	0	1	0	0	1.38750	64	0	1	1	0	0	1	0	0	0.98750
25	0	0	1	0	0	1	0	1	1.38125	65	0	1	1	0	0	1	0	1	0.98125
26	0	0	1	0	0	1	1	0	1.37500	66	0	1	1	0	0	1	1	0	0.97500
27	0	0	1	0	0	1	1	1	1.36875	67	0	1	1	0	0	1	1	1	0.96875
28	0	0	1	0	1	0	0	0	1.36250	68	0	1	1	0	1	0	0	0	0.96250
29	0	0	1	0	1	0	0	1	1.35625	69	0	1	1	0	1	0	0	1	0.95625
2A	0	0	1	0	1	0	1	0	1.35000	6A	0	1	1	0	1	0	1	0	0.95000
2B	0	0	1	0	1	0	1	1	1.34375	6B	0	1	1	0	1	0	1	1	0.94375
2C	0	0	1	0	1	1	0	0	1.33750	6C	0	1	1	0	1	1	0	0	0.93750
2D	0	0	1	0	1	1	0	1	1.33125	6D	0	1	1	0	1	1	0	1	0.93125
2E	0	0	1	0	1	1	1	0	1.32500	6E	0	1	1	0	1	1	1	0	0.92500
2F	0	0	1	0	1	1	1	1	1.31875	6F	0	1	1	0	1	1	1	1	0.91875
30	0	0	1	1	0	0	0	0	1.31250	70	0	1	1	1	0	0	0	0	0.91250
31	0	0	1	1	0	0	0	1	1.30625	71	0	1	1	1	0	0	0	1	0.90625
32	0	0	1	1	0	0	1	0	1.30000	72	0	1	1	1	0	0	1	0	0.90000
33	0	0	1	1	0	0	1	1	1.29375	73	0	1	1	1	0	0	1	1	0.89375
34	0	0	1	1	0	1	0	0	1.28750	74	0	1	1	1	0	1	0	0	0.88750
35	0	0	1	1	0	1	0	1	1.28125	75	0	1	1	1	0	1	0	1	0.88125
36	0	0	1	1	0	1	1	0	1.27500	76	0	1	1	1	0	1	1	0	0.87500
37	0	0	1	1	0	1	1	1	1.26875	77	0	1	1	1	0	1	1	1	0.86875
38	0	0	1	1	1	0	0	0	1.26250	78	0	1	1	1	1	0	0	0	0.86250
39	0	0	1	1	1	0	0	1	1.25625	79	0	1	1	1	1	0	0	1	0.85625
3A	0	0	1	1	1	0	1	0	1.25000	7A	0	1	1	1	1	0	1	0	0.85000
3B	0	0	1	1	1	0	1	1	1.24375	7B	0	1	1	1	1	0	1	1	0.84375
3C	0	0	1	1	1	1	0	0	1.23750	7C	0	1	1	1	1	1	0	0	0.83750
3D	0	0	1	1	1	1	0	1	1.23125	7D	0	1	1	1	1	1	0	1	0.83125
3E	0	0	1	1	1	1	1	0	1.22500	7E	0	1	1	1	1	1	1	0	0.82500
3F	0	0	1	1	1	1	1	1	1.21875	7F	0	1	1	1	1	1	1	1	0.81875

Table 5-5. VR 11.1 Voltage Identification (VID) Table – Part 2 of 2

Hex	VID 7 800mV	VID 6 400mV	VID 5 200mV	VID 4 100mV	VID 3 50mV	VID 2 25mV	VID 1 12.5mV	VID 0 6.25mV	Vcc_Max (V)	Hex	VID 7 800mV	VID 6 400mV	VID 5 200mV	VID 4 100mV	VID 3 50mV	VID 2 25mV	VID 1 12.5mV	VID 0 6.25mV	Vcc_Max (V)
80	1	0	0	0	0	0	0	0	0.81250	C0	1	1	0	0	0	0	0	0	0.41250
81	1	0	0	0	0	0	0	1	0.80625	C1	1	1	0	0	0	0	0	1	0.40625
82	1	0	0	0	0	0	1	0	0.80000	C2	1	1	0	0	0	0	1	0	0.40000
83	1	0	0	0	0	0	1	1	0.79375	C3	1	1	0	0	0	0	1	1	0.39375
84	1	0	0	0	0	1	0	0	0.78750	C4	1	1	0	0	0	1	0	0	0.38750
85	1	0	0	0	0	1	0	1	0.78125	C5	1	1	0	0	0	1	0	1	0.38125
86	1	0	0	0	0	1	1	0	0.77500	C6	1	1	0	0	0	1	1	0	0.37500
87	1	0	0	0	0	1	1	1	0.76875	C7	1	1	0	0	0	1	1	1	0.36875
88	1	0	0	0	1	0	0	0	0.76250	C8	1	1	0	0	1	0	0	0	0.36250
89	1	0	0	0	1	0	0	1	0.75625	C9	1	1	0	0	1	0	0	1	0.35625
8A	1	0	0	0	1	0	1	0	0.75000	CA	1	1	0	0	1	0	1	0	0.35000
8B	1	0	0	0	1	0	1	1	0.74375	CB	1	1	0	0	1	0	1	1	0.34375
8C	1	0	0	0	1	1	0	0	0.73750	CC	1	1	0	0	1	1	0	0	0.33750
8D	1	0	0	0	1	1	0	1	0.73125	CD	1	1	0	0	1	1	0	1	0.33125
8E	1	0	0	0	1	1	1	0	0.72500	CE	1	1	0	0	1	1	1	0	0.32500
8F	1	0	0	0	1	1	1	1	0.71875	CF	1	1	0	0	1	1	1	1	0.31875
90	1	0	0	1	0	0	0	0	0.71250	D0	1	1	0	1	0	0	0	0	0.31250
91	1	0	0	1	0	0	0	1	0.70625	D1	1	1	0	1	0	0	0	1	0.30625
92	1	0	0	1	0	0	1	0	0.70000	D2	1	1	0	1	0	0	1	0	0.30000
93	1	0	0	1	0	0	1	1	0.69375	D3	1	1	0	1	0	0	1	1	0.29375
94	1	0	0	1	0	1	0	0	0.68750	D4	1	1	0	1	0	1	0	0	0.28750
95	1	0	0	1	0	1	0	1	0.68125	D5	1	1	0	1	0	1	0	1	0.28125
96	1	0	0	1	0	1	1	0	0.67500	D6	1	1	0	1	0	1	1	0	0.27500
97	1	0	0	1	0	1	1	1	0.66875	D7	1	1	0	1	0	1	1	1	0.26875
98	1	0	0	1	1	0	0	0	0.66250	D8	1	1	0	1	1	0	0	0	0.26250
99	1	0	0	1	1	0	0	1	0.65625	D9	1	1	0	1	1	0	0	1	0.25625
9A	1	0	0	1	1	0	1	0	0.65000	DA	1	1	0	1	1	0	1	0	0.25000
9B	1	0	0	1	1	0	1	1	0.64375	DB	1	1	0	1	1	0	1	1	0.24375
9C	1	0	0	1	1	1	0	0	0.63750	DC	1	1	0	1	1	1	0	0	0.23750
9D	1	0	0	1	1	1	0	1	0.63125	DD	1	1	0	1	1	1	0	1	0.23125
9E	1	0	0	1	1	1	1	0	0.62500	DE	1	1	0	1	1	1	1	0	0.22500
9F	1	0	0	1	1	1	1	1	0.61875	DF	1	1	0	1	1	1	1	1	0.21875
A0	1	0	1	0	0	0	0	0	0.61250	E0	1	1	1	0	0	0	0	0	0.21250
A1	1	0	1	0	0	0	0	1	0.60625	E1	1	1	1	0	0	0	0	1	0.20625
A2	1	0	1	0	0	0	1	0	0.60000	E2	1	1	1	0	0	0	1	0	0.20000
A3	1	0	1	0	0	0	1	1	0.59375	E3	1	1	1	0	0	0	1	1	0.19375
A4	1	0	1	0	0	1	0	0	0.58750	E4	1	1	1	0	0	1	0	0	0.18750
A5	1	0	1	0	0	1	0	1	0.58125	E5	1	1	1	0	0	1	0	1	0.18125
A6	1	0	1	0	0	1	1	0	0.57500	E6	1	1	1	0	0	1	1	0	0.17500
A7	1	0	1	0	0	1	1	1	0.56875	E7	1	1	1	0	0	1	1	1	0.16875
A8	1	0	1	0	1	0	0	0	0.56250	E8	1	1	1	0	1	0	0	0	0.16250
A9	1	0	1	0	1	0	0	1	0.55625	E9	1	1	1	0	1	0	0	1	0.15625
AA	1	0	1	0	1	0	1	0	0.55000	EA	1	1	1	0	1	0	1	0	0.15000
AB	1	0	1	0	1	0	1	1	0.54375	EB	1	1	1	0	1	0	1	1	0.14375
AC	1	0	1	0	1	1	0	0	0.53750	EC	1	1	1	0	1	1	0	0	0.13750
AD	1	0	1	0	1	1	0	1	0.53125	ED	1	1	1	0	1	1	0	1	0.13125
AE	1	0	1	0	1	1	1	0	0.52500	EE	1	1	1	0	1	1	1	0	0.12500
AF	1	0	1	0	1	1	1	1	0.51875	EF	1	1	1	0	1	1	1	1	0.11875
B0	1	0	1	1	0	0	0	0	0.51250	F0	1	1	1	1	0	0	0	0	0.11250
B1	1	0	1	1	0	0	0	1	0.50625	F1	1	1	1	1	0	0	0	1	0.10625
B2	1	0	1	1	0	0	1	0	0.50000	F2	1	1	1	1	0	0	1	0	0.10000
B3	1	0	1	1	0	0	1	1	0.49375	F3	1	1	1	1	0	0	1	1	0.09375
B4	1	0	1	1	0	1	0	0	0.48750	F4	1	1	1	1	0	1	0	0	0.08750
B5	1	0	1	1	0	1	0	1	0.48125	F5	1	1	1	1	0	1	0	1	0.08125
B6	1	0	1	1	0	1	1	0	0.47500	F6	1	1	1	1	0	1	1	0	0.07500
B7	1	0	1	1	0	1	1	1	0.46875	F7	1	1	1	1	0	1	1	1	0.06875
B8	1	0	1	1	1	0	0	0	0.46250	F8	1	1	1	1	1	0	0	0	0.06250
B9	1	0	1	1	1	0	0	1	0.45625	F9	1	1	1	1	1	0	0	1	0.05625
BA	1	0	1	1	1	0	1	0	0.45000	FA	1	1	1	1	1	0	1	0	0.05000
BB	1	0	1	1	1	0	1	1	0.44375	FB	1	1	1	1	1	0	1	1	0.04375
BC	1	0	1	1	1	1	0	0	0.43750	FC	1	1	1	1	1	1	0	0	0.03750
BD	1	0	1	1	1	1	0	1	0.43125	FD	1	1	1	1	1	1	0	1	0.03125
BE	1	0	1	1	1	1	1	0	0.42500	FE	1	1	1	1	1	1	1	0	off
BF	1	0	1	1	1	1	1	1	0.41875	FF	1	1	1	1	1	1	1	1	off

Notes:
1. VIDs below 0.5 V (shaded gray) are not supported as they are unusable.
2. The actual VID range used by a processor is typically narrower, see the appropriate EMTS for details.

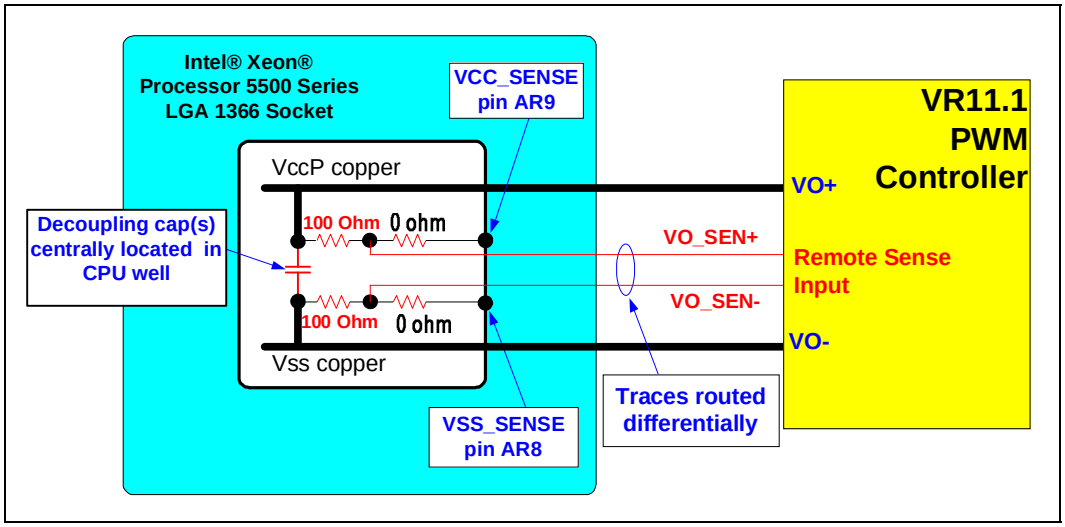
5.5 Differential Remote Sense (VO_SEN+/-) – REQUIRED

The PWM controller must include differential sense inputs (VO_SEN+, VO_SEN-) to compensate for an output voltage IR drop of ≤ **300 mV** (round trip) in the power distribution path. This common mode voltage is expected to occur due to transient currents and parasitic inductances and is not expected to be caused by parasitic resistances.

It's expected that the remote sense lines' Max current draw will be ≤ **500 µA** so it will not push the actual Load Line outside of the Load Line limits shown in Table 2-4. As a practical guideline to minimizing offset errors, it is recommended that the combination of the sense resistor values and the remote sense current draw will result in the total DC voltage offset ≤ **2 mV.**

Note: VCC_DIE_SENSE and VSS_DIE_SENSE of the processor pins are to be used as the VR sense input.

Figure 5-1. Remote Sense Routing – Intel® Xeon® Processor 5500 Series Example



Note:
1. For each processor, refer to the appropriate platform design guide (PDG) for the recommended VR's remote sense routing.

The sense lines should be routed based on the following guidelines:

- Route differentially with a maximum of 5 mils separation.
- Traces should be at least 25 mils thick, but may be reduced when routed through the processor pin field. Also, consider the PWM IC data sheet recommendations about it.
- Traces should have the same length.
- Traces should not exceed 5 inches in length and should not violate pulse-width modulation (PWM) vendor length requirements.
- Traces should be routed at least 20 mils away from other signals.
- Each sense line should include a 0 – 100 Ω, 5% series resistor that is placed close to the PWM or VRM connector in order to filter noise from the power planes. Designers should consult with their power delivery solution vendor to determine the appropriate resistor value.

- Reference a solid ground plane.
- Avoid switching layers.

On a VRM, the positive sense line will be connected to VO_SEN+ and the negative sense line will be connected to VO_SEN–.

The processor $V_{CC\_DIE\_SENSE}$ and $V_{SS\_DIE\_SENSE}$ pins should be connected to test points on the baseboard in order to probe the die voltage. These test points should be as close to the socket pins as possible.

5.6 PMBus* Support for Servers or Work Stations – Optional

Some OEMs may require PMBus* support for data collection from the VR. PWM ICs that support this function should comply with the PMBus* Application Profile for Vcore regulators for Compute Market Segment. See http://www.PMBUS.org for the latest application profile.

PMBus* can be used to implement DAC offset to shift the VID table for over clocking (and such), telemetry, programming of configuration registers, and so on.

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6 Indicator Output Signals

6.1 Voltage Regulator Ready (VR_Ready) – REQUIRED

The VRM/EVRD 11.1' s VR_Ready signal is an output logic signal that, when asserted HIGH, indicates the start-up sequence is complete and the output voltage has moved to the programmed VID value. This signal will be used for start-up sequencing for other voltage regulators, clocks, and microprocessor reset. **This signal is not a representation of the accuracy of the DC output to its VID value** (unlike a PWR_Good signal would)**.**

The platform VR_Ready signal(s) will be connected to logic to assert CPU or system PWRGD. The value of the resistor and the pull-up voltage will be determined by the circuitry on the baseboard that is receiving this signal. Typically a 1 kΩ pull up to 3.3 V is used. This signal should not be de-asserted during dynamic VID operation. It should remain asserted during normal DC-DC operating conditions and only de-assert for fault shutdown conditions. It will be an open-collector/drain or equivalent signal. The pull-up resistor and voltage source will be located on the baseboard. Table 6-1 shows the VR_Ready pin specification.

Table 6-1. VR_Ready Specifications

Symbol	Parameter	Min	Max	Remarks
I_{OL}	Output Low Current	**1mA**	**4mA**	
V_{OH}	Output High Voltage	**0.8V**	**3.465V**	asserted
V_{OL}	Output Low Voltage	**0V**	**0.4V**	de-asserted

6.2 Voltage Regulator Hot (VR_hot#) – EXPECTED

The VRM/EVRD VR_hot# signal is an output signal that is asserted LOW when a thermal event (overheating threshold, pre-OTP shutdown, if OTP is implemented) is detected in the converter. Assertion of this signal will be used by the system to minimize damage to the converter due to the thermal conditions. Table 6-2 shows the VR_hot# signal specification. This signal will be an open-collector/drain or equivalent signal and needs to be pulled up to an appropriate voltage through a pull-up resistor on the baseboard. A typical implementation would be a **50 Ω ±5%** resistor pulled up to **1.1 V/1.2 V.** For platforms using a voltage higher than 1.1 V /1.2 V, a voltage level translation is required. Processors do not tolerate such voltage levels directly. Consult the appropriate PDG.

Table 6-2. VR_hot# Specifications

Symbol	Parameter	Min	Max	Remarks
I_{OL}	Output Low Current	**19.9mA**	**30mA**	
V_{OH}	Output High Voltage	**0.8V**	**3.465V**	de-asserted
V_{OL}	Output Low Voltage	**0V**	**0.4V**	asserted

Each customer is responsible for identifying maximum temperature specifications for all components in the VRM/EVRD 11.1 design and ensuring that these specifications are not violated while continuously drawing specified IccTDC levels. In the occurrence of a

thermal event, a thermal sense circuit may assert the processor's PROCHOT# signal immediately prior to exceeding maximum VRM, baseboard, and/or component thermal ratings to prevent heat damage. The assertion may be made through direct connection to the PROCHOT# pin or through system management logic. Assertion of this signal will lower processor power consumption and reduce current draw through the voltage regulator, resulting in lower component temperatures. Sustained assertion of the PROCHOT# pin will cause noticeable platform performance degradation and should not occur when drawing less than the specified thermal design current for a properly designed system.

Thermal sensors should be external to the PWM control IC since the PWM control IC is normally not located near heat generating components. Thermal sensors need to be implemented in a manner that allows sensing of phase temperature.

It is recommended that adequate hysteresis be designed into the thermal sense circuit to prevent a scenario in which the VR_hot# signal is rapidly being asserted and de-asserted.The trip point needs to be externally programmable by the system designer. The hysteresis should be **~10 deg C**. The tolerance should be **±4%** or approximately **±4 deg C**.

Note: PWM IC has VR_HOT output (asserted High), which needs to be inverted (w/ one OC/OD transistor) to make VR_HOT#, per this specification.

6.3 Advanced Thermal Warning (VR_Fan#)- PROPOSED

VR_Fan# signal has the same electrical spec as VR_Hot#, but VR_fan is an output that toggles ~10% or approximately 10 deg C below the VR_hot# trip set point, allowing the system designer to turn on a fan or do other thermal management actions without initiating CPU's PROCHOT# thermal monitor low power state.

VR_fan# can be used for advanced thermal management on some platforms that have the ability to change the fan speed prior to asserting VR_HOT# and thus prior to forcing CPU thermal throttle through PROCHOT#. **This feature is optional.**

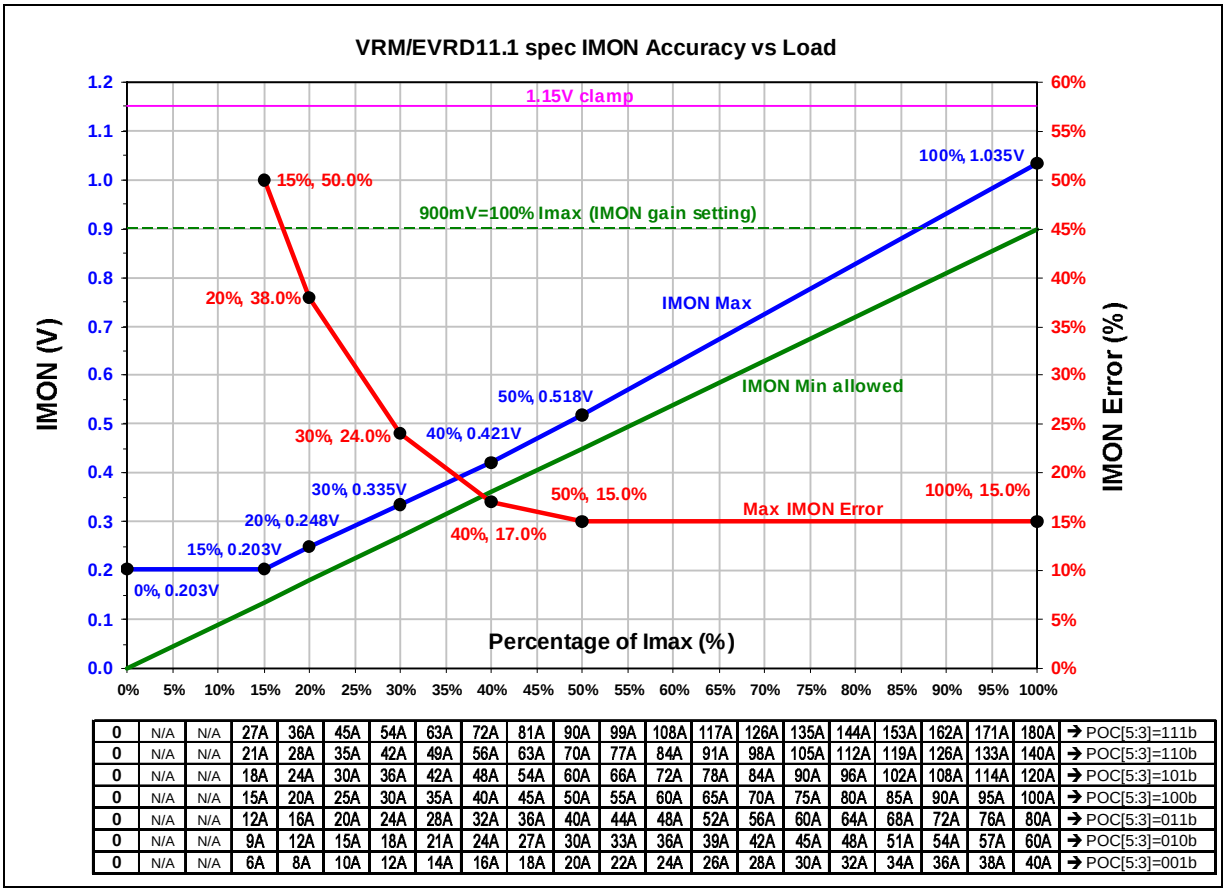
6.4 Load Current Monitor (IMON) – EXPECTED

IMON is an analog output signal proportional to the VR's total output load current. This signal will be connected directly to CPU's IMON. The IMON input leakage current will be ≤ **1µA**. Since the signal connects directly to the CPU, the maximum output voltage must be clamped 1.1-1.15 V (a voltage lower than the platform Vtt).

The proportional gain will be platform specific and thus needs to be externally programmable. The VR regulator on the platform will provide gain setting to CPU during Ta Power-On Configuration (POC) time. The POC levels are MUX-ed onto the VID lines with pull-ups & pull-downs resistors and read by the CPU during the Ta time (between Vtt_PG asserted and OUTEN asserting). At the end of Vboot the VID CMOS drivers override the POC pull-up, pull-down resistors. See Figure 5-2 for more information.

The information for total output current can come from the circuit blocks that generate the load line droop. IMON is expected to be temperature compensated in the same manner as the load line Vdroop. See Table 6-3 for gain definitions.

Figure 6-1. Output Current Monitor (IMON) Characteristic



0	N/A	N/A	27A	36A	45A	54A	63A	72A	81A	90A	99A	108A	117A	126A	135A	144A	153A	162A	171A	180A	→ POC[5:3]=111b
0	N/A	N/A	21A	28A	35A	42A	49A	56A	63A	70A	77A	84A	91A	98A	105A	112A	119A	126A	133A	140A	→ POC[5:3]=110b
0	N/A	N/A	18A	24A	30A	36A	42A	48A	54A	60A	66A	72A	78A	84A	90A	96A	102A	108A	114A	120A	→ POC[5:3]=101b
0	N/A	N/A	15A	20A	25A	30A	35A	40A	45A	50A	55A	60A	65A	70A	75A	80A	85A	90A	95A	100A	→ POC[5:3]=100b
0	N/A	N/A	12A	16A	20A	24A	28A	32A	36A	40A	44A	48A	52A	56A	60A	64A	68A	72A	76A	80A	→ POC[5:3]=011b
0	N/A	N/A	9A	12A	15A	18A	21A	24A	27A	30A	33A	36A	39A	42A	45A	48A	51A	54A	57A	60A	→ POC[5:3]=010b
0	N/A	N/A	6A	8A	10A	12A	14A	16A	18A	20A	22A	24A	26A	28A	30A	32A	34A	36A	38A	40A	→ POC[5:3]=001b

Warning: Under any operating or fault condition the voltage on IMON must not exceed 1.15 V to prevent damage to the processor input gate. At the other extreme, the absolute IMON Min voltage must not fall below -350 mV (350 mV below GND).

Table 6-3. IMON Recommended Accuracy Limits

I_{CC_CORE} (% of Imax)	IMON Absolute Min Allowed (0% error)	IMON Max	IMON Max Error	Remarks
100% of I_{MAX}	900 mV	1035 mV	+15% / -0%	I_{MAX} defined in Table 6-4. IMON max error includes ripple.
90% of I_{MAX}	810 mV	932 mV	+15% / -0%	
80% of I_{MAX}	720 mV	828 mV	+15% / -0%	
70% of I_{MAX}	630 mV	725 mV	+15% / -0%	
60% of I_{MAX}	540 mV	621 mV	+15% / -0%	
50% of I_{MAX}	450 mV	518 mV	+15% / -0%	
40% of I_{MAX}	360 mV	421 mV	+17% / -0%	
30% of I_{MAX}	270 mV	335 mV	+24% / -0%	
20% of I_{MAX}	180 mV	248 mV	+38% / -0%	
15% of I_{MAX}	135 mV	203 mV	+50% / -0%	
0% of I_{MAX}	0 mV	203 mV	n/a	

I_{MAX} is the regulators maximum current, corresponding to (equal or larger) the CPUs IccMax rating, not the VR's OCP level. The IMAX vs $I_{CC\_CORE\text{-}MAX}$ relationship is described in Table 6-4.

Table 6-4. I_{MAX} Definition – Relative to Processor's $I_{CC\_CORE\_MAX}$

CPU SKU, $I_{CC\_CORE\text{-}MAX}$ (Max CPU Core Current)	IMON gain (slope): 900 mV = I_{MAX} (see note below)	CPU gain setting set via POC/VID lines POC[5:3]
Feature disabled	N/A	000b
ICC_CORE-MAX £ 40 A	900 mV = 40A	001b
40 A < ICC_CORE-MAX £ 60 A	900 mV = 60A	010b
60 A < ICC_CORE-MAX £ 80 A	900 mV = 80A	011b
80 A < ICC_CORE-MAX £ 100 A	900 mV = 100A	100b
100 A < ICC_CORE-MAX £ 120 A	900 mV = 120A	101b
120 A < ICC_CORE-MAX £ 140 A	900 mV = 140A	110b
140 A < ICC_CORE-MAX £ 180 A	900 mV = 180A	111b

Note: IMON slope has to be set according to your VR11.1 PWM data sheet; For most PWMs, it takes one or two set resistors.

Assumptions used for the IMON accuracy recommended limits: Intel CRB VRD11.1 design 130W SKU (or 95W SKU) using 4 phase coupled inductor VR with DCR current sensing (±8% DCR tolerance) assuming 3-Sigma distribution in production. VR designs for lower SKUs (IMAX ≤ 100A) would typically use 3 or 2 phase converters with individual inductors having ±5% (or better) DCR tolerance. Current sense resistors or other, more accurate current sensing methods are also available, which may further improve the IMON accuracy.

In order to minimize offset errors and noise coupling, IMON signal from the PWM should be routed to CPU as shown in the table below.

Table 6-5. IMON (PWM) to ISENSE (CPU) Recommended Routing

CPU family	VR PWM connect with ---------> CPU		Notes
Intel® Xeon® Processor 5500 Series Performance WS Processor	IMON	ISENSE	routed differentially, follow your PWM data sheet recommendation
	IMON Return (Analog GND)	VSS_SENSE	

It is expected that, regardless of the implementation method, the max current drawn on reference (Vss_sense) pin will be ≤ **500 µA** due to both IMON and VR's remote sense bias currents (also see Section 5.5). Consult the appropriate platform design guidelines for the recommended layout.

IMON signal must have a low-pass RC filter with time constant ~**300 µs**, which translates to **~500 Hz** cutoff frequency, to prevent ADC aliasing in the CPU. This time constant value should be well above the L/R time constant of typical VR output inductors.

The VRD11.1 generic accuracy guidelines are shown in Figure 6-1 and Table 6-3. Any particular IMON solution total accuracy will be defined by the PWM controller, inductor DCR tolerance (if solution implements inductor current sensing), current sense lines routing (coupled noise rejection) and external IMON slope setting resistors.

It is highly recommended that the IMON linearity and accuracy will be maximized. More accurate IMON reporting will have a positive impact on CPU *Intel® Turbo Boost Technology* performance. The most useful IMON accuracy region is in approx. 30% to 90% of TDC, inside the IMAX range, for each CPU SKU.

Example: for Intel® Xeon® Processor 5500 Series Performance WS Processor 130W SKU, IMAX=180A, TDC=110A, so 33A to 99A (which is 18% to 55% of IMAX) is the load range where tight IMON accuracy is most useful to CPU *Intel Turbo Boost Technology*. Outside of that range, IMON accuracy is less important, although it is expected to still be inside the spec.

PWM vendors should provide the accuracy graphs to the MB designer to aid in component and PWM selection. Consult the latest revision of the related Platform Design Guide for possible additional IMON accuracy requirements.

6.5 VRM Present (VRM_Pres#x) Signals – PROPOSED

The VRM11.1 (module only) should have these three output signals: VRM_Pres# 0, VRM_Pres# 1 and VRM_Pres# 2, which serve 2 functions:

1. to indicate to the system that a VRM 11.1 module is plugged into the socket
2. electronic keying (See Section 7.3.1 for details.)

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7 VRM – Mechanical Guidelines

7.1 VRM Connector – EXPECTED

The part number and vendor name for VRM 11.1 connectors that can be found in Table 7-1. The VRM reference in Section 7.2, Section 7.3 and Section 7.4, is based on the Tyco*/Elcon* interface with the system board is a 27-pin pair edge connector. The connector uses latches to hold the VRM in place. The connector will be rated to handle a continuous load current of **130 A**.

Table 7-1. VRM 11.1 Connector Part Number and Vendor Name

Connector	Vendor Part Number	Notes
Tyco / Elcon	1651929-1 (Solder Tail) 1766336-1 (Surface Mount) 1766436-1 (Press-Fit)	1
Molex	Molex iCool* VRM 24 signal 70 power pins 87787-1012 (Vertical, TH) 87786-1011 (Vertical, SM) 87818-1011 (Right Angle, TH)	1, 2

Notes:
1. These vendors are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change.
2. An alternative connector has been identified by Molex for VRMs. This alternative provides many optional connector variants already in production in both vertical and horizontal (right angle) implementation. Contact your Molex representative for pin assignment, mechanical form factor details and performance characteristic data.

7.2 VRM (Tyco/Elcon) Connector Keying

7.2.1 Connector Keying

- Single notch between pins 3 and 4 (51 and 52 opposite side).
- Single notch between pins 12 and 13 (42 and 43 opposite side).
- Single notch between pins 21 and 22 (33 and 34 opposite side).

7.2.2 Connector Pin 1 Orientation

Referencing Figure 7-1, Outline Drawing, Far Side (FS) pins sequence 1 through 27, left to right. Near Side (NS) pins sequence 54 through 28. Pin 1 and 54 are opposite one another.

7.3 Pin Descriptions and Assignments

Table 7-2 shows the VRM11.1 connector pin description. Pin assignments are shown in Table 7-3.

Table 7-2. VRM 11.1 Connector Pin Descriptions

Name	Type	Description
IMON	Output	Analog voltage signal representing the output load current
OUTEN	Input	Output enable
VR_Ready	Output	Output signal indicating that the start-up sequence is complete and the output voltage has moved to the programmed VID value.
VID [7:0] / / POC	Input	Voltage ID pins used to specify the VRM output voltage. The MUX-ed POC function is transparent to the VR.
VIN+	Power	VRM Input Voltage
VIN–	Ground	VRM Input Ground
VO+	Power	VRM Output Voltage
VO–	Ground	VRM Output Ground
VO_SEN+ VO_SEN–	Input	Output voltage sense pins
VR_hot#	Output	Indicates to the system that a thermal event has been detected in the VR
VRM_pres# x	Output	VRM11.1 presence indicator(s)
PSI#	Input	Indicates CPU's low power state

Note: VR_FAN# and PMBus* as optional I/O signals are not listed for lack of available pins in this connector

Table 7-3. VRM 11.1 Pinout Assignments

VRM11.1 Pinout			
Pin #	**Signal**	**Pin #**	**Signal**
1	VIN-	54	VIN+
2	VIN-	53	VIN+
3	VIN-	52	VIN+
KEY			KEY
4	VID4	51	VID3
5	VID2	50	VID1
6	VID0	49	VID5
7	VO_SEN+	48	VO_SEN-
8	VR_Ready	47	VR_hot#
9	OUTEN	46	VID7
10	IMON	45	PSI
11	VID6	44	VRM_pres#0
12	VRM_pres#2	43	VRM_pres#1
KEY			KEY
13	VO+	42	VO+
14	VO+	41	VO+
15	VO+	40	VO+
16	VO-	39	VO-
17	VO-	38	VO-
18	VO-	37	VO-
19	VO+	36	VO+
20	VO+	35	VO+
21	VO+	34	VO+
KEY			KEY
22	VO-	33	VO-
23	VO-	32	VO-
24	VO-	31	VO-
25	VO+	30	VO+
26	VO+	29	VO+
27	VO+	28	VO+

Notes:
1. This is the preliminary pinout, subject to change in the next revision of the spec.
2. Pins 12, 43, and 44 may be used instead of or in addition to – as optional PMBus* support.

7.3.1 VRM11.1 Electrical Keying – PROPOSED

The VRM11.1 has the same connector and keying as the existing VRM10.x and VRM11.0, but electrically is incompatible. In order to prevent the VR11.1 from turning on when accidentally plugged into VRM10.x / VRM11.0 compatible boards, or conversely, to prevent those older VRMs from powering on when accidentally plugged into the VRM11.1 compatible bd, the electrical keying is proposed.

The proposed VRM11.1 pinout includes 3 different VRM_Present pins with logic functions as follows:

- **VRM_Present# 0** (pin 44) = **Logic 0** (grounded) on VRM side
- **VRM_Present# 1** (pin 43) = **open** (no-connect) on VRM side
- **VRM_Present# 2** (pin 12) = **open** (no-connect) on VRM side

Table 7-4. VRM11.1 Electrical Keying Verifications

	Pin 12	Pin 43	Pin 44
VRM10.x internal	(VRM_Pres#) **GND**	N/C, **Open**	N/C, **Open**
VRM11.0 internal	(VRM_Pres#) **GND**	(VR_ID#) **GND**	(VID_Select) **Open**
VRM11.1 internal	(VRM_Pres#2) **Open**	(VRM_Pres#1) **Open**	(VRM_Pres#0) **GND**
Truland bd. side	**Pull-Up**	**Open**	**Open**
Caneland bd. side	**Pull-Up**	**Pull-Up**	**Pull-Up**
Tylersburg-EP (Thurley) bd. side	**Pull-Up**	**Pull-Up**	**Pull-Up**

Case 1:

If VRM10.x is plugged into an Intel Xeon 5500 Platform board, the system will detect pin 44 as open and will not enable the VR.

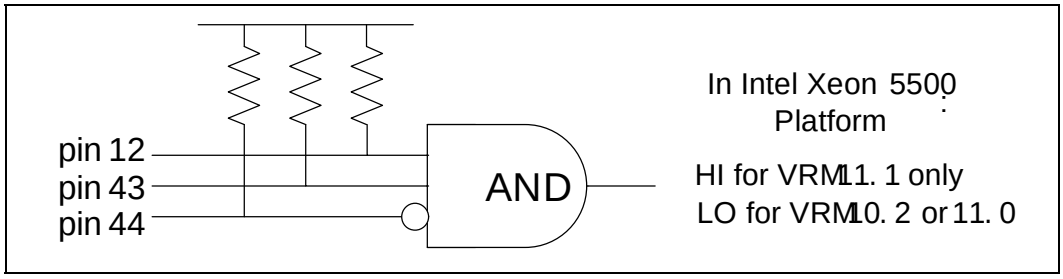
Case 2:

If VRM11.0 is plugged into a VRM11.1 only Intel Xeon 5500 Platform board, the system will detect pin 44 as open and pin 12/43 as grounded and will not enable the VR.

Case 3:

If VRM11.1 is plugged into a non-Intel Xeon 5500 Platform board, the system will detect pin 12 as open and pin 44 as grounded and will not enable the VR.

Figure 7-1. Electrical Keying – System Logic Implementation Concept – Example



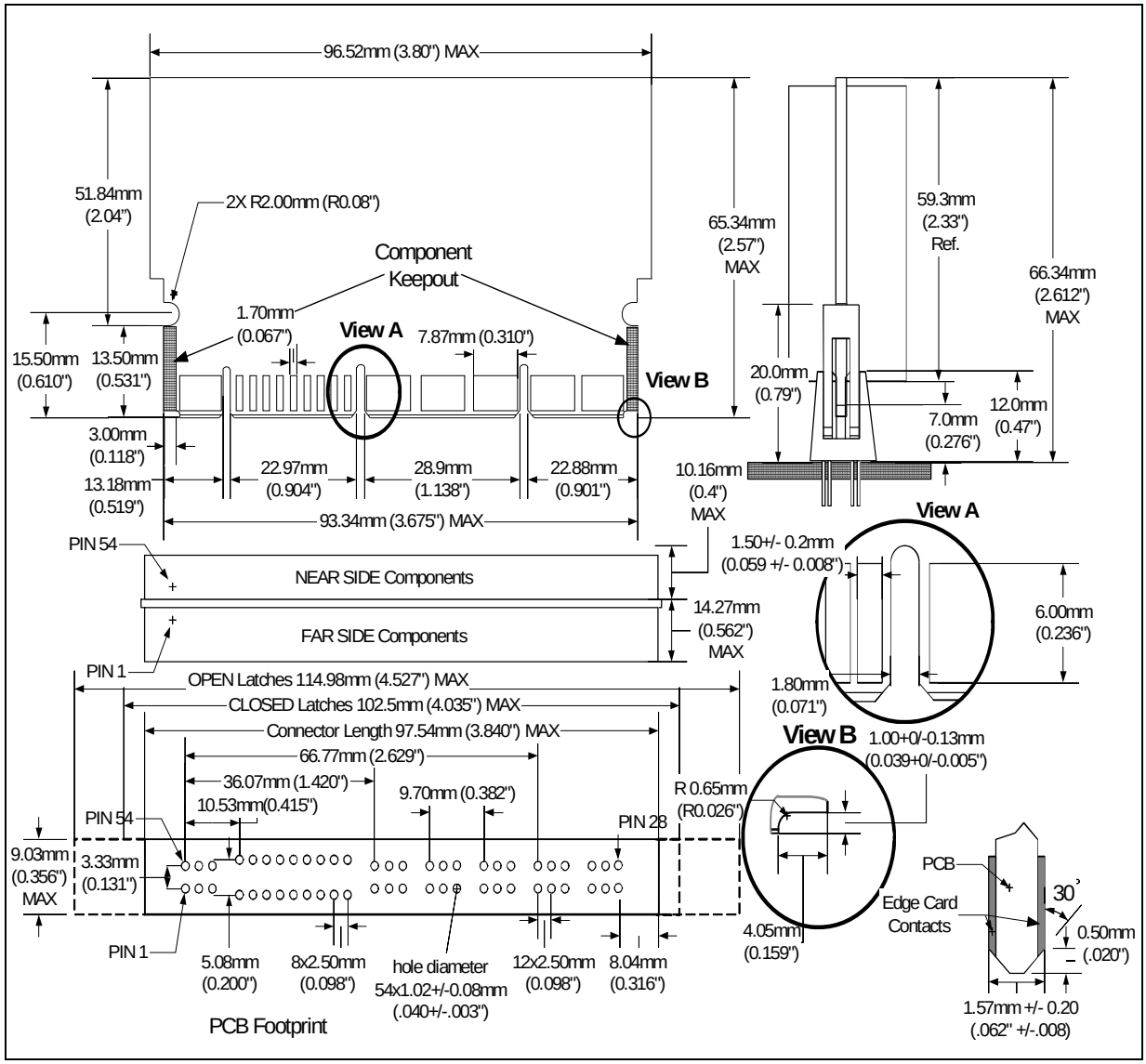
7.4 Mechanical Dimensions – PROPOSED

The mechanical dimensions for the VRM 11.1 module and connector are shown in Figure 7-1.

7.4.1 Gold Finger Specification

The VRM board must contain gold lands (fingers) for interfacing with the VRM connector that is 1.50 mm ±0.2 mm [0.059” ±0.008”] wide by 6.00 mm [0.236”] minimum long and spaced 2.50 mm [0.098”] apart. Traces from the lands to the power plane should be a minimum of 0.89 mm [0.035”] wide and of a minimal length.

Figure 7-1. VRM 11.1 Module and Connector



This form factor is the same as in VRM11.0. There is a study under way whether changing the total height from the one shown 66.34 mm (2.612”) to a new 1U height: 34.0 mm (1.34”) and the total width from the one shown 24.43 mm (0.962”) to a new 13.0 mm (0.5”) is feasible and justifiable by the market demand. Subject to change in the next spec revision.

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8 Environmental Conditions

The VRM/EVRD design, including materials, should meet the environmental requirements specified below.

8.1 Operating Temperature – PROPOSED

The VRM/EVRD shall meet all electrical requirements when operated at the Thermal Design Current (Icc_{TDC}) over an ambient temperature range of 0ºC to +45ºC with a minimum airflow of 400 LFM (2 m/s). The volumetric airflow (Q) can be measured through a wind tunnel. For testing, the baseboard should be mounted in a duct. (A VRM should be mounted on a PCB, and then mounted in a duct.) The recommended duct cross-section, assuming the PCB is horizontal and flush with the bottom of the duct, is as follows:

- Y direction duct width (perpendicular to flow, horizontal) = 0.3 m
- Z direction duct height (perpendicular to flow, vertical) = 0.15 m
- Minimum X direction duct length in front of VRM = 6 hydraulic diameters = 1.2 m
- Minimum X direction duct length behind VRM = 2 hydraulic diameters = 0.4 m
- Velocity (v) is calculated from the volumetric flow and cross-sectional area at the inlet as:
- $v = Q/(0.3 \times 0.15)m^2$ Operating conditions shall be considered to include 10 cycles between min and max temperature at a rate of 10ºC/hour and a dwell time of 30 minutes at extremes. Temperature and airflow measurements should be made in close proximity to the VRM.

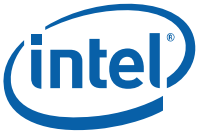
8.1.1 Thermal Drift Bench Test – Proposed

In order to quickly gauge the quality of thermal stability (thermal compensation) of the VR Under Test, a thermal drift bench test is recommended.

Verify that the selected DC and AC voltage regulation tests pass also after 5-10 min of staying under full TDP load with minimal recommended air flow, in room temperature. Consult the latest VRTT (VR Test Tool) test spreadsheet for the test details.

8.2 VRM Board Temperature – REQUIRED

To maintain the connector within its operating temperature range, the VRM board temperature, at the connector interface, shall not exceed a temperature equal to 90ºC. At no time during the operation is the board permitted to exceed 90ºC within a distance of 2.54 mm [0.100”] from the top of connector (0.4 in. from board edge). In order not to exceed 90ºC, it is recommended that the board be constructed from 2-ounce copper cladding. Temperature and airflow measurements should be made in close proximity to the VRM.



8.3 Non-Operating Temperature – PROPOSED

The VRM/EVRD shall not be damaged when exposed to temperatures between –40ºC and +70ºC. These shall be considered to include 50 cycles of minimum to maximum temperatures at 20ºC/hour with a dwell time of 20 minutes at the extremes.

8.4 Humidity – PROPOSED

85% relative – operating

95% relative – non-operating

8.5 Altitude – PROPOSED

3.05 km [10 k feet] – operating

15.24 km [50 k feet] – non-operating

8.6 Electrostatic Discharge – PROPOSED

Testing shall be in accordance with IEC 61000-4-2.

Operating – 15 kV initialization level. The direct ESD event shall cause no out-of-regulation conditions – including overshoot, undershoot and nuisance trips of over-voltage protection, over-current protection or remote shutdown circuitry.

Non-operating –25 kV initialization level. The direct ESD event shall not cause damage to the VRM circuitry.

8.7 Shock and Vibration – PROPOSED

The shock and vibration tests should be applied at the baseboard level. The VRM/EVRD should not be damaged and the interconnect integrity not compromised during:

- A shock of 50 g (± 10%) with velocity change of 170 inches/sec (± 10%) applied three times in each of the orthogonal axes.
- Vibration of 0.01 g^2 per Hz at 5 Hz, sloping to 0.02 g^2 per Hz at 20 Hz and maintaining 0.02 g^2 per Hz from 20 Hz to 500 Hz for 10 minute per axis applied in each of the orthogonal axes.

8.8 Electromagnetic Compatibility – PROPOSED

Design, including materials, should be consistent with the manufacture of units that comply with the limits of FCC Class B and CISPR22 Class B for radiated emissions.

8.9 Reliability – PROPOSED

Design, including materials, should be consistent with the manufacture of units with a Mean Time Between Failure (MTBF) of 500,000 hours of continuous operation at 55ºC, maximum-outputs load, and worst-case line, while meeting specified requirements. MTBF should be calculated in accordance with MIL-STD-217F or Bellcore.

8.10 Safety – PROPOSED

The voltage regulator is to be UL Recognized to standard UL1950 3rd Ed., including requirements of IEC950 and EN 60950. Plastic parts and printed wiring board are to be UL Recognized with 94V-0-flame class.

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9 Manufacturing Considerations

9.1 Lead Free (Pb Free)

The use of lead in electronic products is an environmental and political concern. The drivers for the reduction or elimination of lead in electronic products include:

- Customer desire for environmentally friendly (‘green’) products.
- Manufacturer desire to be environmentally friendly, and be perceived as such.
- Government initiatives regarding recycling of electronic products.
- Planned and potential legislation.

The most notable legislation is the European Union (EU) Restriction on Hazardous Materials directive, also known as RoHS. The commission directive may be found at the following URL:

http://europa.eu.int/eur-lex/pri/en/oj/dat/2003/l_037/l_03720030213en00190023.pdf

European Union “Member States demand that, starting from 1 July 2006, any new electrical and electronic equipment put on the market does not contain lead...” Each EU country will implement this law and establish penalties and fines for non-compliance. The RoHS directive includes certain exemptions:

- Lead in high melting temperature type solders (that is, tin-lead solder alloys containing more than 85% lead).
- Lead in solders for servers, storage and storage array systems (exemption granted until 2010).
- Lead in solders for network infrastructure equipment for switching, signaling, transmission as well as network management for telecommunication.
- Lead in electronic ceramic parts (for example, piezoelectronic devices).

For the latest information on RoHS please refer to the following URL:

http://europa.eu.int/eur-lex/en

Intel recommends to use the Pb Free manufacturing processes and components for the module and module connector.

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A Z(f) Constant Output Impedance Design

A.1 Introduction – PROPOSED

The VRM/EVRD performance specification is based on the concept of output impedance, commonly known as the load line. The impedance is determined by the Pulse Width Modulator (PWM) controller's Adaptive Voltage Positioning (AVP), up to the loop bandwidth of the regulator and the impedance of the output filter and socket beyond the loop bandwidth.

Figure A-1. Typical Intel® Microprocessor Voltage Regulator Validation Setup

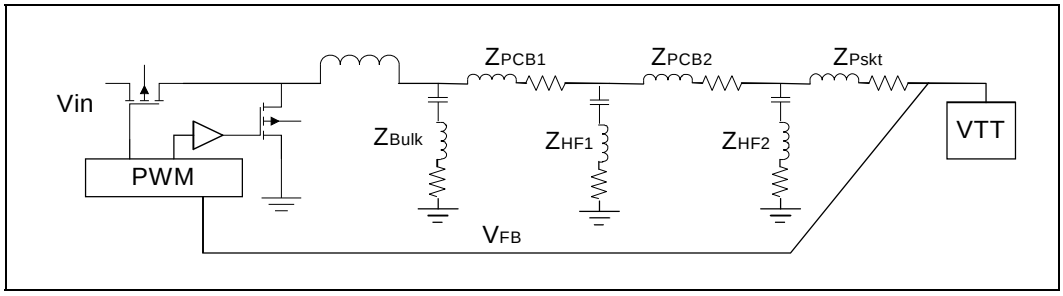
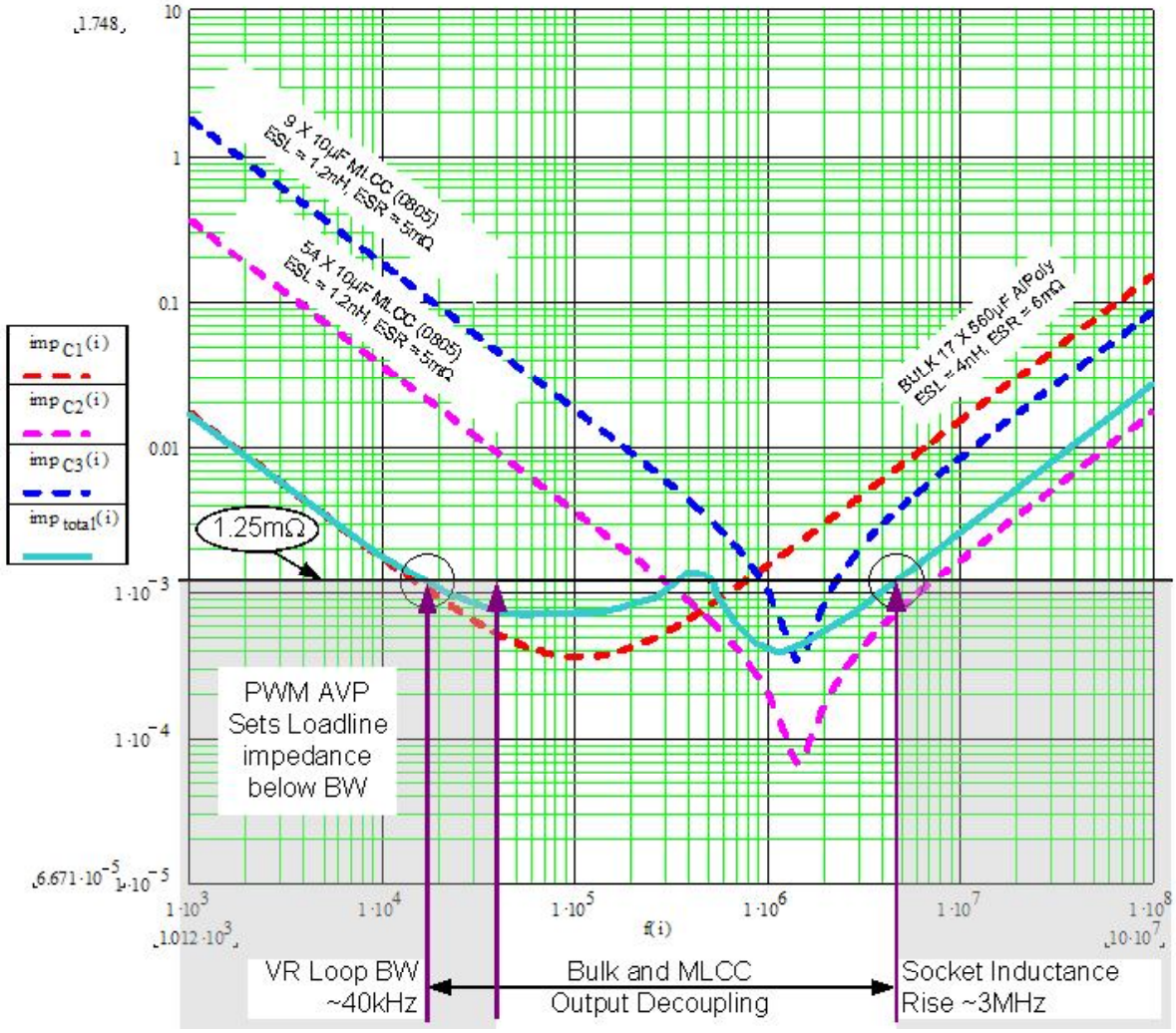


Figure A-2. Z(f) Network Plot with 0.8 mOhm Load Line - Example



The impedance plot Z(f) shown in Figure A-2 can be divided up into three major areas of interest.

- Low frequency, Zero Hz (DC) to the VR loop bandwidth. This is set by AVP and loop compensation of the VR controller or PWM control IC.
- Middle frequency, VR loop bandwidth to socket inductance rise. This is set by the bulk capacitors, MLCC capacitors and PCB layout parasitic elements.
- High frequency, controlled by socket inductance and the CPU package design.

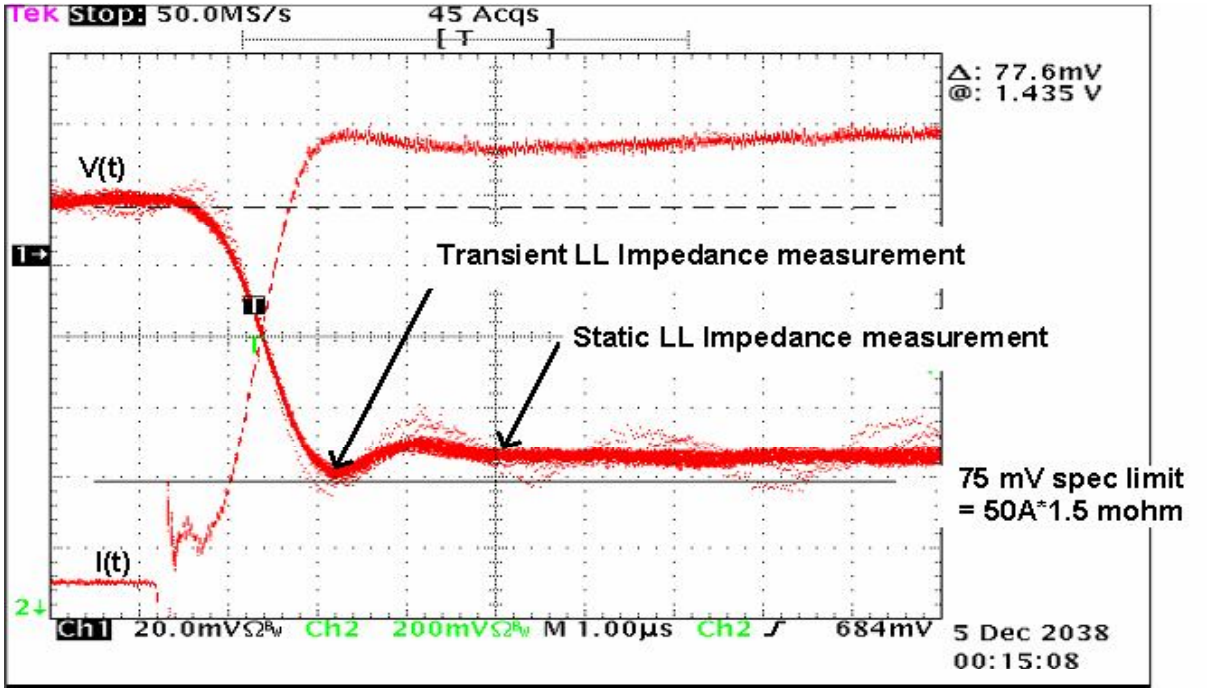
The VRM/EVRD designer has control of the low and mid frequency impedance design. By ensuring these areas meet the load line target impedance in Section 2.2, the system design will work properly with future CPU package designs.

Figure A-2 shows the impedance versus frequency network the system in Figure 2-1. This example consists of 17 560 µF with an ESR of 7 mΩ and ESL of 4 nH per bulk capacitors, 1st PCB impedance of 1.0 µΩ and 0.05 pH between the bulk and 45 10 µF 0805 MLCC, with ESR is 10 mΩ and ESL of 1.1 nH, 2nd PCB impedance of 1.0 µΩ and

0.05 pH between the 45 10 µF and the 9 10 µF 0805 MLCC in the socket cavity with ESR is 10 mΩ and ESL of 1.1 nH, and the LGA771 socket impedance of 330 µΩ and 20 pH. The resonant point seen at 400 kHz is due to the mis-match between the bulk capacitors and the MLCC cavity capacitors. Increasing the capacitance values will drop the magnitude and shift the to a lower resonance frequency. For example, if the 10 µF capacitors are increased to 22 µF, the resonant peak drops in magnitude to 1.0 mΩ and at a frequency of 200 kHz. The resonant peak could also be reduced by reducing the ESL of the bulk capacitors by changing capacitor technology or by adding more bulk capacitors in parallel. The effect of the mid frequency resonant point must be investigated and validated with Vdroop testing to ensure any current load transient pattern, does not violate the V_{min} load line.

By defining the output impedance load line over a frequency range, the voltage regulation or voltage droop is defined at any current level as the output current multiplied by the impedance value. Currently, output impedance is validated in the time domain by measuring the voltage response to a known current step. In Figure A-1, the VTT tool replaces the CPU and the package for platform validation purposes. Typical measured voltage and currents are depicted in Figure A-3. The transient load line is defined as the voltage droop magnitude during the current rise time divided by the current step. The static load line is defined as the voltage level magnitude, after settling, divided by the current step. It is desired to have both the transient and static load line equal.

Figure A-3. Time Domain Response of a Microprocessor Voltage Regulator



The static and transient load line measurements, measure the quality of different parts of the voltage regulator design. The transient load line is governed by the parasitic impedances in the output filter board layout, decoupling capacitors, and power distribution network. The static load line is governed by the PWM controller's AVP accuracy. The time domain Vdroop testing method gives pass, fail data on meeting the target specification, but gives little insight as to how to improve the voltage regulator's response. It can be difficult to determine if you need more bulk capacitance, more high

frequency MLCC capacitance or higher loop bandwidth from the time domain Vdroop waveforms. By measuring the impedance, Z(f) of the voltage regulator, these trade-offs and optimizations can be made.

The impedance can be measured with a network analyzer, but the network analyzer can only measure the passive filter components and will not show the effects of the VR loop bandwidth and AVP. Also MLCC capacitors impedance varies with DC bias and AC ripple frequency applied by the application. Hence a better method is needed to extract the impedance profile with the VR operating. The following sections introduce the theory behind using a VTT tool to create an impedance profile for the VR system.

A.2 Voltage Transient Tool (VTT) Z(f) Theory

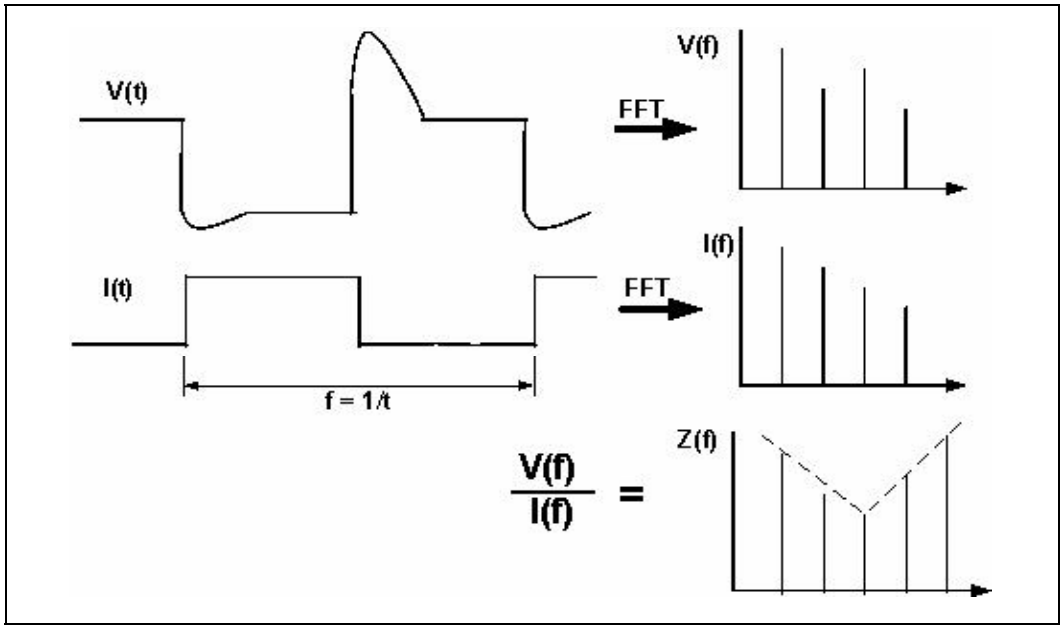
The following expression is the definition of impedance as a function of frequency looking back from the VTT tool into the filter network and VRM.

$$Z(f) = \frac{FFT(V(t))}{FFT(I(t))}$$

The representation of the corresponding Fourier spectra of the voltage and current responses are shown in Figure A-2. The first harmonic values from the Fast Fourier Transform (FFT) are used in the calculation of Z(f). The ratio of the two, yields the impedance at a given frequency, f. By sweeping the VTT generated load transient repetition rate, I(t), over the desired region of interest, additional points are estimated on the impedance profile to obtain a near continuous impedance spectrum plot.

In the VTT tool, the die voltage, V(t), is brought out through a pair of non-current carrying remote sense pins, tied to the Vcc and Vss power plane and measured on the VTT tool substrate. The current, I(t), is a differential voltage measured across the current shunt resistors in the VTT tool. The oscilloscope's math function is used to convert the time domain voltage droop and current measurements into their corresponding frequency domain spectrum. Since the FFT of the actual response waveforms are calculated, perfect square waves of current are not needed as a stimulus. The accuracy and frequency response of this method is limited to the current shunt resistor's accuracy and the shunt's parasitic inductance. Parasitic inductance in the current shunt resistors will over estimate the actual current and hence the method will under estimate the impedance at frequencies where the inductive voltage drop dominates the resistive voltage drop. The 50 pH of parasitic inductance in the VTT causes an over estimation of current for frequencies over 1 MHz and an under estimation of impedance. This can be corrected by post processing of the data and removing the inductive voltage spike.

Figure A-4. Time Domain Responses and Corresponding Fourier Spectra of Voltage, Current and Impedance



A.3 VTT Z(f) Measurement Method

An electronic load that has the capability to change the repetition rate up to 3 MHz of the load step is needed. The Intel LGA771/775V2 VTT by Cascade Systems Design, will meet this requirement. By monitoring the VTT current and voltage waveforms with an oscilloscope capable of executing an FFT on these waveforms, the platform impedance is found. A complete impedance profile is then generated by sweeping the input waveform frequency across the range of interest. In order to automate the data collection process, Intel has modified the VTT control software and a GPIB controlled oscilloscope is used along with software supplied with the VTT.

These utilities allow the user to automatically display and collect the magnitude and phase of the motherboard impedance in a Microsoft Excel* compatible data file. The total time it takes to extract the impedance profile using this method is about 1-2 minutes. This technique is very useful in investigating and assuring MB performance based on its stack up.

For more information on the measurement method and theory, see the paper *Microprocessor Platform Impedance Characterization using VTT Tools* by K. Aygun, S. Chickamenahalli, K. Eilert, M. Hill, K. Radhakrishnan and E. Stanford published at the IEEE Applied Power Electronics Conference, 2005.

A.4 Results

As an example, Figure A-5 shows the test platform with 10 560 µF Al-Poly bulk capacitors and 10 10 µF and 8 22 µF high frequency MLCC capacitors in the socket cavity. Figure A-6 is the measured impedance profile of the board shown in Figure A-5 as capacitors are removed. The VID setting for this measurement was 1.35 V and load

current was 40 A. The waveforms show the effect of capacitor depopulation on the impedance profile above 1 MHz as pairs of high frequency MLCC capacitors are removed (banks 1-9) per the bank designations depicted in Figure A-7.

Simulation comparisons are made in Figure A-8 for the two extreme cases of the decoupling conditions of Figure A-7, with all MLCC plus two Al-Poly bulk capacitors in place and all cavity MLCCs plus two Al-Poly bulk capacitors removed. Simulation depicts a 6-layer distributed motherboard model. The VR model has a Type III feedback compensated switching VR (swvr) and an average model (avgvr). It can be observed from Figure A-8 that the switching model measurements agrees better beyond the VR bandwidth (40 kHz) than the average model, while the average VR model performance agrees with the overall trend. Slightly lower average model impedances are also observed and other disagreements are attributed to imperfect assumptions about the parasitics of the devices and specific adaptive voltage implementation in the VR models.

Figure A-5. Photo of Motherboard Analyzed Showing High Frequency MLCC Capacitors in the Socket Cavity and Bulk Capacitors

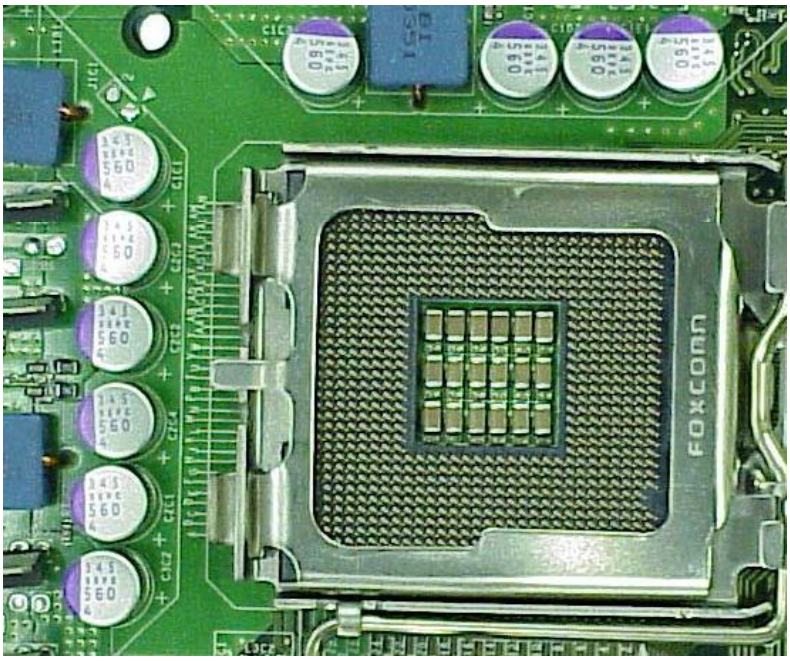


Figure A-6. Measured Platform Impedance Profile Showing Change in Impedance as Capacitors are Removed

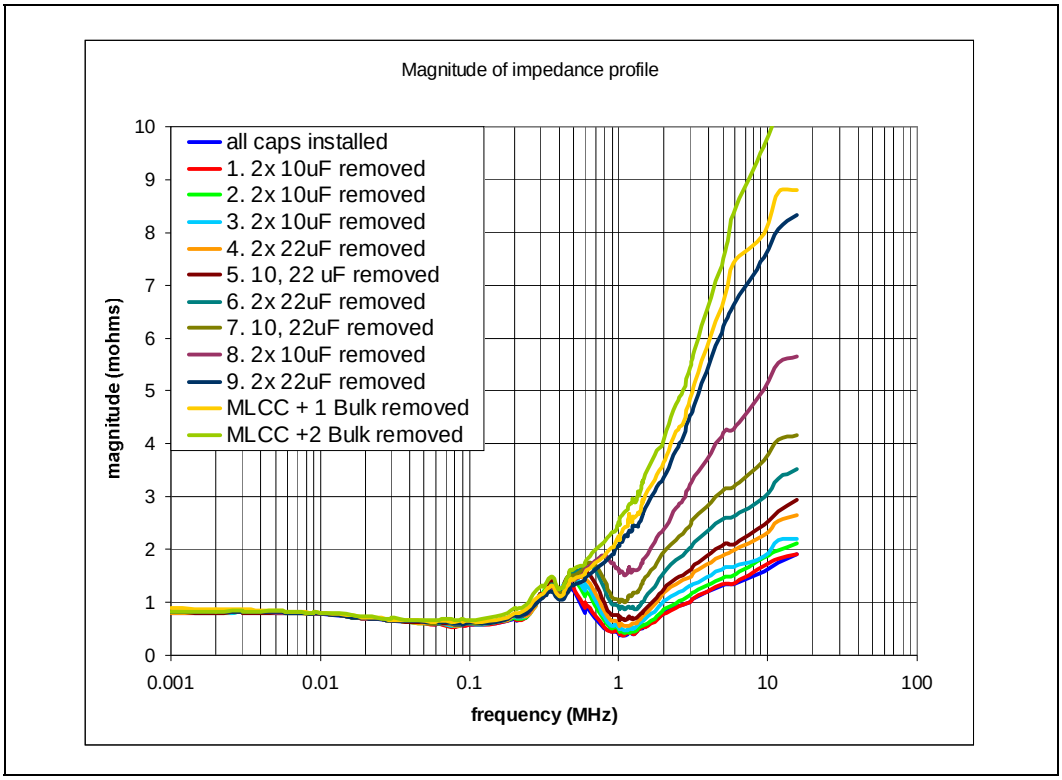


Figure A-7. Designations of MLCC Cavity Capacitor Banks

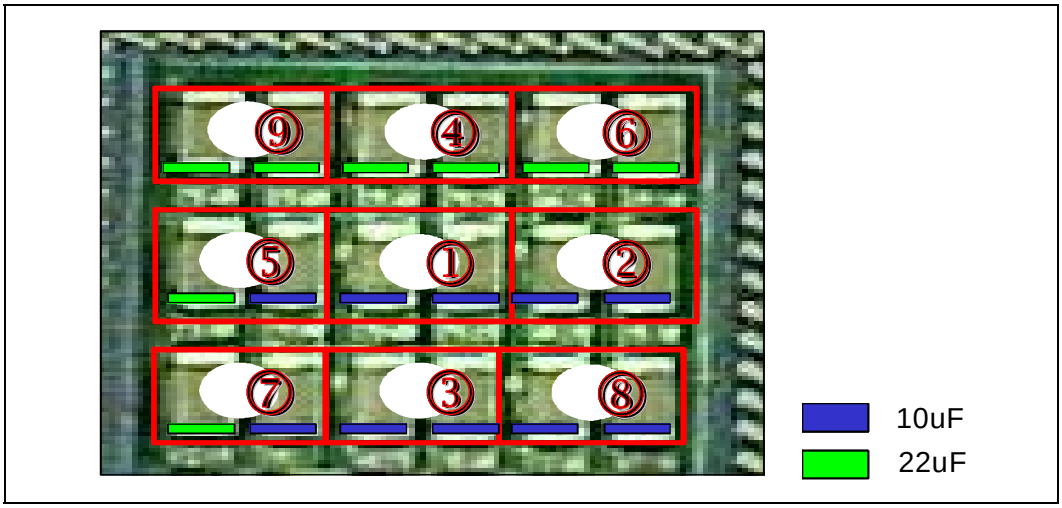
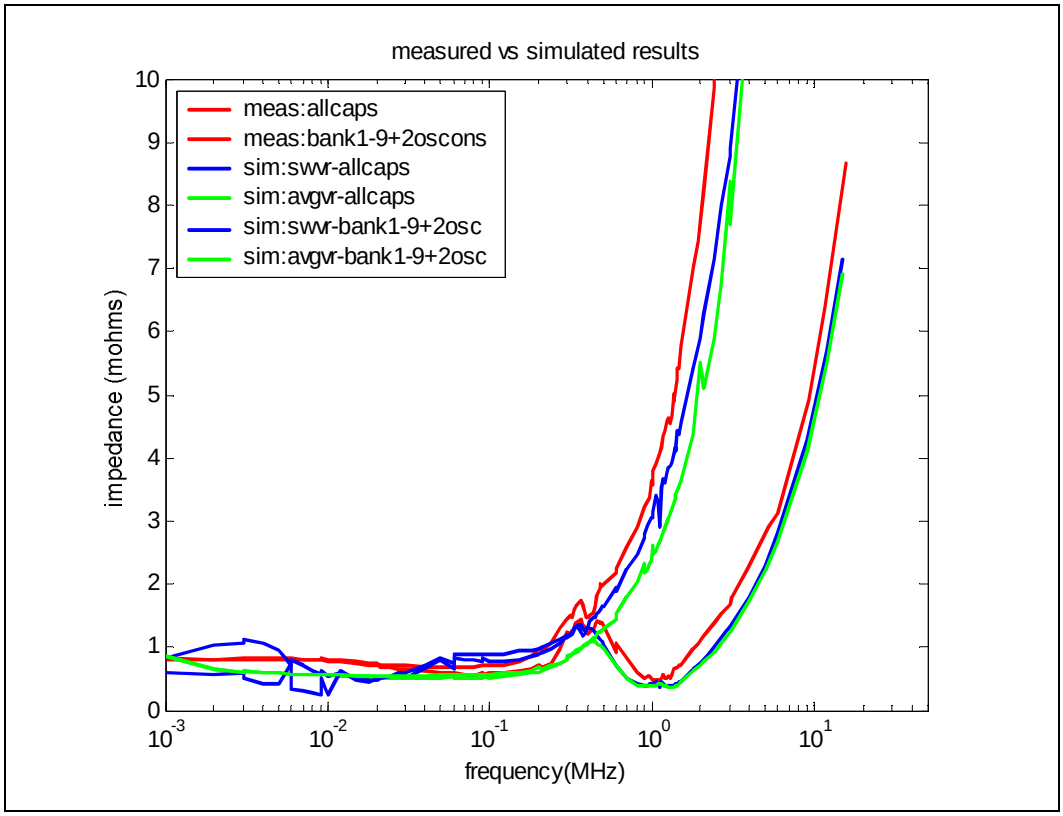


Figure A-8. Simulated and Measured Waveforms of Platform Impedance Profile



A.5 Output Decoupling Design Procedure

1. Select type and number of bulk capacitors. Normally the equivalent ESR needs to be approximately ½ the load line target impedance. For a 1.25 mΩ load line, the equivalent ESR should be less than 0.625 mΩ. The reason for selecting the number of bulk capacitors to yield an equivalent ESR to be ½ the target impedance is to compensate for the parasitic resistance of the PCB layout plane shapes and for aging of the capacitors. This is a starting point for the design. The final number of bulk capacitors will be determined by transient droop testing and Z(f) measurements.
2. The type and number of MLCC capacitors in the socket cavity is specified in the Section 2.11. These are required to meet both power delivery impedance and signal integrity issues.
3. Design the PWM loop bandwidth compensation. The ideal loop BW is set at the frequency where the bulk capacitor impedance meets the target impedance curve. In Figure A-2, it is approximately 30 kHz. Small increases in the loop bandwidth will not improve system performance until the bandwidth is moved to where the MLCC impedance meets the target impedance at ~ 700 kHz which is impractical.

Consult the PWM chip manufacturer's data sheets and application notes on calculating the PWM loop compensation and AVP programming values.

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