Intel® E7505 Chipset Memory Controller Hub (MCH)

Datasheet

December 2002

Document Number: 251932-002

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Revision History

Revision	Description	Date
-001	Initial Release	November 2002
-002	Addidtion of 1.3V MCH Core Voltage data Update I_{CC} requirments for 1.2 V and 1.3V MCH Core Voltage	December 2002

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Intel® E7505 Chipset MCH Features

- Processor/Host Bus Support
  - Symmetric Multiprocessing Protocol (SMP) for up to two processors
  - 533 MHz or 400 MHz (2x address, 4x data)
  - System Bus Dynamic Bus Inversion (DBI)
  - 36-bit host bus addressing
  - 12-deep in-order queue
  - 2-deep defer queue (only one per HI)
  - AGTL+ bus driver technology with on-die termination resistors
  - Parity protection on host bus Data, Address/ Request, and Response signals
- Memory System
  - Dual Channel (144-bits wide) DDR memory interface
  - DDR200 (PC1600) and DDR266 (PC2100) operation
  - Synchronous operation with processor system bus (same clock frequency required on both)
  - 128-Mb, 256-Mb, 512-Mb, 1-Gb DRAM densities
  - Maximum system memory is 16 GB
  - x64 or x72 DIMMs using x4, x8, or x16 DRAM devices (x4 registered only, x16 unbuffered only) Note: Double-sided x16 is not supported
  - Based on three DIMMs - 24 simultaneous open pages (4 per row)
  - Non-ECC mode (64-bit DIMMs)
  - Registered or unbuffered DIMMs
  - DIMMs must be populated in identical pairs for dual channel operation
  - Intel® x4 Single Device Data Correction (x4 SDDC) technology ECC supported
    - Corrects any number of errors contained in 4-bit naturally aligned nibbles
    - Detects all errors contained entirely within two 4-bit naturally aligned nibbles
  - Opportunistic DRAM refresh
- Accelerated Graphics Port (AGP)
  - AGP Specification 3.0
  - Single AGP device
  - AGP interface asynchronously coupled to core
  - AGP 8x / 4x (0.8 V swing) and 4x, 2x, 1x (1.5 V swing)
  - No 3.3 V support
  - 32 deep AGP request queue
  - 32-bit upstream address support for inbound AGP and PCI cycles
  - 32-bit downstream address support for outbound PCI and Fast Write cycles
  - AGP address translation mechanism with two integrated fully associative 20 entry TLBs
  - AGP register set in both Device 0 and Device 1
- Hub Interface_A to Intel® ICH4
  - Connection to ICH4 via HI1.5 (HI1.0 protocol and data rate, HI2.0 electrical characteristics)
  - 8-bit interface
  - 266 MT/s point-to-point HI1.5 interface to ICH4 with parity
  - 66 MHz base clock
  - All HI IB accesses are snooped
  - Isochronous support
  - Parallel termination mode only
  - Asynchronously coupled to core
  - 64-bit addressing on IB transactions (maximum 16-GB memory decode space [1])
  - 32-bit OB addressing
  - Supports the following traffic types to ICH4: HI-to-AGP memory writes, HI-to-DRAM, Processor-to-HI, Messaging
  - MSI Interrupt messages
  - Power Management state change
  - SMI, SCI and SERR error indication
- Hub Interface_B
  - HI2.0 protocols and electrical characteristics
  - Independent 1 GB/s point-to-point 16-bit connection
  - ECC protection
  - 66 MHz base clock running 8x (1 GB/s) data transfers
  - Snooped and non-snooped IB accesses
  - Asynchronously coupled to core
  - Parallel termination mode only
  - 64-bit IB addressing
  - 32-bit OB addressing for PCI-X
  - Supports the following traffic types to ICH4: HI_B to AGP/PCI_B memory writes, HI_B to DRAM (memory reads and writes), CPU to HI_B (memory reads or writes, I/O reads or writes), MSIs between HI_A, Messaging
  - MSI interrupt messages
  - EOI Message
- PCI Support
  - 33 MHz PCI on ICH4
  - 33 MHz and 66 MHz PCI on P64H2
  - 66 MHz, 100 MHz, or 133 MHz for PCI-X on P64H2
- Power Management Support
  - SMRAM space remapping to A0000h (128 KB)
  - Extended SMRAM space above 256 MB
  - SMRAM accesses from TSEG, AGP or HIs are not allowed
  - PC'99 Suspend to RAM (STR)
  - ACPI Rev 2.0 compliant power management
  - NT Hardware Design Guide v1.0 compliant
  - APM Rev 1.2 compliant power management
  - C0, C1, S0, S1 (DT), and S3
- Package
  - 1005 Ballout

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Introduction 1

The Intel® E7505 chipset is a high-performance chipset designed as the next generation workstation. The main components of the chipset are the Memory Controller Hub (MCH) host bridge and the Intel® 82801BA I/O Controller Hub 4 (ICH4) for the I/O subsystem. A supporting component for the platform is the Intel® 82870P2 PCI-64 Hub 2 (P64H2) for I/O expansion.

The MCH is supports the Intel® Xeon™ processor with 512-KB L2 cache and the Intel® Xeon™ processor with 533 MHz system bus in dual-processor mode. Four-way processor mode is not supported by the MCH. The MCH supports up to 16 GB of Double Data Rate (DDR) SDRAM system memory and provides the next generation AGP 8x graphics port.

This document describes the E7505 chipset MCH. The MCH signals, registers, DC electrical characteristics, ballout, package dimensions, and component testability are covered. The major functional blocks of the MCH are described. For detailed descriptions of other chipset components, refer to the respective component's datasheet.

1.1 Terminology

Term	Description
MCH	The Memory Controller Hub component contains the processor interface and system memory interface. The MCH communicates with the I/O Controller Hub 4 (ICH4) and other controller hubs over a proprietary interconnect called the Hub Interface.
HI	The Hub Interface interconnects the MCH to the hub components (ICH4 or P64H2). In this document HI cycles originating from or destined for the primary PCI interface on the ICH4 are generally referred to as HI/PCI_A or simply HI_A cycles. Cycles originating from or destined for any target on the second HI interface is described as HI_B cycles. **NOTE:** There are two versions of HI used on the MCH. An 8-bit HI1.5 protocol is implemented on HI_A and a 16-bit HI2.0 protocol is implemented for the HI_B.
Host	This term is used synonymously with processor.
IB	Inbound, refers to traffic moving from PCI or other I/O toward DRAM or the system bus.
Intel® ICH4	The I/O Controller Hub 4 component contains the primary PCI interface, LPC interface, USB 2.0, ATA-100 and other legacy functions. The ICH4 communicates with the MCH over a proprietary interconnect called the Hub Interface, (HI1.5).
Intel® Xeon® Processor with 512-KB L2 Cache	The MCH supports dual processors on a single 400 MHz system bus.
Intel® Xeon® Processor with 533 MHz System Bus	The MCH supports dual processors on a single 533 MHz system bus.
OB	Outbound, refers to traffic moving from the system bus to PCI or other I/O.

Term	Description
MCH	The Memory Controller Hub component contains the processor interface and system memory interface. The MCH communicates with the I/O Controller Hub 4 (ICH4) and other controller hubs over a proprietary interconnect called the Hub Interface.
Intel® P64H2	The PCI-64 Hub 2 component adds PCI-X functionality to the chipset.The P64H2 connects to the MCH over a proprietary interconnect called the Hub Interface 2.0. The P64H2 can be configured as two 64-bit 100 MHz PCI-X interfaces or a single 64-bit 133 MHz PCI-X interface.
Power Good Reset	All MCH is reset, including sticky registers. This state looks like initial power on.
Primary PCI or PCI_A	The physical PCI bus is driven directly by the ICH4 component. The PCI_A bus supports up to six PCI 2.2 compliant components which operate at 5 V, 32-bit, and 33 MHz. Communication between PCI_A and the MCH occurs over HI_A. **NOTE:** The Primary PCI bus is referred to as PCI_A is **not** PCI Bus #0 from a configuration standpoint.
SB	The processor system bus operates at either 133 MHz or 100 MHz system bus clock.
SDDC	Intel® x4 Single Device Data Correction (x4 SDDC). In a x4 DDR memory device, SDDC provides error detection and correction for 1, 2, 3, or 4 data bits within that single device and provides error detection, up to 8 data bits, within two devices.
SEC-DED	Single Error Correct-Double Error Detect system memory error correction circuitry supported by the MCH.
System Reset	Also called reset, the MCH logic is reset except for certain sticky registers.

1.2 Reference Documents

Title	Document/Location
Intel® Xeon™ Processor and Intel® E7505 Chipset Platform Design Guide	251934
Intel® 82801BA I/O Controller Hub 4 (ICH4) Datasheet	290744
Intel® 82870P2 PCI/PCI-X 64 Bit Hub 2 (P64H2) Datasheet	290732
Intel® E7505 Chipset Memory Controller Hub Specification Update	251933 / http://developer.intel.com/design/chipsets/e7505/
Intel® NetBurst™ Microarchitecture BIOS Writer's Guide	Note 1
Intel® E7500/E7505 Chipset Memory Controller Hub (MCH) Thermal Design Guidelines	298647
CK408 Clock Synthesizer/Driver Specification	Note 1
Accelerated Graphics Port Interface Specification, Revision 3.0	http://www.agpforum.org/
Low Pin Count Interface Specification, Revision 1.0	http://developer.intel.com/design/chipsets/industry/lpc.htm
PCI Local Bus Specification, Revision 2.2	http://www.pcisig.com/
PCI-PCI Bridge Specification, Revision 1.0	http://www.pcisig.com/
PCI Bus Power Management Interface Specification, Revision 1.0	http://www.pcisig.com/
Universal Serial Bus 2.0 Specification	http://www.usb.org/
Advance Configuration and Power Interface (ACPI) Specification	http://www.teleport.com/~acpi/

NOTES:
1. Contact your local Intel representative for the latest revision and document number for this document.
2. Refer to the *Intel® Xeon™ Processor and Intel® E7505 Chipset Platform Design Guide* for an expanded set of reference documents.

1.3 Intel® E7505 Chipset System Architecture

The Intel® E7505 chipset is optimized for the Intel® Xeon™ processor with 512 KB L2 cache. The architecture of the chipset provides the performance and feature-set required for dual-processor based workstations in the volume and performance market segments. The MCH supports AGP 8x with backwards compatibility to AGP 4x. The AGP interface is fully compliant with the *AGP Specification 3.0*. The system bus, used to connect the processor with the Intel® E7505 chipset, utilizes a 400 MHz/533 MHz transfer rate for data transfers, delivering a bandwidth of 4.27 GB/s. The Intel® E7505 chipset architecture supports a 144-bit wide, 266 MHz Double Data Rate (DDR) memory interface also capable of transferring data at 4.27 GB/s (see Table 1-1). The memory interface supports dual channel DDR system memory with registered or unbuffered SDRAM DIMMs. The hub interface 2.0 (HI2.0), a chipset component interconnect, is designed into the Intel® E7505 chipset to provide more efficient communication between chipset components for high-speed I/O. The HI2.0 connection provides 1.066 GB/s I/O bandwidth and can be used for PCI-X via the P64H2 hub component.

Table 1-1. Supported Memory Modes

SB MT/s	SB Clock MHz	SB BW	DDR MT/s	DDR Clock MHz	DDR BW
533	133	4.3 GB/sec	266	133	4.3 GB/sec
400	100	3.2 GB/sec	200	100	3.2 GB/sec

Table 1-2. DIMM Support

Type	Unbuffered	Registered
Dual Channel	1 to 2 pair DIMMs (4 rows)	1 to 3 pair DIMMs (6 rows max)

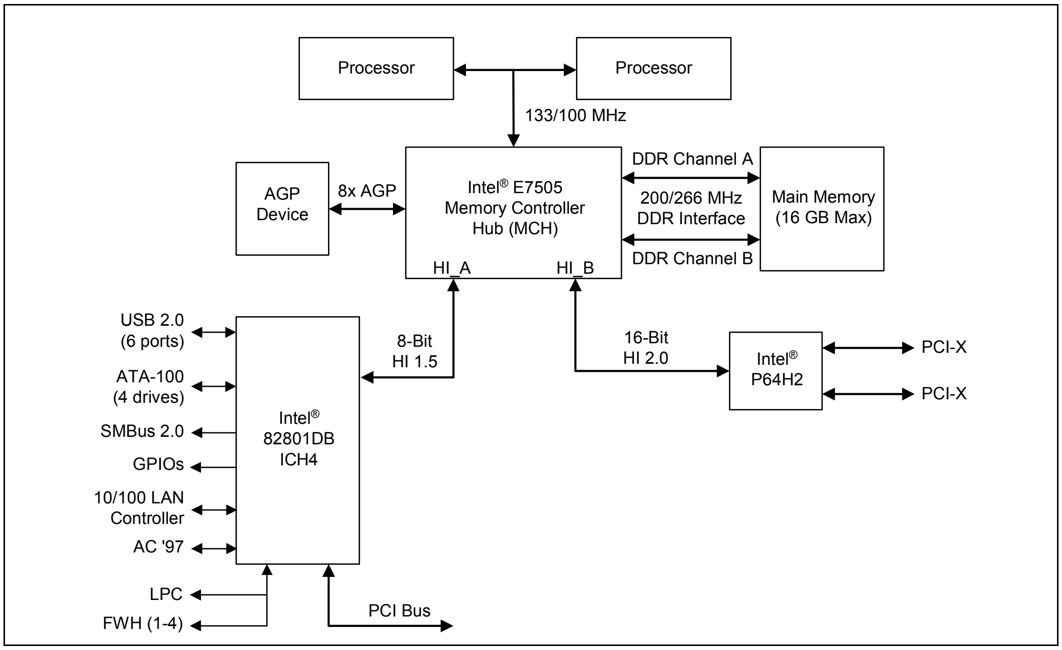
In addition to these performance features, Intel® E7505 chipset-based platforms also provide the RAS (Reliability, Availability, Serviceability) features required for volume and performance workstations. These features include: Intel® x4 Single Device Data Correction (x4 SDDC) technology ECC for memory, ECC for all high-performance I/O, SMBus interface, and processor thermal monitoring.

The Intel® E7505 chipset consists of three major components: the Memory Controller Hub (MCH), the I/O Controller Hub 4 (ICH4), and the PCI/PCI-X 64-bit Hub 2.0 (P64H2). The MCH's I/O interfaces consists of both a HI2.0 and a HI1.5 interface. The chipset components communicate via hub interfaces (HIs). The MCH provides two hub interface connections: one for the ICH4 and one for high-speed I/O using a P64H2 bridge. The P64H2 provides bridging functions between HI_B and the PCI / PCI-X bus.

Additional platform features supported by the Intel® E7505 chipset include four ATA/100 IDE drives, Low Pin Count interface (LPC), integrated LAN Controller, Audio Codec, and Universal Serial Bus (USB).

The Intel® E7505 chipset is also ACPI compliant and supports Full-on, Stop Grant, Suspend to Disk, and Soft-off power management states. Through the use of an appropriate LAN device, the Intel® E7505 chipset also supports wake-on-LAN* for remote administration and troubleshooting.

Figure 1-1. Dual-Processor System Block Diagram



Signal Description 2

This chapter provides a detailed description of MCH signals. The signals are arranged in functional groups according to their associated interface.

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at a high voltage level.

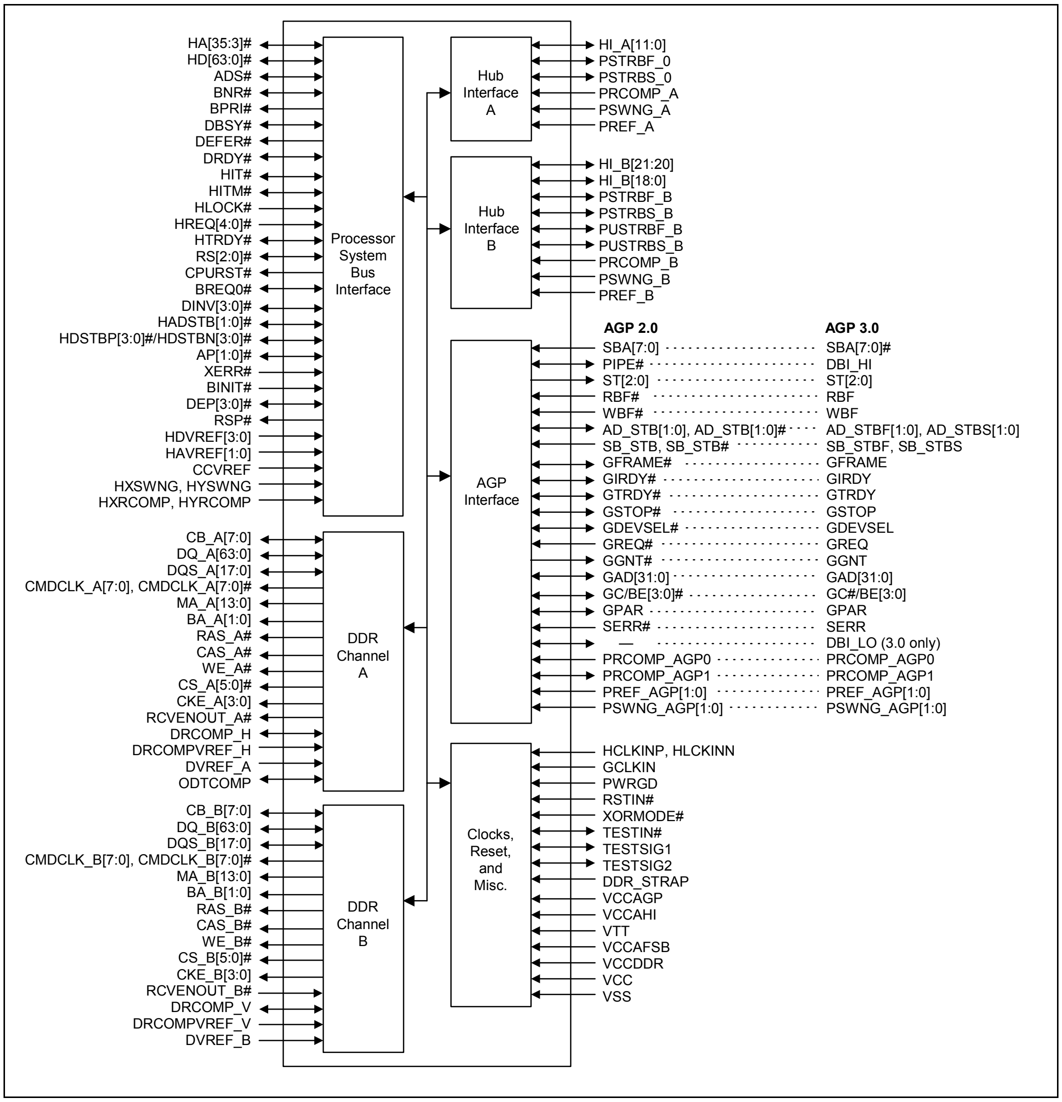
The following notations are used to describe the signal type:

I	Input pin
O	Output pin
I/O	Bidirectional Input/Output pin.
s/t/s	Sustained tri-state. This pin is driven to its inactive state prior to tri-stating.
as/t/s	Active Sustained tri-state. This applies to some of the hub interface signals. This pin is weakly driven to its last driven value.
2x	Double-pump clocking. Addressing at 2x of HCLK
4x	Quad-pump clocking. Data transfer at 4x of HCLK

The signal description also includes the type of buffer used for the particular signal:

AGTL+	The processor's system buses use a technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to assist the pull-up resistors during the first clock of a low-to-high voltage transition.
Asynchronous AGTL+	Intel Xeon processors with 533 MHz Sysytem Bus and with 512-KB L2 cache do not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output FERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to HCLKINx. However, all of the asynchronous GTL+ signals are required to be asserted for at least two HCLKINx in order for the processor to recognize them.
CMOS	CMOS buffers. System bus address and data bus signals are logically inverted signals. The logical values are the inversion of the electrical values on the system bus. A signal "#" indicates an active low, and with no "#" indicates an active high.
AGP	AGP interface signals. These signals are compatible with AGP 2.0 (1.5 V) signaling and AGP 3.0 (0.8 V) Signaling Environment Specifications (AC and DC). These buffers are not 3.3 V tolerant.
SSTL-2	Stub Series Terminated Logic for 2.5 V (DDR interface).
HI2 Buffer	Hub Interface buffer types

Figure 2-1. MCH Interface Signals



2.1 Host Interface Signals

Table 2-1. Host Interface Signals (Sheet 1 of 3)

Signal Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe:** The system bus owner asserts ADS# to indicate the first of two cycles of a request phase.
AP[1:0]#	I/O AGTL+	**Address Parity:** The AP[1:0]# lines are driven by the request initiator and provide parity protection for the Request Phase signals. AP[1:0]# are common clock signals and are driven one common clock after the Request Phase. Address parity is correct if there are an even number of electrically low signals (low voltage) in the set consisting of the covered signals plus the parity signal. Note that the MCH only connects to HA[35:3]#. The MCH may be configured to send an error message to the Intel® ICH4 over HI_A when it detects an error on one of the AP[1:0]# signals.
XERR#	I AGTL+	**Bus Error:** This signal can be connected to the MCERR# signal or IERR# signal, depending on system usage. The MCH detects an electrical high-to-low transition on this input signal and sets the correct error bit. The MCH will take no other action except setting that bit.
BINIT#	I AGTL+	**Bus Initialize:** This signal indicates an unrecoverable error and can be driven by the processor.It is latched by the MCH.
BNR#	I/O AGTL+	**Block Next Request:** This signal is used to block the current request bus owner from issuing a new requests. This signal is used to dynamically control the system bus pipeline depth.
BPRI#	O AGTL+	**Priority Agent Bus Request:** The MCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. The MCH has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted.
BREQ0#	I/O AGTL+	**Bus Request 0#:** The MCH pulls the processor bus, BREQ0# signal low during CPURST#. The signal is sampled by the processors on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 HCLKs and the maximum hold time is 20 HCLKs. BREQ0# should be Tristate after the hold time requirement has been satisfied.
CPURST#	O AGTL+	**CPU Reset:** The CPURST# pin is an output from the MCH. The MCH asserts CPURST# while RSTIN# (PCIRST# from ICH4) is asserted and for approximately 1 ms after RSTIN# is deasserted. The CPURST# allows the processors to begin execution in a known state.
DBSY#	I/O AGTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	**Defer:** This signal, when asserted, indicates that the MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
DEP[3:0]#	I/O AGTL+	**Host Data Parity:** The DEP[3:0]# signals provide parity protection for HD[63:0]#. The DEP[3:0]# signals are common clock signals and are driven one common clock after the data phases they cover. DEP[3:0]# are driven by the same agent driving HD[63:0]#. Data parity is correct if there are an even number of electrically low signals (low voltage) in the set consisting of the covered signals plus the parity signal.
DINV[3:0]#	I/O AGTL+ 4x	**Dynamic Bus Inversion:** These signals are driven along with the HD[63:0]# signals. They indicate when the associated signals are inverted. DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16 bit group never exceeds 8.

Table 2-1. Host Interface Signals (Sheet 2 of 3)

Signal Name	Type	Description
DRDY#	I/O AGTL+	**Data Ready:** This signal is asserted for each cycle that data is transferred.
HA[35:3]#	I/O GTL+ 2x	**Host Address Bus:** HA[35:3]# connect to the system address bus. During processor cycles, HA[35:3]# are inputs. The MCH drives HA[35:3]# during snoop cycles on behalf of HI initiators. HA[35:3] are transferred at 2x rate.
HADSTB[1:0]#	I/O AGTL+ 2x	**Host Address Strobe:** The source synchronous strobes are used to transfer HA[35:3]# and HREQ[4:0]# at the 2x transfer rate.
HD[63:0]#	I/O AGTL+ 4x	**Host Data:** These signals are connected to the system data bus. HD[63:0]# are transferred at the 4x rate.
HDSTBP[3:0]#, HDSTBN[3:0]#	I/O AGTL+ 4x	**Differential Host Data Strobes:** The differential source synchronous strobes are used to transfer HD[63:0]# and DINV[3:0]# at the 4x transfer rate. **Strobe** — **Data Bits** HDSTBP3#, HDSTBN3# — HD[63:48]#, DINV3# HDSTBP2#, HDSTBN2# — HD[47:32]#, DINV2# HDSTBP1#, HDSTBN1# — HD[31:16]#, DINV1# HDSTBP0#, HDSTBN0# — HD[15:0]#, DINV0#
HIT#	I/O AGTL+	**Hit:** This signal indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. HITM# is driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I AGTL+	**Host Lock:** All system bus cycles are sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK#. Must be atomic, i.e., no Hub Interface or AGP snoopable access to DRAM are allowed when HLOCK# is asserted by the processor.
HREQ[4:0]#	I/O AGTL+ 2x	**Host Request Command:** These signals define the attributes of the request. In Enhanced Mode HREQ[4:0]# are transferred at the 2x rate. The request is asserted by the requesting agent during both halves of a Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.
HTRDY#	O AGTL+	**Host Target Ready:** This signal indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	O AGTL+	**Response Signals:** The RS[2:0]# signals indicate the type of response according to the following: 000 = Idle state 001 = Retry response 010 = Deferred response 011 = Reserved (not driven by MCH) 100 = Hard Failure (not driven by MCH) 101 = No data response 110 = Implicit Writeback 111 = Normal data response
RSP#	O AGTL+	**Response Parity:** RSP# provides parity protection for the RS[2:0]# signals. RSP# is always driven by the MCH and must be valid on all clocks. Response parity is correct when there are an even number of low signals (low voltage) in the set consisting of the RS[2:0]# signals and the RSP# signal itself.

Table 2-1. Host Interface Signals (Sheet 3 of 3)

Signal Name	Type	Description
HXRCOMP, HYRCOMP	I/O GTL+	**Host RCOMP:** These signals are used to calibrate the Host GTL+ I/O buffers. Since the Host GTL+ IO buffers cover two sides of the die, HXRCOMP is for the signals on one side of the die, and HYRCOMP handles signals on the other side of the die.
HXSWNG, HYSWNG	I Analog	**Host Voltage Swing:** These signals provide a reference voltage used by the SB RCOMP circuit. HXSWNG is used for the signals handled by HXRCOMP, and HYSWNG is used for the signals handled by HYRCOMP
HDVREF[3:0]	I Analog	**Host Data Reference Voltage:** Reference voltage input for the 4x data signals of the Host GTL interface.
HAVREF[1:0]	I Analog	**Host Address Reference Voltage:** Reference voltage input for the 2x address signals of the Host GTL interface.
CCVREF	I Analog	**Host Common Clock Reference Voltage:** Reference voltage input for the common clock signals of the Host GTL interface.

2.2 DDR Channel A Signals

Table 2-2. DDR Channel A Signals (Sheet 1 of 3)

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>CB_A[7:0]</td><td>I/O
SSTL-2</td><td>ECC Data bits: These signals are the 8-bit ECC data, running at 2x data rate. The data is source synchronous using the DQS strobes.</td></tr>
<tr><td>DQ_A[63:0]</td><td>I/O
SSTL-2</td><td>Data: These signals are the 64-bit data bus, running at 2x data rate. The data is source synchronous using the DQS strobes.</td></tr>
<tr><td>DQS_A[17:0]</td><td>I/O
SSTL-2</td><td>Data Strobes: These signals provide the timing information for the data and ECC bits. They are driven by the source of the data. Nine signals are required for x8 and x16 RAMs; eighteen are required for x4 RAMs. When accessing x8 or x16 DRAM rows, DQS_A[17:9] are driven low during write cycles since these pins will be connected to the DM (data mask) inputs of the DRAMs on the DIMM.</td></tr>
<tr><td>CMDCLK_A[7:0]</td><td>O
CMOS</td><td>Differential Clock: These signals are outputs to the DIMMs. Commands are referenced to the rising edge of CMDCLK_x and the falling edge of CMDCLK_x#; one per DIMM for registered DIMMs, 3 per DIMM for unbuffered DIMMs.
The mapping is shown in the following table:
• CK0/CK0# are at pins 137 and 138 of the DIMM.
• CK1/CK1# are at pins 16 and 17 of the DIMM.
• CMDCLK_A6 is multiplexed with CS_A5#.
<table>
<tr><th>Signal</th><th>2 DIMM</th><th>3 DIMM</th></tr>
<tr><td>CMDCLK_A7</td><td>DIMM 1 CK2</td><td></td></tr>
<tr><td>CMDCLK_A6/CS_A5#</td><td>DIMM 0 CK2</td><td></td></tr>
<tr><td>CMDCLK_A5</td><td>DIMM 1 CK1</td><td></td></tr>
<tr><td>CMDCLK_A4</td><td>DIMM 0 CK1</td><td></td></tr>
<tr><td>CMDCLK_A3</td><td></td><td></td></tr>
<tr><td>CMDCLK_A2</td><td></td><td>DIMM 2 CK0</td></tr>
<tr><td>CMDCLK_A1</td><td>DIMM 1 CK0</td><td>DIMM 1 CK0</td></tr>
<tr><td>CMDCLK_A0</td><td>DIMM 0 CK0</td><td>DIMM 0 CK0</td></tr>
</table></td></tr>
<tr><td>CMDCLK_A[7:0]#</td><td>O
CMOS</td><td>Differential Clock: These signals are outputs to the DIMMs. Commands are referenced to the rising edge of CMDCLK_x and the falling edge of CMDCLK_x#; one per DIMM for registered DIMMs, 3 per DIMM for unbuffered DIMMs.
• CMDCLK_A6# is multiplexed with CS_A4#.
<table>
<tr><th>Signal</th><th>2 DIMM</th><th>3 DIMM</th></tr>
<tr><td>CMDCLK_A7#</td><td>DIMM 1 CK2#</td><td></td></tr>
<tr><td>CMDCLK_A6#/CS_A4#</td><td>DIMM 0 CK2#</td><td></td></tr>
<tr><td>CMDCLK_A5#</td><td>DIMM 1 CK1#</td><td></td></tr>
<tr><td>CMDCLK_A4#</td><td>DIMM 0 CK1#</td><td></td></tr>
<tr><td>CMDCLK_A3#</td><td></td><td></td></tr>
<tr><td>CMDCLK_A2#</td><td></td><td>DIMM 2 CK0#</td></tr>
<tr><td>CMDCLK_A1#</td><td>DIMM 1 CK0#</td><td>DIMM 1 CK0#</td></tr>
<tr><td>CMDCLK_A0#</td><td>DIMM 0 CK0#</td><td>DIMM 0 CK0#</td></tr>
</table></td></tr>
</table>

Table 2-2. DDR Channel A Signals (Sheet 2 of 3)

Signal Name	Type	Description
CS_A[5:0]#	O SSTL-2	**Chip Select:** The chip select inputs determine which row a command is targeting. There is one per row (2 per DIMM). **Multiplexed Chip Selects and clocks:** These signals are chip select outputs on a three-DIMM motherboard supporting registered DIMMs only, and clock outputs on a two DIMM motherboard which supports unbuffered or registered DIMMs. A configuration bit determines their function. The default function is chip selects. • CK2/CK2# are at pins 76 and 75 of the DIMM. **Signal** / **2 DIMM** / **3 DIMM** CS_A5#/CMDCLK_A6 / — / DIMM 2 S1# CS_A4#/CMDCLK_A6# / — / DIMM 2 S0# CS_A3# / DIMM 1 S1# / DIMM 1 S1# CS_A2# / DIMM 1 S0# / DIMM 1 S0# CS_A1# / DIMM 0 S1# / DIMM 0 S1# CS_A0# / DIMM 0 S0# / DIMM 0 S0#
MA_A[13:0]	O SSTL-2	**Memory Address:** These signals provide the row address for ACTIVE commands, and the column address and auto-precharge bit for read/write commands, to select one location out of the memory array in the respective bank. MA_A10 is sampled during a precharge command to determine whether the precharge applies to one bank (MA_A10 low) or all banks (MA_A10 high). If only one bank is to be Precharge, the bank is selected by BA_A0, BA_A1. The address inputs also provide the opcode during a Mode Register Set command. BA_A0 and BA_A1 define which mode register is loaded during the Mode Register Set command (MRS or EMRS).
BA_A[1:0]	O SSTL-2	**Bank Address:** The Bank Address specifies which bank that an activate, read, write, or precharge command is targeting.
RAS_A#	O SSTL-2	**Row Address Strobe:** This signal is used to indicate an activate command, opening a page specified by the MA signals in the bank specified by the BA_x signals. Used with WE_A# to indicate a precharge command, closing the page in the bank specified by the BA_x signals. RAS_A# is also used to enter register set mode or start an auto refresh or enter self refresh.
CAS_A#	O SSTL-2	**Column Address Strobe:** This signal is used to indicate a read or write command to the open page in the bank specified by the BA_x signals. CAS_A# is also used to enter register set mode or start an auto refresh or enter self refresh.
WE_A#	O SSTL-2	**Write Enable:** This signal is used to differentiate a read from a write command when CAS_A# is active and RAS_A# is inactive. it is used to differentiate an activate command when RAS_A# is active and CAS_A# in inactive. WE_A# is also used to terminate a burst, enter register set mode.

Table 2-2. DDR Channel A Signals (Sheet 3 of 3)

Signal Name	Type	Description
CKE_A[3:0]	O SSTL-2	**Clock Enable:** CKE_x high activates, and CKE_x low deactivates the internal clock signals, and device input buffers and output drivers. Driving CKE_x low provides precharge powerdown and self refresh operation (all banks idle), or Active Powerdown (row active in any bank). CKE_x is synchronous for powerdown entry and exit, and for self refresh entry. CKE_x is asynchronous for Self Refresh exit, and for output disable. Input buffers, excluding CK, CK#, and CKE_x are disabled during powerdown. Input buffers, excluding CKEx are disabled during self refresh. The CKE signals are driven low when the RSTIN# signal is low to keep the DRAMs in self refresh mode. Registered: One for even rows, one for odd rows. Unbuffered: One per row. **Signal** / **2 DIMM MB** / **3 DIMM MB** CKE_A3 / DIMM 1 CKE1 / CKE_A2 / DIMM 1 CKE0 / CKE_A1 / DIMM 0 CKE1 / All DIMMs CKE1 CKE_A0 / DIMM 0 CKE0 / All DIMMs CKE0
RCVENOUT_A#	O SSTL-2	**Receive Enable Output:** This signal is driven low and fed back internally when the DQ bus is to receive data (DRAM reads). It is used to set the timing for enabling the DQS input buffers so that they are enabled only when driven by the DRAMs. This signal must be terminated externally.
DVREF_A	I Analog	**Voltage Reference**
DRCOMP_H	I/O SSTL-2	**Compensation for DDR Horizontal Direction:** This signal is used to calibrate the DDR buffers. Used for both channels on the horizontal direction buffers. Externally it is connected to a 25 Ω resistor to ground.
DRCOMPVREF_H	Analog	**RComp VREF:** This signal is used for both channels on the horizontal direction buffers. This pin is connected to an external voltage derived from a resistor network.
ODTCOMP	I/O SSTL-2	**On-Die termination RCOMP:** This signal provides compensation for the On-Die Termination for the DDR interface. It is connected to an external 402 Ω 1% resistor for on die termination.

2.3 DDR Channel B Signals

Table 2-3. DDR Channel B Signals (Sheet 1 of 3)

Signal Name	Type	Description
CB_B[7:0]	I/O SSTL-2	**ECC Data bits:** These signals are the 8-bit ECC data, running at 2x data rate. The data is source synchronous using the DQS strobes.
DQ_B[63:0]	I/O SSTL-2	**Data:** These signals are the 64-bit data bus, running at 2x data rate. The data is source synchronous using the DQS_x strobes.
DQS_B[17:0]	I/O SSTL-2	**Data Strobes:** These signals provide the timing information for the data and ECC bits. They are driven by the source of the data; nine required for x8 and x16 RAMs, eighteen required for x4 RAMs. Mapping to data and ECC signals is shown in the functional description. When accessing x8 or x16 DRAM rows, DQS_B[17:9] are driven low during write cycles since these pins will be connected to the DM (data mask) inputs of the DRAMs on the DIMM.
CMDCLK_B[7:0]	O CMOS	**Differential Clock:** These signals are outputs to the DIMMs. Commands are referenced to the rising edge of CMDCLK_x and the falling edge of CMDCLK_x#. One per DIMM for registered DIMMs, three per DIMM for unbuffered DIMMs. The mapping is shown in the table below: • CK0/CK0# are at pins 137 and 138 of the DIMM. • CK1/CK1# are at pins 16 and 17 of the DIMM. • CMDCLK_B6 is multiplexed with CS_B5# **Signal** / **2 DIMM** / **3 DIMM** CMDCLK_B7 / DIMM 1 CK2 / CMDCLK_B6/CS_B5# / DIMM 0 CK2 / CMDCLK_B5 / DIMM 1 CK1 / CMDCLK_B4 / DIMM 0 CK1 / CMDCLK_B3 / / CMDCLK_B2 / / DIMM 2 CK0 CMDCLK_B1 / DIMM 1 CK0 / DIMM 1 CK0 CMDCLK_B0 / DIMM 0 CK0 / DIMM 0 CK0

Table 2-3. DDR Channel B Signals (Sheet 2 of 3)

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>CMDCLK_B[7:0]#</td><td>O
CMOS</td><td>Differential Clock: Output to DIMMs. Commands are referenced to the rising edge of CMDCLK_x and the falling edge of CMDCLK_x#. One per DIMM for registered DIMMs, three per DIMM for unbuffered DIMMs.
CMDCLK_B6# is multiplexed with CS_B4#
<table>
<tr><th>Signal</th><th>2 DIMM</th><th>3 DIMM</th></tr>
<tr><td>CMDCLK_B7#</td><td>DIMM 1 CK2#</td><td></td></tr>
<tr><td>CMDCLK_B6#/CS_B4#</td><td>DIMM 0 CK2#</td><td></td></tr>
<tr><td>CMDCLK_B5#</td><td>DIMM 1 CK1#</td><td></td></tr>
<tr><td>CMDCLK_B4#</td><td>DIMM 0 CK1#</td><td></td></tr>
<tr><td>CMDCLK_B3#</td><td></td><td></td></tr>
<tr><td>CMDCLK_B2#</td><td></td><td>DIMM 2 CK0#</td></tr>
<tr><td>CMDCLK_B1#</td><td>DIMM 1 CK0#</td><td>DIMM 1 CK0#</td></tr>
<tr><td>CMDCLK_B0#</td><td>DIMM 0 CK0#</td><td>DIMM 0 CK0#</td></tr>
</table></td></tr>
<tr><td>CS_B[5:0]#</td><td>O
SSTL-2</td><td>Chip Select: The chip select inputs determine which row a command is targeting. There is one per row (two per DIMM).
Muxed Chip Selects and clocks. These signals are chip select outputs on a 3-DIMM motherboard supporting registered DIMMs only, and clock outputs on a 2-DIMM motherboard that supports unbuffered or registered DIMMs. A configuration bit determines their function. The default function is chip selects.
CK2/CK2# are at pins 76 and 75 of the DIMM.
<table>
<tr><th>Signal</th><th>2 DIMM</th><th>3 DIMM</th></tr>
<tr><td>CS_B5#/CMDCLK_B6</td><td></td><td>DIMM 2 S1#</td></tr>
<tr><td>CS_B4#/CMDCLK_B6#</td><td></td><td>DIMM 2 S0#</td></tr>
<tr><td>CS_B3#</td><td>DIMM 1 S1#</td><td>DIMM 1 S1#</td></tr>
<tr><td>CS_B2#</td><td>DIMM 1 S0#</td><td>DIMM 1 S0#</td></tr>
<tr><td>CS_B1#</td><td>DIMM 0 S1#</td><td>DIMM 0 S1#</td></tr>
<tr><td>CS_B0#</td><td>DIMM 0 S0#</td><td>DIMM 0 S0#</td></tr>
</table></td></tr>
<tr><td>MA_B[13:0]</td><td>O
SSTL-2</td><td>Memory Address: These signals provide the row address for Active commands, and the column address and auto-precharge bit for read/write commands, to select one location out of the memory array in the respective bank. MA_B10 is sampled during a precharge command to determine whether the precharge applies to one bank (MA_B10 low) or all banks (MA_B10 high). If only one bank is to be precharged, the bank is selected by BA_B0, BA_B1. The address inputs also provide the op–code during a Mode Register Set command. BA_B0 and BA_B1 define which mode register is loaded during the Mode Register Set command (MRS or EMRS).</td></tr>
<tr><td>BA_B[1:0]</td><td>O
SSTL-2</td><td>Bank Address: The Bank Address specifies which bank an activate, read, write, or precharge command is targeting.</td></tr>
<tr><td>RAS_B#</td><td>O
SSTL-2</td><td>Row Address Strobe: This signal is used to indicate an activate command, opening a page specified by the MA_x signals in the bank specified by the BA_x signals. It is used with WE_B# to indicate a precharge command, closing the page in the bank specified by the BA_x signals. RAS_B# is also used to enter register set mode or start an auto refresh or enter self refresh.</td></tr>
</table>

Table 2-3. DDR Channel B Signals (Sheet 3 of 3)

Signal Name	Type	Description
CAS_B#	O SSTL-2	**Column Address Strobe:** This signal is used to indicate a read or write command to the open page in the bank specified by the BA_x signals. CAS_B# is also used to enter register set mode or start an auto refresh or enter self refresh.
WE_B#	O SSTL-2	**Write Enable:** This signal is used to differentiate a read from a write command when CAS_B# is active and RAS_B# is inactive. It is used to differentiate an activate command when RAS is active and CAS _B# is inactive. WE_B# is also used to terminate a burst, enter register set mode.
CKE_B[3:0]	O SSTL-2	**Clock Enable:** CKEx high activates and CKEx low deactivates internal clock signals, and device input buffers and output drivers. Driving CKEx low provides precharge powerdown and self refresh operation (all banks idle), or Active Powerdown (row active in any bank). CKEx is synchronous for powerdown entry and exit, and for self refresh entry. CKEx is asynchronous for self refresh exit, and for output disable. Input buffers, excluding CK, CK and CKEx are disabled during powerdown. Input buffers, excluding CKEx are disabled during self refresh. The CKEx signals are driven low when the RSTIN# signal is low to keep the DRAMs in self refresh mode. Registered: One for even rows, one for odd rows. Unbuffered: One per row. **Signal** / **2 DIMM MB** / **3 DIMM MB** CKE_B3 / DIMM 1 CKE1 / CKE_B2 / DIMM 1 CKE0 / CKE_B1 / DIMM 0 CKE1 / All DIMMs CKE1 CKE_B0 / DIMM 0 CKE0 / All DIMMs CKE0
RCVENOUT_B#	O SSTL-2	**Receive Enable Output:** This signal is driven low and fed back internally when the DQ bus is to receive data (DRAM reads). Used to set the timing for enabling the DQS input buffers so that they are enabled only when driven by the DRAMs. This signal must be terminated externally.
DVREF_B	I Analog	**Voltage Reference.**
DRCOMP_V	I/O SSTL-2	**Compensation for DDR Vertical Direction:** This signal is used to calibrate the DDR buffers. It is used for both channels on the vertical direction buffers. Externally, it is connected to a 25 Ω resistor to ground.
DRCOMPVREF_V	Analog	**RComp VREF:** This signal is used for both channels on the vertical direction buffers. This pin is connected to an external voltage derived from a resistor network.

2.4 Hub Interface_A Signals

Table 2-4. Hub Interface_A Signals

Signal Name	Type	Description
HI_A[11:0]	I/O (as/t/s) HI2	**HI_A Signals:** These signals are used for the hub interface between the Intel® ICH4 and the MCH.
PRCOMP_A	I/O HI2	**Compensation for HI:** This signal is used to calibrate the HI_A I/O Buffers.
PREF_A	I Analog	**HI_A Reference:** This signal is the reference voltage input for HI_A.
PSTRBF_0	I/O (as/t/s) HI2	**Packet Strobe First:** One of two strobe signals used to transmit or receive packet data over HI_A.
PSTRBS_0	I/O (as/t/s) HI2	**Packet Strobe Second:** One of two strobe signals used to transmit or receive packet data over HI_A.
PSWNG_A	I Analog	**HI_A Voltage Swing:** This signal provides a reference voltage used by the HI_A RCOMP Circuit.

2.5 Hub Interface_B Signals

Table 2-5. Hub Interface_B Signals

Signal Name	Type	Description
HI_B[21:20,18:0]	I/O (as/t/s) HI2	**HI_B Signals:** These signals are used for the 16-bit hub interface and the MCH. **NOTE:** HI_B19 is intentionally missing.
PRCOMP_B	I/O HI2	**Compensation for HI:** This signal is used to calibrate the HI_B I/O Buffers
PREF_B	I Analog	**HI_B Reference:** This is the reference voltage input for HI_B.
PSTRBF_B PSTRBS_B	I/O (as/t/s) HI2	**Lower Packet Strobe:** First HI Strobe and second HI Strobe together provide timing for source synchronous data transfer on HI_B16 and HI_B[7:0]. The agent that is sourcing the data drives this signal.
PUSTRBF_B PUSTRBS_B	I/O (as/t/s) HI2	**Upper Packet Strobe:** First Upper HI Strobe and second Upper HI Strobe together provide timing for source synchronous data transfer on HI_B17 and HI_B[15:8]. The agent that is sourcing the data drives this signal.
PSWNG_B	I Analog	**HI_B Voltage Swing:** This signal provides a reference voltage used by the HI_B RCOMP Circuit.

2.6 AGP Interface Signals

2.6.1 AGP Arbitration Signals

Table 2-6. AGP Arbitration Signals

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>GREQ# (2.0)
GREQ (3.0)</td><td>I
AGP</td><td>Request: This signal is the output of the AGP device used to request access to the bus to initiate a PCI (GFRAME(#)) or AGP (PIPE#) request. This signal is not required to initiate an AGP request via SBA.</td></tr>
<tr><td>GGNT# (2.0)
GGNT (3.0)</td><td>O
AGP</td><td>Grant: This signal is the output of the MCH either granting the bus to the AGP device to initiate a GFRAME(#) or PIPE(#) access (in response to GREQ(#) active) or to indicate that data is to be transferred for a previously enqueued AGP transaction. ST[2:0] indicates the purpose of the grant.</td></tr>
<tr><td>ST[2:0]</td><td>O
AGP</td><td>Status: This signal provides information from the arbiter to an AGP Master on what it may do. ST[2:0] only have meaning to the master when its GGNT(#) is asserted. When GGNT(#) is deasserted these signals have no meaning and must be ignored.
ST[2:0] are always an output from the MCH and an input to the master.
<table>
<tr><th>Encoding</th><th>Meaning</th></tr>
<tr><td>000</td><td>Previously requested low priority read data (Async read for AGP 3.0 signaling mode) is being returned to the master</td></tr>
<tr><td>001</td><td>Previously requested high priority read data is being returned to the master. Reserved in AGP 3.0 signaling mode</td></tr>
<tr><td>010</td><td>The master is to provide low priority write data (Async Write for AGP 3.0 signaling mode) for a previously queued write command</td></tr>
<tr><td>011</td><td>The master is to provide high priority write data for a previously queued write command. Reserved in AGP 3.0 signaling mode.</td></tr>
<tr><td>100</td><td>Previously requested isochronous read data is being returned to the master. AGP 3.0 signaling mode only.</td></tr>
<tr><td>101</td><td>The master is to provide isochronous write data for a previously queued write command. AGP 3.0 signaling mode only.</td></tr>
<tr><td>110</td><td>Calibration cycle. AGP 3.0 signaling mode only.</td></tr>
<tr><td>111</td><td>The master has been given permission to start a bus transaction. The master may queue AGP requests by asserting PIPE# (4x mode) or start a PCI transaction by asserting GFRAME(#).</td></tr>
</table></td></tr>
</table>

2.6.2 AGP Address / Data Signals

Table 2-7. AGP Address/ Data Signals

Signal Name	Type	Description
GDEVSEL# (2.0), GDEVSEL (3.0)	I/O s/t/s AGP	**Device Select:** During GFRAME(#) based accesses, GDEVSEL(#) is driven active by the target to indicate that it is responding to the access. Not used during AGP transactions
GAD[31:0]	I/O AGP	**Address/Data:** These signals provide the address for GFRAME(#) and PIPE(#) transactions, and the data for all transactions. They operate at a 1x data rate for GFRAME(#) based cycles other than Fast Write data phases, and the address phase of PIPE(#) based cycles, and operate at the specified channel rate (1x, 2x, 4x, or 8x) for AGP data phases and fast write data phases.
GC/BE[3:0]# (2.0), GC#/BE[3:0] (3.0)	I/O AGP	**Command/Byte Enables:** These signals provide the command during the address phase of a GFRAME(#) or PIPE(#) transaction, and byte enables during data phases. Byte enables are not used for read data of AGP 1x and 2x accesses, but are used for all write transactions, GFRAME(#) based reads, and 4x and 8x reads. These signals operate at the same data rate as the GAD[31:0] signals at any given time.
GPAR	I/O AGP	**Parity:** This signal is Not used on AGP transactions but used during GFRAME(#) based transactions as defined by the PCI specification. GPAR is not used during fast writes.
DBI_LO (3.0 only)	I/O AGP	**Dynamic Bus Inversion Lo:** This signal is provided along with GAD[15:0] to indicate whether GAD[15:0] must be inverted on the receiving end. • DBI_LO = 0. GAD[15:0] is not inverted so receiver may use as is. • DBI_LO = 1. GAD[15:0] is inverted so receiver must invert before use. The AD_STBF1 and AD_STBS1 strobes are used with DBI_LO. DBI is used in AGP 3.0 signaling mode only. In AGP 3.0 signaling mode (4x data rate), DBI is disabled by the MCH while transmitting (data never inverted and DBI_HI driven low) but is enabled when receiving data. For 8x data rate DBI is enabled when transmitting and receiving data.
AD_STB0 (2.0), AD_STBF0 (3.0)	I/O (s/t/s) AGP	**AD Bus Strobe-0:** In AGP 2.0 signaling mode, this signal provides timing for 2x and 4x clocked data on GAD[15:0] and GC/BE[1:0]#. The agent that is providing data drives this signal. **AD Bus Strobe First-0** in AGP 3.0 signaling mode. In AGP 3.0 signaling mode this signal strobes the first and all odd numbered data items with a low-to-high transition. It is used with GAD[15:0] and GC#/BE[1:0]
AD_STB0# (2.0), AD_STBS0 (3.0)	I/O (s/t/s) AGP	**AD Bus Strobe-0 Complement:** The differential complement to the AD_STB0 signal. In AGP 2.0 signaling mode, this signal is used to provide timing for 4x clocked data. **AD Bus Strobe Second-0:** In AGP 3.0 signaling mode this signal strobes the second and all even numbered data items with a low-to-high transition.
AD_STB1 (2.0), AD_STBF1 (3.0)	I/O (s/t/s) AGP	**AD Bus Strobe-1:** In AGP 2.0 signaling mode, this signal provides timing for 2x and 4x clocked data on GAD[31:16] and GC/BE[3:2]#. The agent that is providing data drives this signal. **AD Bus Strobe First-1:** In AGP 3.0 signaling mode this signal strobes the first and all odd numbered data items with a low-to-high transition. It is used with GAD[31:16], GC#/BE[3:2], DBI_HI, and DBI_LO.
AD_STB1# (2.0), AD_STBS1 (3.0)	I/O (s/t/s) AGP	**AD Bus Strobe-1 Complement:** The differential complement to the AD_STB1 signal. In AGP 2.0 signaling mode, it is used to provide timing for 4x clocked data. **AD Bus Strobe Second-1:** In AGP 3.0 signaling mode this signal strobes the second and all even numbered data items with a low-to-high transition.

2.6.3 AGP Command/Control Signals

Table 2-8. AGP Command/ Control Signals (Sheet 1 of 2)

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>PIPE# (2.0),
DBI_HI (3.0)</td><td>I/O
AGP</td><td>Pipelined Read: This signal is asserted by the current master to indicate a full width address is to be enqueued by the target. The master enqueues one request each rising clock edge while PIPE# is asserted. When PIPE# is deasserted, no new requests are re-queued across the AD bus.
PIPE# may be used in AGP 2.0 signaling modes, but is not permitted by the AGP 3.0 specification. When operating in AGP 3.0 signaling mode, the PIPE# signal is used for dynamic bus inversion.
PIPE# is a sustained tri-state signal from the master (graphics controller) and is an input to the MCH.
Dynamic Bus Inversion Hi (AGP 3.0 signaling mode). This signal goes along with GAD[31:16] to indicate whether GAD[31:16] must be inverted on the receiving end.
• DBI_HI = 0 GAD[31:16] is not inverted so receiver may use as is
• DBI_HI = 1 GAD[31:16] is inverted so receiver must invert before use.
• The AD_STBF1 and AD_STBS1 strobes are used with DBI_HI.
In AGP 3.0 signaling mode (4x data rate), DBI is disabled by the MCH while transmitting (data never inverted and DBI_HI driven low) but is enabled when receiving data. For 8x data rate, DBI is enabled when transmitting and receiving data.</td></tr>
<tr><td>SBA[7:0] (2.0),
SBA[7:0]# (3.0)</td><td>I
AGP</td><td>Sideband Address: This bus provides an additional bus to pass address and command to the MCH from the AGP master.

NOTE: In AGP 2.0 signaling mode, when sideband addressing is disabled, these signals are isolated. When sideband addressing is enabled, internal pull-ups are enabled to prevent indeterminate values on them in cases where the Graphics Card may not have its SBA[7:0] output drivers enabled yet.</td></tr>
<tr><td>SB_STB (2.0),
SB_STBF (3.0)</td><td>I
AGP</td><td>Sideband Strobe: In AGP 2.0 signaling mode, this signal is used to provide timing for 4x clocked data.
Sideband Strobe First: In AGP 3.0 signaling mode this signal strobes the first and all odd numbered data items with a low-to-high transition.</td></tr>
<tr><td>SB_STB# (2.0),
SB_STBS (3.0)</td><td>I
AGP</td><td>Sideband Strobe Complement: The differential complement to the SB_STB signal. In AGP 2.0 signaling mode, it is used to provide timing for 4x clocked data in.
Sideband Strobe Second: In AGP 3.0 signaling mode this signal strobes the second and all even numbered data items with a low-to-high transition.</td></tr>
<tr><td>GFRAME# (2.0),
GFRAME (3.0)</td><td>I
AGP</td><td>FRAME: This signal is driven by the current master to indicate the beginning and duration of a standard PCI protocol (“Frame Based”) transaction and during fast writes. It is not used, and must be inactive during AGP transactions.</td></tr>
<tr><td>GIRDY# (2.0),
GIRDY (3.0)</td><td>I/O
s/t/s
AGP</td><td>Initiator Ready: This signal is used for both GFRAME(#) based and AGP transactions. During AGP transactions, it indicates the AGP compliant master is ready to provide all write data for the current transaction. Once IRDY# is asserted for a write operation, the master is not allowed to insert wait-states. The assertion of IRDY# (IRDY) for reads indicates that the master is ready to transfer to a subsequent block (32 bytes) of read data. The master is never allowed to insert a wait-state during the initial data transfer (32 bytes) of a read transaction. However, it may insert wait-states after each 32-byte block is transferred.

NOTE: There is no GFRAME(#) – GIRDY(#) relationship for AGP transactions.</td></tr>
</table>

Table 2-8. AGP Command/ Control Signals (Sheet 2 of 2)

Signal Name	Type	Description
GTRDY# (2.0), GTRDY (3.0)	I/O s/t/s AGP	**Target Ready:** This signal is used for both GFRAME(#) based and AGP transactions. During AGP transactions, it indicates the AGP compliant target is ready to provide read data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait-states after each block (32 bytes) is transferred on both read and write transactions.
GSTOP# (2.0), GSTOP (3.0)	I/O s/t/s AGP	**STOP:** This signal is used during GFRAME(#) based transactions by the target to request that the master stop the current transaction. This signal is not used during AGP transactions.
RBF# (2.0), RBF (3.0)	I/O s/t/s AGP	**Read Buffer Full:** This signal indicates if the master is ready to accept previously requested low priority read data. When RBF(#) is asserted, the MCH is not allowed to return low priority read data to the AGP master on the first block. RBF(#) is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data, then it is not required to implement this signal.
WBF# (2.0), WBF (3.0	I AGP	**Write Buffer Full:** This signal indicates if the master is ready to accept Fast Write data from the MCH. When WBF(#) is asserted, the MCH is not allowed to drive Fast Write data to the AGP master. WBF(#) is only sampled at the beginning of a cycle. If the AGP master is always ready to accept fast write data, it is not required to implement this signal.
SERR# (2.0), SERR (3.0)	I AGP	**Serious Error:** The AGP master may assert this signal to indicate an address parity error or other serious error. The master asserts the signal for one clock, then float it. When enabled, the SERR will be passed onto the Intel® ICH4 as an SERR message on the HI_A. The enable bit is in the Bridge Control Register of Device 1 (the SERRE bit of the PCI Command register of Device 1 must also be a 1).
PRCOMP_AGP0	I	**Compensation for AGP:** This signal is used to calibrate the AGP buffers. It needs to be pulled up to VCC_AGP through a 40 Ω resistor.
PRCOMP_AGP1	I/O CMOS	**Compensation for AGP:** This signal is used to calibrate the AGP buffers. It needs to be pulled up to VCC_AGP through a 40 Ω resistor.
PREF_AGP0	I Analog	**AGP Reference 0:** Provides the VREF for AGP signals. The PREF_AGP0 signal is the switching point for the signaling on the AGP bus. The signals are tied together on the MCH side.
PREF_AGP1	I Analog	**AGP Reference 1:** Provides the VREF for AGP signals. The PREF_AGP1 signal is the switching point for the signaling on the AGP bus. The signals are tied together on the MCH side.
PSWNG_AGP0	I Analog	**PSWNG_AGP0:** This signal provides a reference voltage used by the AGP RCOMP0 circuit. This signal is derived from 1.5 V by a resistor divider circuit. The max level for this signal is 0.8 V
PSWNG_AGP1	I Analog	**PSWNG_AGP1:** This signal provides a reference voltage used by the AGP RCOMP1 circuit. This signal is derived from 1.5 V by a resistor divider circuit. The max level for this signal is 0.8 V.

2.7 Clocks, Reset, and Miscellaneous Signals

Table 2-9. Clocks, Reset, and Miscellaneous Signals

Signal Name	Type	Description
HCLKINP HCLKINN	I DiffCLK	**Differential Host Clock In:** These pins receive a differential host clock from the external clock synthesizer. This clock is used by all the Intel® E7505 chipset MCH logic in the host clock domain.
GCLKIN	I CMOS	**66 MHz Clock In:** This pin receives a 66 MHz clock from the clock synthesizer. This clock is used by AGP/PCI and HI_A,B clock domains. Note that this clock input is 3.3 V tolerant.
PWRGD	I CMOS	**Power Good:** PWRGD resets all MCH, including “sticky” logic.
RSTIN#	I CMOS	**Reset In:** When asserted, this signal will asynchronously reset the MCH logic. This signal is connected to the PCIRST# output of the Intel® ICH4. This signal is sampled in the S3 power state and used to force DDR outputs to the reset state and force the CKE pins low. • This input does not reset the sticky logic. • This input should have a Schmitt trigger to avoid spurious resets. • This input needs to be 3.3 V tolerant.
XORMODE#	I CMOS	**Test Input:** When asserted, the MCH places all outputs in XOR-mode for board-level testing.
TESTIN#	I/O CMOS	**Test Input:** This pin is used for manufacturing and board level test purposes.
TESTSIG1	I/O	**Test signal 1:** To keep the XOR Chain contiguous, this signal must have an accessible test point if XOR Testing is to be implemented. This signal may be floated.
TESTSIG2	I/O	**Test signal 2:** To keep the XOR Chain contiguous, this signal must have an accessible test point, if XOR Testing is to be implemented. This signal may be floated.
VCCAGP		**Power:** Power pins for the APG interface.
VCCAHI		**Power:** Analog power pin for hub interface.
VTT		**Power:** Power pins for the processor interface.
VCCAFSB		**Power:** Analog power for system bus interface.
VCCDDR		**Power:** Power pins for DDR interface.
VCC[1]		**Power:** These pins are 1.2 V and 1.3 V power pins.
VSS		**Ground:** Ground pin.

NOTE: 1) VCC is set at 1.2 V or 1.3V depending on the part. Please refer to the E7505 Specification Update for more information

2.8 Strap Signals

Pin	Strap Name	Description
DDR_STRAP	I CMOS	**DDR Strap Input.** This pin is used to indicate to the BIOS the memory type. This pin should be grounded on a motherboard implementing registered DDR DIMMs. It should be pulled up to 2.5 V on a motherboard implementing unbuffered DDR DIMMs.
HA7#	CPU Bus In-Order Queue Depth	The value on HA7# is sampled by all processor bus agents, including the MCH, on the rising edge of CPURST#. Its latched value determines the maximum IOQ depth mode supported on the processor bus. • If HA7# is sampled low, the IOQ depth on the bus is one. • If HA7# is sampled high, the IOQ depth on the bus is the maximum of 12. This signal is driven by the MCH from the value set by BIOS.
HA15#	SB Bus Parking	The value on HA15# is sampled by all processor bus agents, including the MCH, on the rising edge of CPURST#. A high voltage level will force the processor(s) into Bus Parking Mode. This signal has no functional affect on the MCH itself. This signal is driven by the MCH from the value set by BIOS.
VREF Compare	AGP Select	The state of the VREF Comparator determines the use of the muxed AGP signals. The PREF_AGP[1:0] inputs will be at 0.35 V for AGP 3.0 signaling made, and 0.75 V for AGP 2.0 signaling mode. This level is set by resistors using the GC_DET# pin on the AGP connector, or from the AGPVREFGC generated by the graphics card. The VREF Comparator will be 0 for AGP3.0 signaling mode and a 1 for AGP 2.0 signaling mode **VREF Analog Level** **Mode** 0.35 V AGP 3.0 signaling 0.75 V APG 2.0 signaling

NOTE: HA7# and HA15# are part of the regular system address bus; therefore, they do not require extra pins for this support.

Register Description 3

This chapter describes the MCH PCI configuration registers. A detailed register bit description is provided. The MCH contains two sets of software accessible registers, accessed via the Host processor I/O address space:

- **Control registers** – These registers are I/O mapped into the processor I/O space, which control access to PCI configuration space (see section entitled I/O Mapped Registers)
- **Internal configuration registers** – These registers, which reside within the MCH, are partitioned into multiple logical device register sets ("logical" since they reside within a single physical device). There are three primary device register sets; for the DRAM controller/HI_A (controls PCI_A, i.e., DRAM configuration, other chipset operating parameters, and optional features); another set is for the AGP; and another set for the HI_B interface.

The MCH supports PCI configuration space accesses using the mechanism denoted as Configuration Mechanism #1 in the PCI specification.

The MCH internal registers (I/O mapped and configuration registers) are accessible by the host. The registers can be accessed as Byte (8-bit), Word (16-bit), or DWord (32-bit) quantities, with the exception of the CONFIG_ADDRESS Register, which can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field).

3.1 Register Nomenclature and Access Attributes

Term	Description
RO	**Read-Only**. If a register is read-only, writes to this register have no effect.
R/W	**Read/Write**. A register with this attribute can be read and written
R/WC	**Read/Write Clear**. A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.
R/WO	**Read/Write-Once**. A register bit with this attribute can be written to only once after power up. After the first write, the bit becomes read-only.
R/W/L	**Read/Write/Lock.** A register with this attribute can be read, written, and locked.
L	**Lock.** A register bit with this attribute becomes read only after a lock bit is set.
Sticky	Certain registers in the MCH are sticky through a soft-reset. They will only be reset on a hard reset or power-good reset. These registers in general are the error logging registers and a few special cases.
Reserved Bits	Some of the MCH registers described in this section contain reserved bits. These bits are labeled "Reserved" or "Intel Reserved." Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note that software does not need to perform read, merge, write operation for the configuration address register.

Term	Description
Reserved Registers	In addition to reserved bits within a register, the MCH contains address locations in the configuration space of the Host-hub interface Bridge/DRAM Controller and the internal graphics device entities that are marked either “Reserved” or Intel Reserved.” When a “Reserved” register location is read, a random value can be returned. (“Reserved” registers can be 8, 16, or 32 bits in size). Registers that are marked as “Reserved” must not be modified by system software. Writes to “Reserved” registers may cause system failure.
Default Value Upon Reset	Upon a full reset, the MCH sets all of its internal configuration registers to predetermined **default** states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters, and optional system features that are applicable, and to program the MCH registers accordingly.

3.2 PCI Configuration Space Access

The MCH and the ICH4 are physically connected by HI_A. From a configuration standpoint, HI_A is logically PCI bus #0. As a result, all devices internal to the MCH and ICH4 appear to be on PCI bus #0. The system’s primary PCI expansion bus is physically attached to the ICH4 and, from a configuration perspective appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI Bus number.

Note: The primary PCI bus is referred to as PCI_A in this document and is not PCI bus #0 from a configuration standpoint.

The 16-bit hub interface ports appear to system software to be real PCI buses behind PCI-to-PCI bridges resident as devices on PCI bus #0. The MCH decodes multiple PCI Device numbers. The configuration registers for the devices are mapped as devices residing on PCI bus #0. Each Device Number may contain multiple functions.

- **Device 0**: Chipset Host Controller. Logically device 0 appears as a PCI device residing on PCI bus #0. Physically, device 0 contains the standard PCI registers, DRAM controller registers, HI_A registers, and other MCH specific registers.
- **Device 1:** Host-to-AGP Bridge. Logically this appears as a “virtual” PCI-to-PCI bridge residing on PCI bus #0. Physically Device 1 contains the standard PCI-to-PCI bridge registers and the standard AGP/PCI configuration registers (including the AGP I/O and memory address mapping).
- **Device 2**: Host-to-HI_B Bridge. Logically this bridge appears to be a PCI-to-PCI bridge device residing on PCI bus #0. Physically, Device 2 contains the standard PCI registers and configuration registers for HI_B.

Table 3-1 shows the device number assignment for the various internal MCH devices:

Table 3-1. MCH Logical Configuration Resources

MCH Function	Device #, Function #
Chipset Host Controller	Device 0, Function 0
Chipset Host RAS Controller	Device 0, Function 1
Host-to-AGP Bridge (16 bit PCI-to-PCI)	Device 1, Function 0
Host-to-HI_B Bridge Controller (16 bit PCI-to-PCI)	Device 2, Function 0
Host-to-HI_B Bridge Error Reporting (16 bit PCI-to-PCI)	Device 2, Function 1

A disabled or non-existent device's configuration register space is hidden, returning all 1s for reads and dropping writes just as if the cycle terminated with a Master Abort on PCI.

The MCH automatically detects if devices are connected to HI_B by sampling the corresponding REQI signal on the rising edge of RSTIN#. When a hub interface is unpopulated, the associated configuration register space is hidden, returning all 1s for all registers just as if the cycle terminated with a Master Abort on PCI.

Logically, the ICH4 appears as multiple PCI devices within a single physical component also residing on PCI bus #0. One of the ICH4 devices is a PCI-to-PCI bridge. Logically, the primary side of the bridge resides on PCI #0 while the secondary side is the standard PCI expansion bus.

Note: A physical PCI bus #0 does not exist. HI_A and the internal devices in the MCH and ICH4 logically constitute PCI Bus #0 to configuration software.

3.2.1 PCI Bus Configuration Mechanism

The PCI Bus defines a slot-based configuration space that allows each device to contain up to eight functions; each function contains up to 256, 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the MCH. The PCI specification defines two mechanisms to access configuration space, Mechanism 1 and Mechanism 2. **The MCH supports only Mechanism 1**.

The configuration access mechanism makes use of the CONFIG_ADDRESS register and CONFIG_DATA register. To reference a configuration register a Dword I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFIG_ADDRESS31 must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA results in the MCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The MCH is responsible for translating and routing the processor's I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal MCH configuration registers for HI_A, HI_B.

3.3 General Routing Configuration Accesses

The MCH supports two Hub interfaces: HI_A and HI_B. PCI configuration cycles are selectively routed to one of these interfaces. The MCH is responsible for routing PCI configuration cycles to the proper interface. PCI configuration cycles to ICH4 internal devices and Primary PCI (including downstream devices) are routed to the ICH4 via HI_A. PCI configuration cycles to any of the 16-bit hub interfaces are routed to HI_B. AGP configuration cycles are routed to AGP. The AGP interface is treated as a separate PCI bus from the configuration point of view. Routing of configuration accesses to HI_B is controlled via the standard PCI-to-PCI bridge mechanism using information contained within the primary bus number, the secondary bus number, and the subordinate bus number registers of the corresponding PCI-to-PCI bridge device.

Note: The MCH supports a variety of connectivity options. When any of the MCH's interfaces are disabled, the associated interface's device registers are not visible. Configuration cycles to these registers will return all 1s for a read and master abort for a write.

3.3.1 Logical PCI Bus #0 Configuration Mechanism

The MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. When the Bus Number field of CONFIG_ADDRESS is 0, the configuration cycle is targeting a PCI Bus #0 device.

- The Host-HI_A Bridge entity within the MCH is hardwired as Device 0 on PCI Bus #0
- The AGP Bridge entity within the MCH is hardwired as Device 1 on PCI Bus #0.
- The Host-HI_B bridge entity within the MCH is hardwired as Device 2 on PCI Bus #0.

Configuration cycles to any of the MCH's enabled internal devices are confined to the MCH and not sent over HI_A. Accesses to disabled MCH internal devices are forwarded over HI_A as Type 0.

The ICH4 decodes the Type 0 access and generates a configuration access to the selected internal device.

3.3.2 Primary PCI Downstream Configuration Mechanism

When the Bus Number in the CONFIG_ADDRESS is non-zero, and does not lie between the Secondary Bus Number registers and the Subordinate Bus Number registers for the hub interface, the MCH generates a type 1 HI_A Configuration Cycle.

When the cycle is forwarded to the ICH4 via HI_A, the ICH4 compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus Number registers of its PCI-to-PCI bridges to determine if the configuration cycle is meant for Primary PCI, or a downstream PCI bus.

3.3.3 HI_B Bus Configuration Mechanism

From the chipset configuration perspective, HI_B is seen as a PCI bus interface residing on a Secondary Bus side of the virtual PCI-to-PCI bridge referred to as the MCH Host-HI_B bridge.

When the bus number is non-zero, greater than the value programmed into the Secondary Bus Number register, and less than or equal to the value programmed into the corresponding Subordinate Bus Number register, the configuration cycle is targeting a PCI bus downstream of the targeted hub interface. The MCH generates a Type 1 hub interface configuration cycle on the appropriate hub interface.

3.3.4 AGP Bus Configuration Mechanism

From the chipset configuration perspective, AGP is seen as a PCI bus interface residing on a Secondary Bus side of the virtual PCI-to-PCI bridges referred to as the MCH Host-to-AGP bridge. On the Primary bus side, the virtual PCI-to-PCI bridge is attached to PCI Bus #0. Therefore, the Primary Bus Number register is hardwired to 0. The virtual PCI-to-PCI bridge entity converts Type #1 PCI Bus Configuration cycles on PCI Bus #0 into Type 0 or Type 1 configuration cycles on the AGP interface. Type 1 configuration cycles on PCI Bus #0 that have a Bus Number that matches the Secondary Bus Number of the MCH's virtual Host-to-AGP bridge will be translated into Type 0 configuration cycles on the AGP interface. The MCH will decode the Device Number field 15:11 and assert the appropriate GAD signal as an IDSEL in accordance with the PCI-to-PCI Bridge Type 0 configuration mechanism.

If the Bus Number is non-zero, greater than the value programmed into the Secondary Bus Number register, and less than or equal to the value programmed into the Subordinate Bus Number register the configuration cycle is targeting a PCI bus downstream of the targeted interface. The MCH will generate a Type 1 PCI configuration cycle on AGP.

3.4 I/O Mapped Registers

The MCH contains two registers that reside in the processor I/O address space; the Configuration Address (CONFIG_ADDRESS) register and the Configuration Data (CONFIG_DATA) register. The Configuration Address register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.4.1 CONFIG_ADDRESS—Configuration Address Register

Address Offset: 0CF8h
Default Value: 0000 0000h
Attribute: R/W
Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a Dword. A “byte” or “word” reference will pass through the Configuration Address register and HI_A onto the PCI_A bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Default, Access	Descriptions
31	0b R/W	**Configuration Enable (CFGE).** 1 = Enable. 0 = Disable.
30:24		**Reserved** (These bits are read only and have a value of 0.)
23:16	00h R/W	**Bus Number.** Contains the bus number being targeted by the config cycle.
15:11	00000b R/W	**Device Number.** Selects one of the 32 possible devices per bus.
10:8	000b R/W	**Function Number.** Selects one of eight possible functions within a device.
7:2	00000b R/W	**Register Number.** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address register. This field is mapped to A7:2 during HI_A-D Configuration cycles.
1:0		Reserved

3.4.2 CONFIG_DATA—Configuration Data Register

Address Offset: 0CFCh
Default Value: 0000 0000h
Attribute: R/W
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Default, Access	Descriptions
31:0	0000h, R/W	**Configuration Data Window (CDW).** If bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register are mapped to configuration space using the contents of CONFIG_ADDRESS.

3.5 Chipset Host Controller Registers (Device 0, Function 0)

The Chipset Host Controller registers are in Device 0 (D0), Function 0 (F0). Table 3-2 provides the register address map for this device, function.

Warning: Address locations that are not listed the table are considered reserved register locations. Writes to “Reserved” registers may cause system failure. Reads to “Reserved” registers may return a non-zero value.

Table 3-2. Chipset Host Controller Register Address Map (D0:F0)

Address Offset	Mnemonic	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	2550h	RO
04–05h	PCICMD	PCI Command Register	0006h	RO, RW
06–07h	PCISTS	PCI Status Register	0090h	R/WC, RO
08h	RID	Revision Identification	see register description	RO
0Ah	SUBC	Sub Class Code	00h	RO
0Bh	BCC	Base Class Code	00h	RO
0Dh	MLT	Master Latency Timer	06h	RO
0Eh	HDR	Header Type	00h	RO
10–13h	APBASE	Aperture Base Config	0000 0008h	RO, RW
2C–2Dh	SVID	Subsystem Vendor ID	0000 0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAPPTR	Capabilities Pointer	40h	RO
40–43h	CAPID	Product Specific Capability Identifier	00 0104 A009h	RO
50–51h	MCHCFG	MCH Configuration	0004h	RO, RW
59–5Fh	PAM[0–6]	Programmable Attribute Map (7 registers)	00h	RO, RW
60–67h	DRB	DRAM Row Boundary	xxh	RW
70–73h	DRA	DRAM Row Attribute	00h	RO, RW
78–7Bh	DRT	DRAM TIming Register	0000 0010h	RO
7C–7Fh	DRC	DRAM Controller Mode	0044 0009h	RO, RW
80–81	REROTC	Receive Enable Reference Output Timing Control Register	00	RW
8Ch	CLOCK_DIS	CK/CK# Clock Disable	FFh	
8Eh	DDR_CNTL	DDR Memory control Register	00xx 0000b	
9Dh	SMRAM	System Management RAM Control	02h	RW, RO
9Eh	ESMRAMC	Extended System Management RAM Control	38h	R/W/L, RW/C, RO
A0–A3h	ACAPID	AGP Capability Identifier	0030 0002h	RO

Table 3-2. Chipset Host Controller Register Address Map (D0:F0)

Address Offset	Mnemonic	Register Name	Default Value	Access
A4–A7h	AGPSTAT	AGP Status Register	see register description	RO
A8–ABh	AGPCMD	AGP Command Register	0000 0000h	RW, RO
B0–B3h	AGPCTRL	AGP Control Register	0000 0000h	RW, RO
B4h	APSIZE	Aperture Size	00h	RW, RO
B8–BBh	ATTBASE	Aperture Translation Table	0000 0000h	RW, RO
BCh	AMTT	AGP MTT Control Register	00h	RW, RO
BDh	LPTT	AGP Low Priority Transaction Timer Reg	00h	RW, RO
C4–C5h	TOLM	Top of Low Memory Register	0800h	RW, RO
C6–C7h	REMAPBASE	Remap Base Address Register	03FFh	RW, RO
C8–C9h	REMAPLIMIT	Remap Limit Address Register	0000h	RW, RO
DE–DFh	SKPD	Scratch Pad Data	0000h	RW
E0–E1h	DVNP	Device Not Present	1D1Fh	RW, RO

3.5.1 VID—Vendor Identification Register (D0:F0)

Address Offset: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register combined with the Device Identification register uniquely identify any PCI device.

Bits	Default, Access	Description
15:0	8086h, RO	**Vendor Identification Number**. This register field contains the PCI standard identification for Intel, 8086h.

3.5.2 DID—Device Identification Register (D0:F0)

Address Offset: 02–03h
Default Value: 2550h
Attribute: RO
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device.

Bits	Default, Access	Description
15:0	2550h, RO	**Device Identification Number (DID).** This is a 16-bit value assigned to the MCH Host Controller Bridge Function 0.

3.5.3 PCICMD—PCI Command Register (D0:F0)

Address Offset: 04–05h
Default Value: 0006h
Attribute: RO, R/W
Size: 16 bits

Since MCH Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Bits	Default, Access	Description
15:10		Reserved
9	0b RO	**Fast Back-to-Back Enable (FB2B).** Hardwired to 0. This bit controls whether or not the master can do fast back-to-back write. Since device 0 is strictly a target, this bit is not implemented.
8	0b R/W	**SERR Enable (SERRE).** This bit is a global enable bit for Device 0 SERR messaging. The MCH does not have an SERR signal. The MCH communicates the SERR condition by sending an SERR message over HI_A to the Intel® ICH4. 0 = Disable. SERR message is not generated by the MCH for Device 0. 1 = Enable. MCH is enabled to generate SERR messages over HI_A for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTAT and PCISTS registers. **NOTE:** Note that this bit only controls SERR messaging for the Device 0. Devices 1-6 have their own SERR bits to control error reporting for error conditions occurring on their respective devices. The control bits are used in a logical OR manner to enable the SERR HI message mechanism.
7	0b RO	**Address/Data Stepping Enable (ADSTEP).** Hardwired to 0. Address/data stepping is not implemented in the MCH.
6	0b R/W	**Parity Error Enable (PERRE).** 0 = Disable. MCH does not take any action when it detects a parity error on HI_A. 1 = Enable. MCH generates an SERR message over HI_A to the ICH4 when an address or data parity error is detected by the MCH on HI_A (DPE set in PCISTS) and SERRE is set to 1.
5	0b RO	**VGA Palette Snoop Enable (VGASNOOP).** Hardwired to 0. The MCH does not implement this bit.
4	0b RO	**Memory Write and Invalidate Enable (MWIE).** Hardwired to 0. The MCH never issues memory write and invalidate commands.
3	0b RO	**Special Cycle Enable (SCE).** Hardwired to 0. The MCH does not implement this bit.
2	1b RO	**Bus Master Enable (BME).** Hardwired to 1. The MCH is always enabled as a master on HI_A.
1	1b RO	**Memory Access Enable (MAE).** Hardwired to 1. The MCH always allows access to main memory.
0	0b RO	**I/O Access Enable (IOAE).** Hardwired to 0. This bit is not implemented in the MCH.

3.5.4 PCISTS—PCI Status Register (D0:F0)

Address Offset: 06–07h
Default Value: 0090h
Attribute: RO, R/WC
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device 0's PCI interface. Bit 14 is read/write clear. All other bits are Read Only. Since MCH Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Note: Software must write a 1 to clear bits that are set.

Bits	Default, Access	Description
15	0b R/WC	**Detected Parity Error (DPE).** 0 = No Parity error detected. 1 = MCH detected an address or data parity error on the HI_A interface.
14	0b R/WC	**Signaled System Error (SSE).** 0 = No SERR generated by MCH Device 0. 1 = MCH Device 0 generated an SERR message over HI_A for an enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD and ERRCMD registers. Device 0 error flags are read/reset from the PCISTS or Error registers.
13	0b RO	**Received Master Abort Status (RMAS).** Hardwired to 0. The Intel® ICH4 will never send a Master Abort completion on HI_A.
12	0b R/WC	**Received Target Abort Status (RTAS).** 0 = No received Target Abort generated by MCH. 1 = MCH generated a HI_A request that receives a Target Abort completion packet.
11	0b RO	**Signaled Target Abort Status (STAS).** Hardwired to 0. The MCH will not generate a Target Abort HI_A completion packet.
10:9	00b RO	**DEVSEL Timing (DEVT).** Hardwired to 00. Device 0 does not physically connect to PCI_A. These bits are set to 00 (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the MCH.
8	0b RO	**Master Data Parity Error Detected (DPD).** Hardwired to 0. PERR signaling and messaging are not implemented by the MCH.
7	1b RO	**Fast Back-to-Back (FB2B).** Hardwired to 1. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the MCH.
6:5		Reserved
4	1b, RO	**Capability List (CLIST).** Hardwired to 1. This indicates to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the AGP Capability standard register resides. This bit is always a 1, since the fuse capability structure exists in all configurations.
3:0		Reserved

3.5.5 RID—Revision Identification Register (D0:F0)

Address Offset: 08h
Default Value: see table below
Attribute: RO
Size: 8 bits

This register contains the revision number of the MCH Device 0.

Bits	Default, Access	Description
7:0	00h, RO	**Revision Identification Number (RID).** This is an 8-bit value that indicates the revision identification number for the MCH Device 0. 03h = B-0 Stepping

3.5.6 SUBC—Sub-Class Code Register (D0:F0)

Address Offset: 0Ah
Default Value: 00h
Attribute: RO
Size: 8 bits

Bits	Default, Access	Description
7:0	00h, RO	**Sub-Class Code (SUBC).** This is an 8-bit value that indicates the category of Bridge into which the MCH falls. 00h = Host Bridge.

3.5.7 BCC—Base Class Code Register (D0:F0)

Address Offset: 0Bh
Default Value: 06h
Attribute: RO
Size: 8 bits

Bits	Default, Access	Description
7:0	06h, RO	**Base Class Code (BASEC).** This is an 8-bit value that indicates the Base Class Code for the MCH. 06h = Bridge device.

3.5.8 MLT—Master Latency Timer Register (D0:F0)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Device 0 in the MCH is not a PCI master; therefore, this register is not implemented.

Bits	Default, Access	Description
7:0		Reserved

3.5.9 HDR—Header Type Register (D0:F0)

Address Offset: 0Eh
Default Value: 00h or 80h
Attribute: RO
Size: 8 bits

Bits	Default, Access	Description
7:0	00h or 80, RO	**PCI Header (HDR).** This read only field indicates whether the MCH is a multi-function device. 00h = Single Function Device (Function 1 is disabled in address offset E0h, bit 0) 80h = Multi Function Device (Function 1 is enabled in address offset E0h, bit 0)

3.5.10 APBASE—Aperture Base Configuration Register (D0:F0)

Address Offset: 10–13h
Default Value: 0000 0008h
Attribute: RO, RW
Size: 32 bits

The APBASE is a standard PCI Base Address register that is used to set the base of the Graphics Aperture. The standard PCI Configuration mechanism defines the base address configuration register such that only a fixed amount of space can be requested (dependent on which bits are hardwired to 0 or behave as hardwired to 0). To allow for flexibility (of the aperture) an additional register called APSIZE is used as a "back-end" register to control which bits of the APBASE will behave as hardwired to 0. This register will be programmed by the MCH specific BIOS code that will run before any of the generic configuration software is run. **Set by BIOS.**

Note: The intention is that the APSIZE register force individual bits to Read Only as 0; however, the MCH (and other chips) implementation only causes them to be read only, and does not force them to 0. The default is 0, so the difference only occurs if the aperture is set to a small size, specific APBASE bits are set to 1s, and the aperture size is then increased. APBASE bits affected by the APSIZE change are then RO as whatever value had previously been written. While this could cause bits to read back as 1 instead of 0, the actual aperture decode will be done properly according to the APSIZE register. Software can avoid this situation by writing the APBASE register to 0 prior to increasing the aperture size via APSIZE. The aperture should be disabled prior to any change in APBASE or APSIZE.

Note: Bit 9 of the MCHCFG register is used to prevent accesses to the aperture range before this register is initialized by the configuration software and the appropriate translation table structure has been established in the main memory.

Bits	Default, Access	Description
31:28	0h R/W	**Upper Programmable Base Address (UPBITS).** These bits are part of the aperture base set by configuration software to locate the base address of the graphics aperture. They correspond to bits 31:28 of the base address in the processor's address space that will cause a graphics aperture translation to be inserted into the path of any memory read or write.
27:22	00h RW or RO depending on aperture size	**Middle Hardwired/Programmable Base Address (MIDBITS).** These bits are part of the aperture base set by configuration software to locate the base address of the graphics aperture. They correspond to bits 27:4 of the base address in the processor's address space that will cause a graphics aperture translation to be inserted into the path of any memory read or write. These bits can individually behave as read only if programmed to do so by the APSIZE bits of the APSIZE register. This causes configuration software to understand that the granularity of the graphics aperture base address is either finer or more coarse, depending upon the bits set by MCH-specific configuration software in APSIZE.
21:4	00000h RO	**Lower Bits (LOWBITS).** Hardwired to 00000h. This forces the minimum aperture size selectable by this register to be 4 MB without regard to the aperture size definition enforced by the APSIZE register.
3	1b RO	**Prefetchable (PF).** Hardwired to 1. This identifies the Graphics Aperture range as perfectible, as per the PCI specification for base address registers. Thus, there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and the MCH can merge processor writes into this range without causing errors.
2:1	00b RO	**Addressing Type (TYPE).** Hardwired to 00. This indicates that address range defined by the upper bits of this register can be located anywhere in the 32-bit address space as per the PCI specification for base address registers.
0	0b RO	**Memory Space Indicator (MSPACE).** Hardwired to 0. This identifies the aperture range as a memory range as per the specification for PCI base address registers.

3.5.11 SVID—Subsystem Vendor Identification Register (D0:F0)

Address Offset: 2C–2Dh
Default Value: 0000h
Attribute: R/WO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bits	Default, Access	Description
15:0	0000h R/WO	**Subsystem Vendor ID (SUBVID).** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

3.5.12 SID—Subsystem Identification Register (D0:F0)

Address Offset: 2E–2Fh
Default Value: 0000h
Attribute: R/WO
Size: 16 bits

This value is used to identify a particular subsystem.

Bits	Default, Access	Description
15:0	0000h R/WO	**Subsystem ID (SUBID).** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

3.5.13 CAPPTR—Capabilities Pointer Register (D0:F0)

Address Offset: 34h
Default Value: 40h
Attribute: RO
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location where the first set of capabilities registers are located. **Read by drivers.**

Bits	Default, Access	Description
7:0	40h RO	**First capability ID Pointer.** This field points to the offset of the first capability ID register block. In this case the first capability is the Product_Specific Capability, which is located at offset 40h.

3.5.14 CAPID—Product Specific Capability Identifier Register (D0:F0)

Address Offset: 40–43h
Default Value: 0104 A009h
Attribute: RO
Size: 32 bits

The fields in this register contain product specific capabilities. The CAPPTR register provides the offset that points to this register. **Set by BIOS.**

Bits	Default, Access	Description
31:28		Reserved
27:24	0001b RO	**CAPID Version.** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	04h RO	**CAPID Length.** This field has the value 04h to indicate the structure length (4 bytes)
15:8	A0h RO	**Next Capability Pointer.** This field points to the next Capability ID in this device, which is the AGP register block.
7:0	09h RO	**CAP_ID.** This field has the value to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

3.5.15 MCHCFG—MCH Configuration Register (D0:F0)

Address Offset: 50–51h
Default Value: 0004h
Attribute: RO, R/W
Size: 16 bits

Bits	Default, Access	Description
15		Reserved
14:13	00b R/W	**Number of Stop Grant Cycles (NSG).** This field contains the number of Stop Grant transactions expected on the SB bus before a Stop Grant Acknowledge packet is sent to the Intel® ICH4. This field is programmed by the BIOS after it has enumerated the processors and before it has enabled Stop Clock generation in the ICH4. Once this field has been set, it should not be modified. Note that each enabled thread within each processor will generate Stop Grant Acknowledge transactions. Note that this register is read/write and not Write-once as in some implementations. 00 = HI_A Stop Grant generated after 1 System Bus Stop Grant 01 = HI_A Stop Grant generated after 2 System Bus Stop Grant 10 = HI_A Stop Grant generated after 3 System Bus Stop Grant 11 = HI_A Stop Grant generated after 4 System Bus Stop Grant
12:10		Reserved
9	0b R/W	**Aperture Access Global Enable (APEN).** This bit is used to prevent access to the graphics aperture from any port (processor, HI_A, HI_B, or, AGP) before the aperture range is established by the configuration software and appropriate translation table in the main memory has been initialized. Since the default value is 0, this field must be set after the system is fully configured to enable aperture accesses. Set by Drivers.
8:6		Reserved
5	0b R/W	**MDA Present (MDAP).** This bit works with the VGA enable bits in the BCTRL registers of devices 2–4 to control the routing of processor-initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if none of the VGA enable bits are set. If none of the VGA enable bits are set, then accesses to I/O address range x3BCh–x3BFh are forwarded to HI_A. If the VGA enable bit is not set, then accesses to I/O address range x3BCh–x3BFh are treated just like any other I/O accesses. That is, the cycles are forwarded to HI_B if the address is within the corresponding IOBASE and IOLIMIT and ISA enable bit is not set; otherwise, they are forwarded to HI_A. MDA resources are defined as the following: Memory: 0B0000h–0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A15:10 are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to hub interface even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: **VGA MDA Behavior** 0 1 All References to MDA and VGA go to HI_A 0 1 Illegal Combination (DO NOT USE) 1 0 All References to VGA go to device with VGA enable set. MDA-only references (I/O address 3BF and aliases) will go to HI_A. 1 1 VGA References go to the HI which has its BCTRL3 bit set; MDA references go to HI_A

Bits	Default, Access	Description
4	0b R/W	**Throttled-Write Occurred.** 0 = This bit is cleared by writing a 0 to it. 1 = This bit is set when a write is throttled. This bit is set when the maximum allowed number of writes has been reached during a time-slice and there is at least one more write to be done.
3	0b R/W	**Throttled-Read Occurred.** 0 = This bit is cleared by writing a 0 to it. 1 = This bit is set when a read is throttled. This bit is set when the maximum allowed number of reads has been reached during a time-slice and there is at least one more read to be done.
2	1b RO loaded from HA7# on RESET#	**In-Order Queue Depth (IOQD).** This bit reflects the value sampled on HA7# on the deassertion of the CPURST#. It indicates the depth of the processor bus in-order queue (i.e., level of processor bus pipelining). 0 = When IOQD is set to 0 (HA7# is sampled asserted; i.e., 1; or an electrical low), the depth of the IOQ is set to 1 (i.e., no pipelining support on the processor bus). HA7# may be driven low during CPURST# by an external source. 1 = When IOQD is set to 1 (HA7# sampled as 0; an electrical high), the depth of the processor bus in-order queue is configured to the maximum allowed by the processor protocol (i.e., 12).
1:0		Reserved

3.5.16 PAM[0:6]—Programmable Attribute Map Registers (D0:F0)

Address Offset: 59–5Fh (PAM0–PAM6)
Default Value: 00h
Access: R/W
Size: 8 bits each

The MCH allows programmable memory attributes on 13 *legacy* memory segments of various sizes in the 768 KB to 1 MB address range. Seven Programmable Attribute Map (PAM) Registers support these features. However, not all seven of these registers are identical. PAM 0 controls only one segment (high), while PAM 1:6 controls two segments (high and low) each. Cacheability of these areas is controlled via the MTRR Registers in the processor. Two bits are used to specify memory attributes for each memory segment. These bits only apply to host initiator access to the PAM areas. The MCH forwards to main memory any Hub Interface_A–B initiated accesses to the PAM areas. At the time that hub interface accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable. It is illegal to issue a hub initiated transaction to a PAM region with the associated PAM register not set to 11. Each of these regions has a 2-bit field. The two bits that control each region have the same encoding.

As an example, consider BIOS that is implemented on the expansion bus. During the initialization process, BIOS can be shadowed in main memory to increase the system performance. When BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The host then does a write of the same address, which is directed to main memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus. Table 3-3and Figure 3-1 show the PAM Registers and the associated attribute bits:

Bits	Default, Access	Description
7:6		Reserved
5:4	00b R/W	**Attribute Register (HIENABLE).** This field controls the steering of read and write cycles that address the BIOS. 00 = DRAM Disabled - All accesses are directed to HI_A 01 = Read Only - All Reads are serviced by DRAM. All Writes are forwarded to HI_A. 10 = Write Only - All writes are sent to DRAM. Reads are serviced by HI_A. 11 = Normal DRAM operation - All reads and writes are serviced by DRAM
3:2		Reserved
1:0	00b R/W	**Attribute Register (LOENABLE).** This field controls the steering of read and write cycles that address the BIOS. 00 =DRAM Disabled - All accesses are directed to HI_A 01 =Read Only - All Reads are serviced by DRAM. All Writes are forwarded to HI_A. 10 =Write Only - All writes are sent to DRAM. Reads are serviced by HI_A. 1 1 =Normal DRAM operation - All reads and writes are serviced by DRAM **NOTE:** The LO Segment for PAM0 is reserved as shown in Figure 3-1.

Figure 3-1. PAM Registers

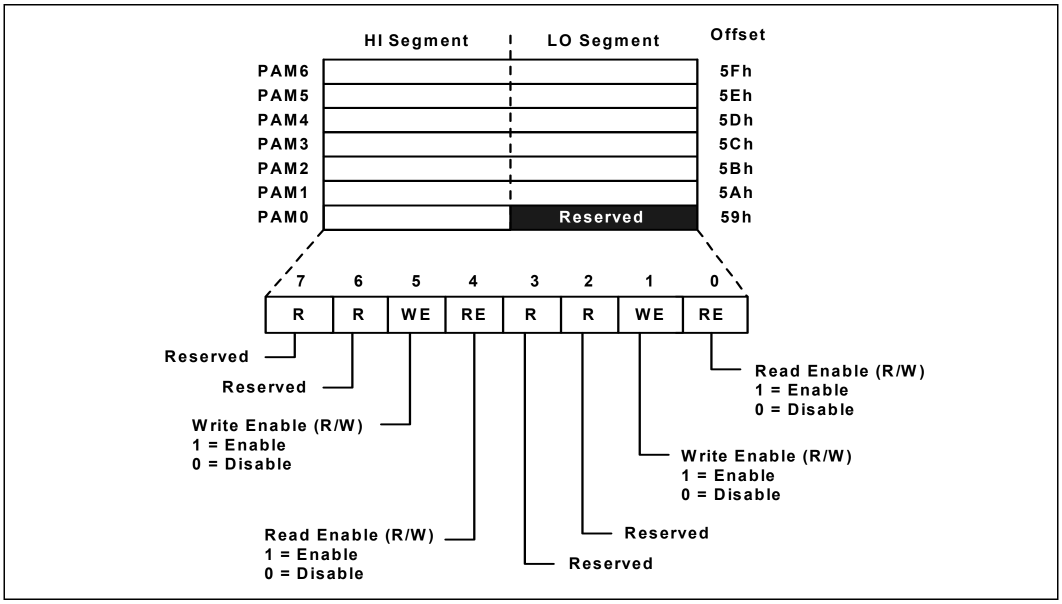


Table 3-3. PAM Associated Attribute Bits

PAM Reg	Attribute Bits				Memory Segment	Comments	Offset
PAM0 3:0, 7:6	Reserved				—	—	59h
PAM0 5:4	R	R	WE	RE	0F0000h–0FFFFFh	BIOS Area	59h
PAM1 3:2, 7:6	—	—	—	—	—	Reserved	5Ah
PAM1 1:0	R	R	WE	RE	0C0000h–0C3FFFh	BIOS Area	5Ah
PAM1 5:4	R	R	WE	RE	0C4000h–0C7FFFh	BIOS Area	5Ah
PAM2 3:2, 7:6	—	—	—	—	—	Reserved	5Bh
PAM2 1:0	R	R	WE	RE	0C8000h–0CBFFFh	BIOS Area	5Bh
PAM2 5:4	R	R	WE	RE	0CC000h–0CFFFFh	BIOS Area	5Bh
PAM3 3:2, 7:6	—	—	—	—	—	Reserved	5Ch
PAM3 1:0	R	R	WE	RE	0D0000h–0D3FFFh	BIOS Area	5Ch
PAM3 5:4	R	R	WE	RE	0D4000h–0D7FFFh	BIOS Area	5Ch
PAM4 3:2, 7:6	—	—	—	—	—	Reserved	5Dh
PAM4 1:0	R	R	WE	RE	0D8000h–0DBFFFh	BIOS Area	5Dh
PAM4 5:4	R	R	WE	RE	0DC000h–0DFFFFh	BIOS Area	5Dh
PAM5 3:2, 7:6	—	—	—	—	—	Reserved	5Eh
PAM5 1:0	R	R	WE	RE	0E0000h–0E3FFFh	BIOS Extension	5Eh
PAM5 5:4	R	R	WE	RE	0E4000h–0E7FFFh	BIOS Extension	5Eh
PAM6 3:2, 7:6	—	—	—	—	—	Reserved	5Fh
PAM6 1:0	R	R	WE	RE	0E8000h–0EBFFFh	BIOS Extension	5Fh
PAM6 5:4	R	R	WE	RE	0EC000h–0EFFFFh	BIOS Extension	5Fh

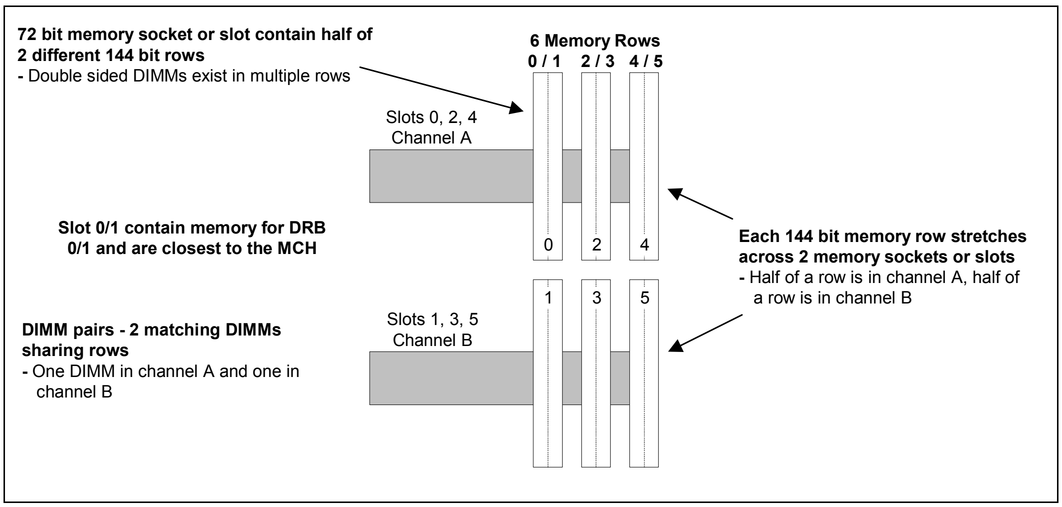
3.5.17 DRB—DRAM Row Boundary Register (D0:F0)

Address Offset: 60–67h (DRB[0:7])
Default Value: 00h
Attribute: RO
Size: 8 bits x 8 registers

The DRAM Row Boundary registers defines the upper boundary address of each DRAM row with a granularity of 64 MB. Each row has its own single-byte DRB register. For example, a value of 1 in DRB0 indicates that 64 MB of DRAM has been populated in the first row. In this mode a row spans across both DIMMs.

Bits	Default, Access	Description
7:0	00h R/W	**DRAM Row Boundary Address.** This 8-bit value defines the upper address for each of the DRAM rows. This 8-bit value is compared against a set of address lines to determine the upper address limit of a particular row. This field corresponds to bits 33:26 of the address. A DRAM row is addressed if the address is below the row's DRAM Row Boundary Address and greater than or equal to the previous row's DRAM Row Boundary Address.

Figure 3-2. Memory Socket Rows Description



DIMM PAIR	Even Row (or Single Sided)		Odd row (Present if Double-Sided)	
	Row Number	Address of DRB	Row Number	Address of DRB
DIMM 1	Row 0	60h	Row 1	61h
DIMM 2	Row 2	62h	Row 3	63h
DIMM 3	Row 4	64h	Row 5	65h
DIMM 4	Row 6	66h	Row 7	67h

DRB0 = Total memory in row0 (in 64-MB increments)

DRB1 = Total memory in row0 + row1 (in 64-MB increments)

...

DRB7 = Total memory in row0 + row1 + row2 + row3 + row4 + row5 + row6 + row7 (in 64-MB increments)

The row referred to by this register is defined by the DIMM chip select used. Double-sided DIMMs use both Row0 and Row1 (for CS0# and CS1#, even though there is one physical slot for the row. Single-sided DIMMs use only the even row number, since single-sided DIMMs only support CS0#. For single-sided DIMMs the value BIOS places in the odd row should equal the same value as what was placed in the even row field. A row is the 128-b wide interface consisting of two identical DIMMs.

- Unpopulated rows must be programmed with the value of the last populated row.
- If 16 GB are populated, then the present definition does not allow the full 16 GB to be accessed. The maximum DRAM addressing is 16 GB–64 MB.

Programming Example:

DIMM1	256 MB in even row, none in odd row (single sided DIMM)
DIMM2	512 MB in even row, 512M in odd row (double sided DIMM)
DIMM3	128 MB in even row, none in odd row (single sided DIMM)
DIMM4	256 MB in even row, 256M in odd row (double sided DIMM)

Address	Row	Size of Row	Accumulative Size	Register Value
60h	Row 0 (DIMM 1, even)	256 M	256 M	04h
61h	Row 1 (DIMM 1, odd)	empty	256 M	04h
62h	Row 2 (DIMM 2, even)	512 M	768 M	0Ch
63h	Row 3 (DIMM 2, odd)	512 M	1280 M	14h
64h	Row 4 (DIMM 3, even)	128 M	1408 M	16h
65h	Row 5 (DIMM 3, odd)	empty	1408 M	16h
66h	Row 6 (DIMM 4, even)	256M	1664 M	1A
67h	Row 7 (DIMM 4, odd)	256M	1920 M	1E

3.5.18 DRA—DRAM Row Attribute Register (D0:F0)

Address Offset:	70–73h
Default Value:	00h
Attribute:	RO, R/W
Size:	8 bits x 4 registers

The DRAM Row Attribute register defines the page sizes to be used for each row of memory. Each nibble of information in the DRA registers describes the page size of a row. For this register, a row is defined by the chip select used by the DIMM; thus, a double-sided DIMM has both an even and an odd entry. For single-sided DIMMs, only the even side is used.

DRA	Bits	Row	DRB
70h	3:0	Row0	DRB0
	7:4	Row1	DRB1
71h	3:0	Row2	DRB2
	7:4	Row3	DRB3
72h	3:0	Row4	DRB4
	7:4	Row5	DRB5
73h	3:0	Row6	DRB6
	7:4	Row7	DRB7

Bits	Default, Access	Description
7	0b R/W	**ODD Device Width.** This bit defines the width of the DDR-SDRAM devices populated in this row. This bit is used in the mapping of DQS signals to DQ signals, in the DDR-SDRAM receive path. 0 = x8 or x16 DIMMs 1 = x4 DIMMs.
6:4	000b R/W	**ODD Row Attribute for Odd-numbered Row.** This 3-bit field defines the page size of the corresponding row. 000 = Reserved 001 = 4 KB 010 = 8 KB 011 = 16 KB 100 = 32 KB 101 = 64 KB 11x = Reserved
3	0b R/W	**Even Device Width.** This bit defines the width of the DDR-SDRAM devices populated in this. This bit field is used in the mapping of DQS signals to DQ signals in the DDR-SDRAM receive path. 0 = x8 or x16 DIMMs 1 = x4 DIMMs.
2:0	000b R/W	**Even Row Attribute for Even-numbered Row.** This 3-bit field defines the page size of the corresponding row. 000 = Reserved 001 = 4 KB 010 = 8 KB 011 = 16 KB 100 = 32 KB 101 = 64 KB 11x = Reserved

3.5.19 DRT—DRAM Timing Register (D0:F0)

Address Offset: 78–7Bh
Default Value: 0000 0010h
Attribute: RO, R/W
Size: 32 bits

This register controls the timing of the DRAM Controller.

<table>
<tr><th>Bits</th><th>Default, Access</th><th>Description</th></tr>
<tr><td>31:30</td><td></td><td>Reserved</td></tr>
<tr><td>29</td><td>0b
R/W</td><td>Back To Back Write-Read Turn Around. This field determines the minimum number of CMDCLK (command clocks, at 100 MHz) between Write-Read commands. It applies to WR-RD pairs to different rows. A WR-RD pair to the same row has sufficient turnaround due to the tWTR timing parameter. The purpose of this bit is to control the turnaround time on the DQ bus.
0 = 3 clocks between WR-RD commands (2 turnaround clocks on DQ)
1 = 2 clock between WR-RD commands (1 turnaround clock on DQ)

NOTE: The bigger turn-around is used in large configurations where the difference in total channel delay between the fastest and slowest DIMM is large.</td></tr>
<tr><td>28</td><td>0b
R/W</td><td>Back To Back Read-Write Turn Around. This field, along with bit 15 of the REROTC register (offset 80–81h), determines the minimum number of CMDCLK (command clocks, at 100/133 MHz) between Read-Write commands. It applies to RD-WR pairs to any destination (in same or different rows). The purpose of this bit is to control the turnaround time on the DQ bus.

<table><tr><th>DRT bit 28</th><th>REROTC bit 15</th><th>Description</th></tr><tr><td>0</td><td>1</td><td>6 (8) clocks between RD-WR commands</td></tr><tr><td>0</td><td>0</td><td>5 (7) clocks between RD-WR commands</td></tr><tr><td>1</td><td>1</td><td>5 (7) clocks between RD-WR commands</td></tr><tr><td>1</td><td>0</td><td>4 (6) clocks between RD-WR commands</td></tr></table>
NOTES:
1. Number in parenthesis is for single channel operation.
2. The bigger turn-around is used in large configurations where the difference in total channel delay between the fastest and slowest DIMM is large.</td></tr>
<tr><td>27</td><td>0b
R/W</td><td>Back To Back Read Turn Around. This field determines the minimum number of CMDCLK (command clocks, at 100 MHz) between two Reads to different rows. The purpose of this bit is to control the turnaround time on the DQ bus.
0 = 4 clocks between RD commands to different rows (2 turnaround clocks on DQ)
1 = 3 clocks between RD commands to different rows (1 turnaround clock on DQ)

NOTE: The bigger turn-around is used in large configurations where the difference in total channel delay between the fastest and slowest DIMM is large.</td></tr>
</table>

Bits	Default, Access	Description
26:24	000b R/W	**Read Delay (t_{RD}).** This t_{RD} value represents the time elapsed from the internal DCLK rising (for which command is sent) until HCLK rising for which initial SB data is driven (and the data can be read from the DDR receive FIFO). **Parameter** / **Min** / **Max** DCLK to CK rising / 5 ns / 5 ns CAS Latency / 15 ns / 25 ns DIMM type / 0 ns / 10 ns CH DLY / 0 ns / 10 ns t_{PD} / 0 ns / 10 ns Even Odd arrival / 5 ns / 5 ns t_{RD} (Round number to integer number) / 30 ns / 70 ns **CAS# Latency** / **Registered DIMM** t_{RD}**min**, t_{RD}**max** / **Unbuffered DIMM** t_{RD}**min**, t_{RD}**max** 2 / 5 / 7 / 4 / 6 2.5 / 5 / 7 / 4 / 7 **Encoding** / t_{RD} **100 MHz** / t_{RD} **133 MHz** / **Clocks** 000 / 70 ns / 52.5 ns / 7 001 / 60 ns / 45 ns / 6 010 / 50 ns / 37.5 ns / 5 011 / 40 ns / 30 ns / 4 100 / 30 ns / 22.5 ns / 3 101 / 80 ns / 60 ns / 8 110 / 90 ns / 67.5 ns / 9 111 / reserved / reserved / reserved
23:19		Reserved
18:16	000b R/W	**DRAM Idle Timer.** This field determines the number of clocks the DRAM controller will remain in the idle state before it begins precharging all pages. 000 = Infinite 001 = 0 010 = 8 DRAM clocks 011 = 16 DRAM clocks 100 = 64 DRAM clocks Others = Reserved
15:11		Reserved
10:9	00b R/W	**Activate to Precharge delay (t_{RAS}).** This bit controls the number of DRAM clocks for t_{RAS}. 00 = 7 Clocks 01 = 6 Clocks 10 = 5 Clocks 11 = Reserved
8:6		Reserved

Bits	Default, Access	Description
5:4	01b R/W	**CAS# Latency (t_{CL}).** The number of clocks between the rising edge used by DRAM to sample the Read Command and the rising edge that is used by the DRAM to drive read data. 00 = 2.5 01 = 2 10 = Reserved 11 = Reserved
3	0b R/W	**Write RAS# to CAS# Delay (t_{RCD}).** This bit controls the number of clocks inserted between a row activate command and a write command to that row. 0 = 3 DRAM Clocks 1 = 2 DRAM Clocks

2:1	00b
	R/W
		READ RAS# to CAS# Delay (t_{RCD}). This bit controls the number of clocks inserted between a row activate command and a read command to that row.
		00 = 5 DRAM clocks
		01 = 4 DRAM clocks
		10 = 3 DRAM clocks
		11 = 2 DRAM clocks
		Note that t_{RCD} is first expanded (beyond 2,3 clocks options), to correctly support $t_{RAS\text{-}min}$ timing during auto-precharge cycles. Also, note that t_{RCD} is separated between reads and writes, since slower timing (with auto-precharge) is needed for read cycles only. The following tables should be used by BIOS to correctly set t_{RCD}, based on DDR-SDRAM speed, CAS Latency, and whether auto-precharge is enabled for read cycles.
		Case 1: DDR200, t_{RAS} = 5 clocks (50 ns).
		
		  Without AP **With AP**
		RD-RCD 2 3
		WR-RCD 2 2
		
		Case 2: DDR266, t_{RAS} = 6 clocks (45 ns).
		
		  Without AP **With AP**
		RD-RCD 3 4
		WR-RCD 3 3

0	0b R/W	**DRAM RAS# Precharge (t_{RP}).** This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same row. 0 = 3 DRAM clocks 1 = 2 DRAM clocks

3.5.20 DRC—DRAM Controller Mode Register (D0:F0)

Address Offset: 7C–7Fh
Default Value: 0044_0009h
Attribute: RO, R/W
Size: 32 bits

Bits	Default, Access	Description
31:30	00b RO	**Revision Number (REV).** This field reflects the revision number of the format used for SDR/DDR register definition.
29	0b R/W	**Initialization Complete (IC).** This bit is used for communication of software state between the memory controller and the BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete. Note the following: • Periodic refresh will not start until this bit is set. • tRC timing counter is not enabled until this bit is set.
28:22		Reserved
21:20	00b	**DRAM Data Integrity Mode (DDIM).** These bits select one of 4 DRAM data integrity modes. **DDIM** **Operation** 00 Non-ECC mode, no ECC correction is done and no errors are flagged in FERR or NERR 01 Reserved 10 Error checking, with correction 11 Reserved
19:18		Reserved
17	0b R/W	**Fast CS# Enable (FCSEN).** This bit enables/disables Fast CS# mode. 0 = Disable. 1 = Enable. When set to 1, and when the DRAM interface is idle, CS# is asserted in the same time the DRAM tracking transitions to active state. This mode of operation reduces leadoff access latency by one clock and is used in selected configurations (with light loads on address and command lines).
16	0b R/W	**Command Per Clock- Address/Control Assertion Rule (CPC).** This bit defines the number of clock cycles the MA, RAS#, CAS#, WE# are asserted. 0 = 2n rule: (MAx:x, RAS#, CAS#,WE# asserted for 2 clock cycles 1 = 1n rule: (MAx:x, RAS#, CAS#,WE# asserted for 1 clock cycles
13	0b R/W	**Auto-Precharge for Read Enable (APR).** 0 = Disable. All reads are sent without auto-precharge 1 = Enable. All reads are sent with Auto-precharge attribute attached.
12	0b R/W	**Auto-Precharge for Write Enable (APW).** 0 = Disable. All writes commands are sent without auto-precharge. 1 = Enable. All write commands are sent with auto-precharge attribute attached.
11		Reserved
10:8	000b R/W	**Refresh Mode Select (RMS).** This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. 000 = Disable 001 = Enable. Refresh interval 15.6 µs 010 = Enable. Refresh interval 7.8 µs 011 = Enable. Refresh interval 64 µs 111 = Enable. Refresh interval 64 clocks (fast refresh mode) Others = Reserved
7		Reserved

Bits	Default, Access	Description
6:4	000b R/W	**Mode Select (SMS).** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. When this field is first set to a non-zero value, the DRBs must be set to properly indicate which ranks are populated, since this information is latched shortly after a non-zero value is first written. DRBs can be changed later to adjust the rank addresses. A rank that is indicated as not populated when this field is first written to a non-zero value cannot be changed to populate later. It should be noted that some of the MA lines (MA[11:7]) are mapped to two possible HA bits depending on the installed memory configuration (specifically the page size programmed for the row in the DRA registers). 000 Post Reset State: In this mode CKEs are deasserted and the DRAMS are in self-refresh mode. All other combinations of SMS bits results in assertion of one or more CKEs, except when the device is in C3, or S1 state, where all devices are in self-refresh, without regard to the value in SMS. 001 NOP Command Enable: All Processor cycles to DRAM result in a NOP command on the DRAM interface. 010 All Banks Pre-charge Enable: All processor cycles to DRAM result in an “all banks precharge” command on the DRAM interface. 011 Mode Register Set Enable: All processor cycles to DRAM result in a “mode register” set command on the DRAM interface. Host address lines are mapped to SDRAM address lines in order to specify the command sent. Host address lines [15:3] are mapped to MA[12:0]. 100 Extended Mode Register Set Enable: All processor cycles to SDRAM result in an “extended mode register set” command on the DRAM interface (DDR only). Host address lines are mapped to SDRAM address lines in order to specify the command sent. Host address lines [15:3] are mapped to MA[12:0]. 101 Reserved. 110 CBR Refresh Enable: In this mode all processor cycles to DRAM result in a CBR cycle on the SDRAM interface. 111 Normal operation
3	1b R/W	**Registered DIMM Mode Enable (REGD).** This bit indicates whether the system has been populated entirely with registered DIMMs or unbuffered DIMMs. The MCH supports either registered or unbuffered DIMMs. Note that the specification does not support mixing of un-buffered DIMMs and registered DIMMs. 0 = All rows are populated with unbuffered DIMMs. 1 = All rows populated with registered DIMMs
2		Reserved
1:0	01b RO	**DRAM Type (DT).** This field is used to select between supported SDRAM types. This is a read only bit in the MCH. 01 = Dual data rate SDRAM All Others = Reserved

3.5.21 REROTC—Receive Enable Reference Output Timing Control Register (D0:F0)

Address Offset: 80–81h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bits	Default, Access	Description
15	0b R/W	**Increase Read/Write Turnaround Margin.** Total turnaround margin is controlled by this field in addition to the back-to-back read write turnaround control (bit 28) of the DRAM Timing Register. It is expected that extra margin will be required for 266 MHz DDR operation with CAS Latency of 2.5 and would increase the total delay between commands to 6 clocks from 5. 0 = No extra turnaround margin between read and write cycles. 1 = Add 1 DCLK of turnaround margin between read and write cycles.
14:0		Reserved

3.5.22 CLOCK_DIS—CK/CK# Clock Disable Register (D0:F0)

Address Offset: 8Ch
Default Value: FFh
Attribute: R/W
Size: 8bit

<table>
<tr><th>Bits</th><th>Default, Access</th><th>Description</th></tr>
<tr><td>7:0</td><td>FFh
R/W</td><td>CK/CK# Disable. Each bit corresponds to a CK/CK# pair of pins on each channel. Bit 0 corresponds to CK0 and CK0# while bit 5 corresponds to CK5 and CK5#. When set to 1, these bits turn off the corresponding CK/CK# pair on both channels. CK is driven low and CK# is driven high. This feature is intended to reduce EMI due to clocks toggling to DIMMs which are not populated.
The table below shows how the clock pins are used on the two main motherboard types.
<table>
<tr><th>Bit</th><th>Pins</th><th>Registered</th><th>Unbuffered MB</th></tr>
<tr><td>7</td><td>CMDCLK x7
CMDCLK x7#</td><td>Not Used. Pins become chip selects</td><td>DIMM1 CK2/CK2#</td></tr>
<tr><td>6</td><td>CMDCLK x6
CMDCLK x6#</td><td>Not Used. Pins become chip selects</td><td>DIMM0 CK2/CK2#</td></tr>
<tr><td>5</td><td>CMDCLK x5
CMDCLK x5#</td><td>Not Used</td><td>DIMM1 CK1CK1#</td></tr>
<tr><td>4</td><td>CMDCLK x4
CMDCLK x4#</td><td>Not Used</td><td>DIMM0 CK1/CK1#</td></tr>
<tr><td>3</td><td>CMDCLK x3
CMDCLK x3#</td><td>DIMM3 CK0/CK0#</td><td>Not Used</td></tr>
<tr><td>2</td><td>CMDCLK x2
CMDCLK x2#</td><td>DIMM2 CK0/CK0#</td><td>Not Used</td></tr>
<tr><td>1</td><td>CMDCLK x1
CMDCLK x1#</td><td>DIMM1 CK0/CK0#</td><td>DIMM1 CK0CK0#</td></tr>
<tr><td>0</td><td>CMDCLK x0
CMDCLK x0#</td><td>DIMM0 CK0/CK0#</td><td>DIMM0 CK0CK0#</td></tr>
</table></td></tr>
</table>

3.5.23 DDR_CNTL—DDR Memory Control Register (D0:F0)

Address Offset: 8Eh
Default Value: 00xx 0000b
Attribute: RO, R/W
Size: 8 bits

Bits	Default, Access	Description
7	0b R/W	**DDR Refresh Frequency.** This bit is set by the BIOS to the DDR refresh frequency. It is used by the refresh timer to set the refresh period properly according to the number of clocks per microsecond. This is an indicator bit to the DDR logic only. It does **not** change the DDR frequency. 0 = 100 MHz (200 MHz data rate) 1 = 133 MHz (266 MHz data rate).
6:5		Reserved
4	x RO	**DRAM Strap, latched.** This bit provides the value of the DRAM strap pin, latched at reset. It is used to determine the motherboard type. 0 = Registered only motherboard 1 = Unbuffered DIMM support.
3		Reserved
2	0b R/W	**CS# / Clock Muxing.** This bit determines whether the multiplexed DRAM pins are used as clocks or chip selects. See the pin description for the specific muxing. 0 = CS_x[5:4] are output on the multiplexed pins. Used on third DIMM slot on registered (only) mother board.
1:0		Reserved

3.5.24 SMRAM—System Management RAM Control Register (D0:F0)

Address Offset: 9Dh
Default Value: 02h
Attribute: RO, R/W
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the Lock bit is set.

Bits	Default, Access	Description
7		Reserved
6	0b R/W	**SMM Space Open (D_OPEN).** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	0b R/W	**SMM Space Closed (D_CLS).** When D_CLS = 1, SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This allows SMM software to reference through SMM space to update the display, even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. **NOTE:** D_CLS only applies to Compatible SMM space.
4	0b R/W	**SMM Space Locked (D_LCK).** When D_LCK is set to 1, D_OPEN is reset to 0 and D_LCK, D_OPEN, G_SMRARE, H_SMRAME, TSEG_SZ and T_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	0b R/W/L	**Global SMRAM Enable (G_SMRARE).** When this bit is 1, Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADS# with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details. **NOTE:** Once D_LCK is set, this bit becomes read only.
2:0	010b RO	**Compatible SMM Space Base Segment (C_BASE_SEG).** This field indicates the location of SMM space. SMM DRAM is not remapped. It is made visible if the conditions are right to access SMM space; otherwise, the access is forwarded to the hub interface. Since the MCH supports only the SMM space between A0000h and BFFFFh, this field is hardwired to 010.

3.5.25 ESMRAMC—Extended System Management RAM Control Register (D0:F0)

Address Offset: 9Eh
Default Value: 38h
Attribute: RO, R/W/L, R/WC
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bits	Default, Access	Description
7	0b R/W/L	**Enable High SMRAM (H_SMRAME).** This bit controls the SMM memory space location (i.e., above 1 MB or below 1 MB) 0 = Disable. 1 = Enable. When G_SMRAME is 1 and H_SMRAME is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA_0000h to 0FEDA_FFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. **NOTE:** Once D_LCK is set, this bit becomes read only.
6	0b R/WC	**Invalid SMRAM Access (E_SMERR).** 1 = This bit is set when processor has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. **NOTE:** The software must write a 1 to this bit to clear it.
2:1	00b R/W/L	**TSEG Size (TSEG_SZ).** This field selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space (TOLM – TSEG_SZ) to TOLM is partitioned away so that it may only be accessed by the processor interface, and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to the hub interface when the TSEG memory block is enabled. 00 = (TOLM–128 KB) to TOLM 01 = (TOLM – 256 KB) to TOLM 10 = (TOLM – 512 KB) to TOLM 11 = (TOLM – 1 MB) to TOLM **NOTE:** Once D_LCK is set, these bits become read only.
0	0b R/W/L	**TSEG Enable (TSEG_EN).** Enabling of SMRAM memory for Extended SMRAM space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. **NOTE:** Once D_LCK is set, this bit becomes read only.

3.5.26 ACAPID—AGP Capability Identifier Register (D0:F0)

Address Offset: A0–A3h
Default Value: 0030 0002h
Attribute: RO
Size: 32 bits

This register provides the standard identifier for AGP capability. **Read by drivers.**

Bits	Default, Access	Description
31:24		Reserved
23:20	3h RO	**Major AGP Revision Number (MAJREV).** These bits provide a major revision number of AGP specification to which this version of MCH conforms. This field is hardwired to value of 0011b (i.e., implying *AGP Specification 3.0*).
19:16	0h RO	**Minor AGP Revision Number (MINREV).** These bits provide a minor revision number of AGP specification to which this version of MCH conforms. This number is hardwired to value of 0000 which implies that the revision is x.0. Together with major revision number this field identifies the MCH as an *AGP Specification 2.0* compliant device.
15:8	00h RO	**Next Capability Pointer (NCAPTR).** AGP capability is the first and the last capability described via the capability pointer mechanism and therefore these bits are hardwired to 0s to indicate the end of the capability linked list.
7:0	02h RO	**AGP Capability ID (CAPID).** This field identifies the linked list item as containing AGP registers. This field has a value of 0000_0010b assigned by the PCI SIG.

3.5.27 AGPSTAT—AGP Status Register (D0:F0)

Address Offset: A4–A7h
Default Value: See table below
Attribute: RO
Size: 32 bits

This register reports AGP device capability/status. **Read by drivers.**

Bits	Default, Access	Description
31:24	1Fh RO	**Request Queue (RQ).** Hardwired to 1Fh. This field contains the maximum number of AGP command requests the MCH is configured to manage. 1Fh =32 outstanding AGP command requests maximum can be handled by the MCH.
23:16		Reserved
15:13	010b RO	**Async Request Size**. This value is LOG2 of the optimum asynchronous request size in bytes minus 4 to be used with the MCH. 2h = 64 byte MCH cache line size.
12:10	000b RO	**MCH Bus Period for I/O Buffer Calibration.** 000 = 4 ms
9	1b RO	**Side Band Addressing Support (SBA).** Hardwired to 1. The MCH supports side band addressing.
8:7		Reserved
6	0 RO	**Host Translation Support (HTRANS#).** Hardwired to 0. The MCH supports translating accesses from the host processor through the aperture.

<table>
<tr><th>Bits</th><th>Default, Access</th><th>Description</th></tr>
<tr><td>5</td><td>0b
RO</td><td>Greater Than Four Gigabyte Support (GT4GIG). Hardwired to 0. The MCH does not support addresses greater than 4 GB.</td></tr>
<tr><td>4</td><td>1b
RO</td><td>Fast Write Support (FW). Hardwired to a 1. The MCH supports Fast Writes from the processor to the AGP master. It is</td></tr>
<tr><td>3</td><td>xb
RO</td><td>AGP 3.0 Signaling Mode. This bit is set by the hardware on reset based on the AGP 8x detection via the VREF Comparator.
0 = AGP 2.0 signaling mode (1.5 V).
1 = Graphics card is AGP 8x mode.</td></tr>
<tr><td>2:0</td><td>111b or 01xb
RO</td><td>Data Rate Support (RATE). The value of this field is determined by the AGP 3.0 signaling mode bit above.
In AGP 3. 0 signaling mode (AGP 3.0 signaling mode bit = 1), these bits are 01X, indicating that 8x mode is supported. A 1 indicates that the 4x data rate is supported in 8x mode.
In AGP 2.0 signaling mode, these bits are 111 indicating that 1x, 2x, and 4x modes are all supported.
<table>
<tr><th>2.0 Signaling (1.5 V)</th><th>Bit 2</th><th>Bit 1</th><th>BIt 0</th></tr>
<tr><td>Data Rate</td><td>4x</td><td>2x</td><td>1x</td></tr>
<tr><td>MCH Value</td><td>1 (supported)</td><td>1 (supported)</td><td>1 (supported)</td></tr>
</table>
<table>
<tr><th>3.0 Signaling (0.8 V)</th><th>Bit 2</th><th>Bit 1</th><th>BIt 0</th></tr>
<tr><td>Data Rate</td><td>reserved</td><td>8x</td><td>4x</td></tr>
<tr><td>MCH value</td><td>0</td><td>1 (supported)</td><td>Programmable by BIOS</td></tr>
</table>
Signaling mode is determined by bit 3 (AGP 3.0 signaling mode bit) above.</td></tr>
</table>

3.5.28 AGPCMD—AGP Command Register (D0:F0)

Address Offset: A8–ABh
Default Value: 0000 0000h
Attribute: R/W
Size: 32 bits

This register provides control of the AGP operational parameters. **Set by drivers.**

Bits	Default, Access	Description
31:13		Reserved
12:10	000b RO	**Programmed Calibration Period (PCAL_Cycle).** 000 = 4 ms
9	0b R/W	**Side Band Addressing Enable (SBAEN).** 0 = Disable. 1 = Enable. In AGP 3.0 signaling mode this bit is ignored as sideband addressing is the only allowed mechanism.
8	0b R/W	**AGP Enable (AGPEN).** 0 = Disable. MCH ignores all AGP. operations, including the sync cycle. Any AGP operations received while this bit is set to 1 will be serviced even if this bit is reset to 0. If this bit transitions from a 1 to a 0 on a clock edge in the middle of an SBA command being delivered in 1x mode the command will be issued. 1 = Enable. MCH responds to AGP. operations delivered via PIPE#, or to operations delivered via SBA if the AGP side band enable bit is also set to 1.
7:6		Reserved
5	0b RO	**Greater Than Four Gigabyte Enable (GT4GIG).** Hardwired to 0. The MCH, as an AGP target, does not support addressing greater than 4 GB.
4	0b R/W	**Fast Write Enable (FWEN).** 0 = Disable. When this bit is 0 or the data rate bits are set to 1x mode, the memory write transactions from the MCH to the AGP master uses standard PCI protocol. 1 = Enable. MCH uses the Fast Write protocol for memory write transactions from the MCH to the AGP master. Fast Writes will occur at the data transfer rate selected by the data rate bits (2:0) in this register.
3		Reserved
2:0	000b R/W	**Data Rate Enable (DRATE).** The setting of these bits determines the AGP data transfer rate. One (and only one) bit in this field must be set to indicate the desired data transfer rate. The same bit must be set on both master and target.The encoding is determined by the AGP 3.0 signaling mode bit in the AGPSTAT register. **Encoding** / **AGP Specification 2.0 Signaling** / **AGP Specification 3.0 Signaling** 001 / 1x Transfer Mode / 4x Transfer Mode 010 / 2x Transfer Mode / 8x Transfer Mode 100 / 4x Transfer Mode / reserved

3.5.29 AGPCTRL—AGP Control Register (D0:F0)

Address Offset: B0–B3h
Default Value: 0000 0000h
Attribute: RO, R/W
Size: 32 bits

This register provides for additional control of the AGP interface. **Set by drivers**

Bits	Default, Access	Description
31:8		Reserved
7	0b R/W	**GTLB Enable (GTLBEN).** 0 = Disable. The GTLB is flushed by clearing the valid bits associated with each entry. In this mode of operation all accesses that require translation bypass the GTLB. All requests that are positively decoded to the graphics aperture force the MCH to access the translation table in main memory before completing the request. Translation table entry fetches will not be cached in the GTLB. When an invalid translation table entry is read, this entry will still be cached in the GTLB (ejecting the least recently used entry). 1 = Enable. Normal operations of the Graphics Translation look aside Buffer. **NOTE:** This bit can be changed dynamically (i.e., while an access to GTLB occurs); however, the completion of the configuration write that asserts or deasserts this bit will be delayed pending a complete flush of all dirty entries from the write buffer. This delay will be incurred because this bit is used as a mechanism to signal the chipset that the graphics aperture translation table is about to be modified or has completed modifications. In the first case, all dirty entries need to be flushed before the translation table is changed. In the second case, all dirty entries need to be flushed because one of them is likely to be a translation table entry which must be made visible to the GTLB by flushing it to memory.
6:0		Reserved

3.5.30 APSIZE—Aperture Size Register (D0:F0)

Address Offset: B4h
Default Value: 00h
Attribute: RO, R/W
Size: 8 bits

This register determines the effective size of the Graphics Aperture used for a particular MCH configuration. This register can be updated by the MCH-specific BIOS configuration sequence before the PCI standard bus enumeration sequence takes place. If the register is not updated, the default value will select an aperture of maximum size (i.e., 256 MB). The size of the table that will correspond to a 256-MB aperture is not practical for most applications; therefore, these bits must be programmed to a smaller practical value that will force adequate address range to be requested via APBASE register from the PCI configuration software. **Set by BIOS.**

Bits	Default, Access	Description
7:6		Reserved
5:0	00h R/W	**Graphics Aperture Size (APSIZE).** Each bit in APSIZE5:0 operates on similarly ordered bits in APBASE27:22 of the Aperture Base configuration register. When a particular bit of this field is 0, it forces the similarly ordered bit in APBASE27:22 to behave as “hardwired” to 0. When a particular bit of this field is set to 1, it allows corresponding bit of the APBASE27:22 to be read/write accessible. The default value (APSIZE5:0=000000b) forces the default APBASE27:22 to read as 000000b (i.e., all bits respond as hardwired to 0). This provides the maximum aperture size of 256 MB. As another example, programming APSIZE5:0 to 111000b hardwires APBASE24:22 to 000b and enables APBASE27:25 to be read/write programmable. 000000 = 256-MB Aperture Size 100000 = 128-MB Aperture Size 110000 = 64-MB Aperture Size 111000 = 32-MB Aperture Size 111100 = 16-MB Aperture Size 111110 = 8-MB Aperture Size 111111 = 4-MB Aperture Size

3.5.31 ATTBASE—Aperture Translation Table Register (D0:F0)

Address Offset: B8–BBh
Default Value: 0000 0000h
Attribute: R/W
Size: 32 bits

This register provides the starting address of the Graphics Aperture Translation Table (GART) Base located in the main memory. This value is used by the MCH's Graphics Aperture address translation logic (including the GTLB logic) to obtain the appropriate address translation entry required during the translation of the aperture address into a corresponding physical main memory address. The ATTBASE register may be dynamically changed. **Set by drivers.**

Bits	Default, Access	Description
31:12	0...0b R/W	**Aperture Translation Table Base (TTABLE).** This field contains a pointer to the base of the translation table used to map memory space addresses in the aperture range to addresses in main memory. Note that it should be modified only when the GTLB has been disabled.
11:0		Reserved

3.5.32 AMTT—AGP MTT Control Register (D0:F0)

Address Offset: BCh
Default Value: 00h
Attribute: RO, R/W
Size: 8 bits

AMTT is an 8-bit register that controls the amount of time that the MCH's arbiter allows AGP/PCI master to perform multiple back-to-back transactions. The MCH's AMTT mechanism is used to optimize the performance of the AGP master (using PCI semantics) that performs multiple back-to-back transactions to fragmented memory ranges (and as a consequence it can not use long burst transfers). The AMTT mechanism applies to the processor-AGP/PCI transactions as well and it assures the processor of a fair share of the AGP/PCI interface bandwidth.

The number of clocks programmed in the AMTT represents the guaranteed time slice (measured in 66 MHz clocks) allotted to the current agent (either AGP/PCI master or Host bridge) after which the AGP arbiter will grant the bus to another agent. The default value of AMTT is 00h and disables this function. The AMTT value can be programmed with 8-clock granularity. For example, if the AMTT is programmed to 18h, then the selected value corresponds to the time period of 24 AGP (66 MHz) clocks. **Set by BIOS.**

Bits	Default, Access	Description
7:3	00000b R/W	**Multi-Transaction Timer Count Value (MTTC).** The number programmed into these bits represents the time slice (measured in eight 66 MHz clock granularity) allotted to the current agent (either AGP/PCI master or Host bridge) after which the AGP arbiter will grant the bus to another agent.
2:0		Reserved

3.5.33 LPTT—AGP Low Priority Transaction Time Register (D0:F0)

Address Offset: BDh
Default Value: 00h
Attribute: R/W
Size: 8 bits

LPTT is an 8-bit register similar in function to AMTT. This register is used to control the minimum tenure on the AGP for low priority data transaction (both reads and writes) issued using PIPE# or SB mechanisms.

The number of clocks programmed in the LPTT represents the guaranteed time slice (measured in 66 MHz clocks) allotted to the current low priority AGP transaction data transfer state. This does not necessarily apply to a single transaction but it can span over multiple low-priority transactions of the same type. After this time expires, the AGP arbiter may grant the bus to another agent if there is a pending request. The LPTT does not apply in the case of high-priority request where ownership is transferred directly to high-priority requesting queue. The default value of LPTT is 00h and disables this function. The LPTT value can be programmed with 8-clock granularity. For example, if the LPTT is programmed to 10h, the selected value corresponds to the time period of 16 AGP (66 MHz) clocks. **Set by BIOS.**

Bits	Default, Access	Description
7:3	00h R/W	**Low Priority Transaction Timer Count Value (LPTTC).** The number of clocks programmed in these bits represents the time slice (measured in eight 66 MHz clock granularity) allotted to the current low priority AGP transaction data transfer state).
2:0		Reserved

3.5.34 TOLM—Top of Low Memory Register (D0:F0)

Address Offset: C4–C5h
Default Value: 0800h
Attribute: R/W
Size: 16 bits

This register contains the maximum address below 4 GB that should be treated as a memory access, and is defined on a 128-MB boundary. Usually, it will sit below the areas configured for hub interface and PCI memory and the graphics aperture. Note that the memory address found in DRB7 reflects the top of total memory. In the event that there is less than 4 GB of DRAM and PCI space in the system, these two registers will be identical.

Bits	Default, Access	Description
15:11	00001b R/W	**Top of Low Memory (TOLM).** This register contains the address that corresponds to bits 31 to 27 of the maximum main memory address that lies below 4 GB. Configuration software should set this value to either the maximum amount of memory in the system or to the minimum address allocated for PCI memory or the graphics aperture, whichever is smaller. Address bits 15:0 are assumed to be 0000h for the purposes of address comparison. Addresses equal to or greater than the TOLM, and less than 4 GB, are treated as accesses to HI. All accesses less than the TOLM are treated as DRAM accesses (except for the 15-16 MB or PAM gaps). This register must be set to at least 0800h, for a minimum of 128 MB of DRAM. There is also a minimum of 128 MB of PCI space, since this register is on a 128-MB boundary. Configuration software should set this value to either the maximum amount of memory in the system (same as DRB7), or to the lower 128-MB boundary of the Memory Mapped I/O range, whichever is smaller. **Programming example:** 1100_00h = 3 GB (assuming that DRB7 is set > 4 GB): An access to 0_C000_0000h or above (but <4 GB) will be considered above the TOLM and therefore not to main memory. It may go to one of the HI's or be subtractively decoded to HI_A. An access to 0_BFFF_FFFFh and below will be considered below the TOLM and go to main memory.
10:0		Reserved

3.5.35 REMAPBASE—Remap Base Address Register (D0:F0)

Address Offset: C6–C7h
Default Value: 03FFh
Attribute: RO, R/W
Size: 16 bits

Bits	Default, Access	Description
15:10		Reserved
9:0	3FFh R/W	**Remap Base Address 35:26.** The value in this register defines the lower boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A25:0 of the Remap Base Address are assumed to be zeros. Thus, the bottom of the defined memory range will be aligned to a 64-MB boundary. When the value in this register is greater than the value programmed into the Remap Limit register, the Remap window is disabled.

3.5.36 REMAPLIMIT—Remap Limit Address Register (D0:F0)

Address Offset: C8–C9h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bits	Default, Access	Description
15:10		Reserved
9:0	00h R/W	**Remap Limit Address 35:26.** The value in this register defines the upper boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A25:0 of the Remap Limit Address are assumed to be Fhs. Thus, the top of the defined range will be one less than a 64-MB boundary. When the value in this register is less than the value programmed into the Remap Base register, the Remap window is disabled. This field defaults to 0000h.

3.5.37 SKPD—Scratch Pad Data Register (D0:F0)

Address Offset: DE–DFh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bits	Default, Access	Description
15:0	0000h R/W	**Scratch pad (SCRTCH).** These bits are R/W storage bits that have no effect on the MCH functionality.

3.5.38 DVNP—Device Not Present Register (D0:F0)

Address Offset: E0–E1h
Default Value: 1D1Fh
Attribute: RO, R/W
Size: 32 bits

Bits	Default, Access	Description
15:3		Reserved
2	1b R/W	**Device 2, Function 1 Hide.** 0 = Present 1 = **Not** present. Accesses from the processor are disabled when this bit is set.
1		Reserved
0	1b R/W	**Device 0, Function 1 Hide.** 0 = Present 1 = **Not** present. Accesses from the processor are disabled when this bit is set.

3.6 Chipset Host RAS Controller Registers (Device 0, Function 1)

The Chipset Host RAS Controller Error Reporting registers are in Device 0 (D0), Function 1 (F1). Table 3-4 provides the register address map for this device, function.

Warning: Address locations that are not listed the table are considered reserved register locations. Writes to "Reserved" registers may cause system failure. Reads to "Reserved" registers may return a non-zero value.

Table 3-4. Chipset Host RAS Controller Register Address Map (D0:F1)

Address Offset	Mnemonic	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	2551h	RO
04–05h	PCICMD	PCI Command	0000h	RO, RW
06–07h	PCISTS	PCI Status Register	0000h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
0Ah	SUBC	Sub Class Code	00h	RO
0Bh	BCC	Base Class Code	FFh	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	R/WO
40–43h	FERR_GLOBAL	Global First Error	0000 0000h	R/WC, RO
44–47h	NERR_GLOBAL	Global Next Error	0000 0000h	R/WC, RO
50h	HIA_FERR	HI_A First Error	00h	R/WC, RO
52h	HIA_NERR	HI_A Next Error	00h	R/WC, RO
58h	SCICMD_HIA	SCI Command	00h	RO, RW
5Ah	SMICMD_HIA	SMI Command	00h	RO, RW
5Ch	SERRCMD_HIA	SERR Command	00h	RO, RW
60h	SB_FERR	System Bus First Error	00h	R/WC
62h	SB_NERR	System Bus Next Error	00h	R/WC
68h	SCICMD_SB	SCI Command	00h	RW
6Ah	SMICMD_SB	SCI Command	00h	RW
6Ch	SERRCMD_SB	SERR Command	00h	RW
80h	DRAM_FERR	DRAM First Error	00h	R/WC, RO
82h	DRAM_NERR	DRAM Next Error	00h	R/WC, RO
88h	SCICMD_DRAM	SCI Command	00h	RO, RW
8Ah	SMICMD_DRAM	SMI Command	00h	RO, RW
8Ch	SERRCMD_DRAM	SCI Command	00h	RO, RW
A0–A3h	DRAM_CELOG_ADD	DRAM First Correctable Memory Error Address	0000 0000h	RO
B0–B3h	DRAM_UELOG_ADD	DRAM First Uncorrectable Memory Error Address	0000 0000h	RO
D0–D1h	DRAM_CELOG_SYNDROME	DRAM First Correctable Memory Syndrome Error	0000h	RO

3.6.1 VID—Vendor Identification Register (D0:F1)

Address Offset: 00–01h
Default Value: 8086h
Sticky No
Attribute: RO
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register combined with the Device Identification register uniquely identify any PCI device.

Bits	Default, Access	Description
15:0	8086h RO	**Vendor Identification (VID).** This register field contains the PCI standard identification for Intel, 8086h.

3.6.2 DID—Device Identification Register (D0:F1)

Address Offset: 02–03h
Default Value: 2551h
Sticky No
Attribute: RO
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device.

Bits	Default, Access	Description
15:0	2551h RO	**Device Identification Number (DID).** This is a 16-bit value assigned to the MCH Host-HI Bridge Function 1.

3.6.3 PCICMD—PCI Command Register (D0:F1)

Address Offset: 04–05h
Default Value: 0000h
Sticky No
Attribute: RO, R/W
Size: 16 bits

Since MCH Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Bits	Default, Access	Description
15:9		Reserved
8	0b R/W	**SERR Enable (SERRE).** This bit is a global enable bit for Device 0 SERR messaging. The MCH does not have an SERR signal. The MCH communicates the SERR condition by sending an SERR message over HI_A to the Intel® ICH4. 0 = Disable. SERR message is not generated by the MCH for Device 0. 1 = Enable. MCH generates SERR messages over HI_A for specific Device 0 error conditions that are individually enabled in the SERRCMD_HI, SERRCMD_SB, and SERRCMD_DRAM registers. The error status is reported in the FERR register / NERR register and PCISTS registers.
7:0		Reserved

3.6.4 PCISTS—PCI Status Register (D0:F1)

Address Offset: 06–07h
Default Value: 0000h
Sticky No
Attribute: RO/R/W
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device 0's PCI interface. Bit 14 is read/write clear. All other bits are Read Only. Since MCH Device 0 does not physically reside on PCI_A, many of the bits are not implemented.

Bits	Default, Access	Description
15		Reserved
14	0b R/WC	**Signaled System Error (SSE).** Software clears this bit by writing a 1 to it. 0 = MCH Device 0 did **Not** generate an SERR message over HI_A. 1 = MCH Device 0 generated an SERR message over HI_A for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD and SERRCMD_HI, SERRCMD_SB, and SERRCMD_DRAM registers. Device 0 error flags are read/reset from the PCISTS or Error registers.
13:0		Reserved

3.6.5 RID—Revision Identification Register (D0:F1)

Address Offset: 08h
Default Value: see table below
Sticky No
Attribute: RO
Size: 8 bits

This register contains the revision number of the MCH Device 0.

Bits	Default, Access	Description
7:0	00h RO	**Revision Identification Number (RID).** This is an 8-bit value that indicates the revision identification number for the MCH Device 0. This number is always the same as the RID for function 0. 03h = B-0 Stepping.

3.6.6 SUBC—Sub-Class Code Register (D0:F1)

Address Offset: 0Ah
Default Value: 00h
Sticky No
Attribute: RO
Size: 8 bits

Bits	Default, Access	Description
7:0	00h RO	**Sub-Class Code (SUBC).** This is an 8-bit value that indicates the category of Bridge into which the MCH falls. The code is 00h.

3.6.7 BCC—Base Class Code Register (D0:F1)

Address Offset: 0Bh
Default Value: FFh
Sticky No
Attribute: R/O
Size: 8 bits

Bits	Default, Access	Description
7:0	FFh RO	**Base Class Code (BASEC).** This is an 8-bit value that indicates the Base Class Code for the MCH. FFh =Non-defined device. Since this function is used for error conditions, it does not fall into any other class.

3.6.8 MLT—Master Latency Timer Register (D0:F1)

Address Offset: 0Dh
Default Value: 00h
Sticky No
Attribute: RO
Size: 8 bits

Device 0 in the MCH is not a PCI master; therefore, this register is not implemented.

Bits	Default, Access	Description
7:0		Reserved

3.6.9 HDR—Header Type Register (D0:F1)

Address Offset: 0Eh
Default Value: 01h
Sticky No
Attribute: RO
Size: 8 bits

Bits	Default, Access	Description
7:0	01h RO	**PCI Header (HDR).** This read only field always returns 01h to indicate that device 1 is a single-function device with bridge header layout.

3.6.10 SVID—Subsystem Vendor Identification Register (D0:F1)

Address Offset: 2Ch
Default Value: 0000h
Sticky No
Attribute: R/WO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bits	Default, Access	Description
15:0	0000h R/WO	**Subsystem Vendor ID (SUBVID).** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

3.6.11 SID—Subsystem Identification Register (D0:F1)

Address Offset: 2E–2Fh
Default Value: 0000h
Sticky No
Attribute: R/WO
Size: 16 bits

This value is used to identify a particular subsystem.

Bits	Default, Access	Description
15:0	0000h R/WO	**Subsystem ID (SUBID).** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

3.6.12 FERR_GLOBAL—Global First Error Register (D0:F1)

Address Offset:	40–43h
Default Value:	0000 0000h
Sticky	Yes
Attribute:	RO, R/WC
Size:	32 bits

This register is used to report various error conditions. An SERR is generated on a 0-to-1 transition of any of these flags (if enabled by the ERRCMD and PCICMD registers). These bits are set regardless of whether or not the SERR is enabled and generated.

This register stores the FIRST global error. Any future errors (NEXT errors) will be set in the NERR_Global Register. No further error bits in this register will be set until the existing error bit is cleared.

Note: To prevent the same error from being logged twice in FERR_GLOBAL and NERR_GLOBAL, a FERR_GLOBAL bit being set blocks the respective bit in the NERR_GLOBAL Register from being set. In addition, bits [18:16] are grouped such that if any of these bits are set in the FERR_GLOBAL Register, none of the bits [18:16] can be set in the NERR_GLOBAL Register. For example, if HI_A causes its respective FERR_GLOBAL bit to be set, any subsequent DDR, FSB, or HI_A error will not be logged in the NERR_GLOBAL Register. Each of these three bits are part of Device 0 status and having any one of them set in FERR_GLOBAL represents a "Device 0 First Error" occurred. This implementation blocks logging in NERR_GLOBAL of any subsequent "Device 0" errors, and allows only logging of subsequent errors that are from other devices.

Note: Software must write a 1 to clear bits that are set.

Bits	Default, Access	Description
31:19		Reserved
18	0b R/WC	**DRAM Interface Error Detected.** 0 = No DRAM interface error. 1 = MCH detected an error on the DRAM interface.
17	0b R/WC	**HI_A Error Detected.** 0 = No HI_A interface error. 1 = MCH detected an error on the HI_A.
16	0b R/WC	**System Bus Error Detected.** 0 = No system bus interface error. 1 = MCH detected an error on the System Bus.
15:3		Reserved
2	0b R/WC	**HI_B Error Detected.** 0 = No HI_B interface error. 1 = MCH detected an error on HI_B.
1:0		Reserved

3.6.13 NERR_GLOBAL—Global Next Error Register (D0:F1)

Address Offset: 44–47h
Default Value: 0000 0000h
Sticky Yes
Attribute: RO, R/WC
Size: 32 bits

The FIRST global error will be stored in FERR_GLOBAL. This register stores all future global errors. Multiple bits in this register may be set.

Note: To prevent the same error from being logged twice in FERR_GLOBAL and NERR_GLOBAL, a FERR_GLOBAL bit being set blocks the respective bit in the NERR_GLOBAL Register from being set. In addition, bits [18:16] are grouped such that if any of these bits are set in the FERR_GLOBAL Register, none of the bits [18:16] can be set in the NERR_GLOBAL Register. For example, if HI_A causes its respective FERR_GLOBAL bit to be set, any subsequent DDR, FSB, or HI_A error will not be logged in the NERR_GLOBAL Register. Each of these three bits are part of Device 0 status and having any one of them set in FERR_GLOBAL represents a "Device 0 First Error" occurred. This implementation blocks logging in NERR_GLOBAL of any subsequent "Device 0" errors, and allows only logging of subsequent errors that are from other devices.

Note: Software must write a 1 to clear bits that are set.

Bits	Default, Access	Description
31:19		Reserved
18	0b R/WC	**DRAM Interface Error Detected.** 0 = No DRAM interface error detected. 1 = The MCH has detected an error on the DRAM interface.
17	0b R/WC	**HI_A Error Detected.** 0 = No HI_A interface error detected. 1 = The MCH has detected an error on the HI_A.
16	0b R/WC	**System Bus Error Detected.** 0 = No system bus interface error detected. 1 = The MCH has detected an error on the System Bus.
15:3		Reserved
2	0b R/WC	**HI_B Error Detected.** 0 = No HI_B interface error detected. 1 = The MCH has detected an error on HI_B.
1:0		Reserved

3.6.14 HIA_FERR—HI_A First Error Register (D0:F1)

Address Offset:	50h
Default Value:	00h
Sticky	Yes
Attribute:	RO, R/WC
Size:	8 bits

This register stores the first error related to the HI_A interface. Only 1 error bit will be set in this register. Any future errors (NEXT errors) will be set in the HIA_NERR Register. No further error bits in this register will be set until the existing error bit is cleared.

Note: Software must write a 1 to clear bits that are set.

Bits	Default, Access	Description
7		Reserved
6	0b R/WC	**HI A Target Abort (TAHLA).** 0 = No Target Abort on MCH originated HI_A cycle detected. 1 = MCH detected that an MCH originated HI_A cycle was terminated with a Target Abort.
5		Reserved
4	0b R/WC	**HI_A Data Parity Error Detected.** 0 = No data parity error detected. 1 = MCH detected a parity error on a HI_A data transfer.
3:1		Reserved
0	0b R/WC	**HI_A Address/Command Error Detected.** 0 = No address or command parity error detected. 1 = MCH detected a parity error on a HI_A address or command.

3.6.15 HIA_NERR—HI_A Next Error Register (D0:F1)

Address Offset: 52h
Default Value: 00h
Sticky Yes
Attribute: RO, R/WC
Size: 8 bits

The first HI_A error will be stored in the HIA_FERR Register. This register stores all future HI_A errors. Multiple bits in this register may be set.

Note: Software must write a 1 to clear bits that are set.

Bits	Default, Access	Description
7		Reserved
6	0b R/WC	**HI_A Target Abort.** 0 = No Target Abort on MCH originated HI_A cycle terminated. 1 = MCH originated HI_A cycle was terminated with a Target Abort.
5		Reserved
4	0b R/WC	**HI_A Data Parity Error Detected.** 0 = No data parity error detected. 1 = Parity error on a HI_A data transfer.
3:1		Reserved
0	0b R/WC	**HI_A Data Address/Command Error Detected.** 0 = No address or command parity error detected. 1 = Parity error on a HI_A address or command.

3.6.16 SCICMD_HIA—SCI Command Register (D0:F1)

Address Offset: 58h
Default Value: 00h
Sticky No
Attribute: RO, R/W
Size: 8 bits

This register determines whether SCI will be generated when the associated flag is set in the HIA_FERR or HIA_NERR Register. When an error flag is set in the HIA_FERR or HIA_NERR Register, it can generate an SERR, SMI, or SCI when enabled in the SERRCMD, SMICMD, or SCICMD Registers, respectively. Only one message type can be enabled.

Bits	Default, Access	Description
7		Reserved
6	0b R/W	**SCI on HI_A Target Abort Enable.** 0 = No SCI generation 1 = Generate SCI if bit 6 is set in HIA_FERR or HIA_NERR
5		Reserved
4	0b R/W	**SCI on HI_A Data Parity Error Detected Enable.** 0 = No SCI generation 1 = Generate SCI if bit 4 is set in HIA_FERR or HIA_NERR
3:1		Reserved
0	0b R/W	**SCI on HI_A Data Address/Comment Error Detected Enable.** 0 = No SCI generation 1 = Generate SCI if bit 0 is set in HIA_FERR or HIA_NERR

3.6.17 SMICMD_HIA—SMI Command Register (D0:F1)

Address Offset: 5Ah
Default Value: 00h
Sticky No
Attribute: RO, R/W
Size: 8 bits

This register determine whether SMI will be generated when the associated flag is set in either the HIA_FERR or HIA_NERR Register. When an error flag is set in the HIA_FERR or HIA_NERR Register, it can generate an SERR, SMI, or SCI when enabled in the SERRCMD, SMICMD, or SCICMD Registers, respectively. Only one message type can be enabled.

Bits	Default, Access	Description
7		Reserved
6	0b R/W	**SMI on HI_A Target Abort Enable.** 0 = No SMI generation 1 = Generate SMI if bit 6 is set in HIA_FERR or HIA_NERR
5		Reserved
4	0b R/W	**SMI on HI_A Data Parity Error Detected Enable.** 0 = No SMI generation 1 = Generate SMI if bit 4 is set in HIA_FERR or HIA_NERR
3:1		Reserved
0	0b R/W	**SMI on HI_A Data Address/Comment Error Detected Enable.** 0 = No SMI generation 1 = Generate SMI if bit 0 is set in HIA_FERR or HIA_NERR

3.6.18 SERRCMD_HIA—SERR Command Register (D0:F1)

Address Offset: 5Ch
Default Value: 00h
Sticky No
Attribute: RO, R/W
Size: 8 bits

This register determine whether SERR will be generated when the associated flag is set in either the HIA_FERR or HIA_NERR Register. When an error flag is set in the HIA_FERR or HIA_NERR Register, it can generate an SERR, SMI, or SCI when enabled in the SERRCMD, SMICMD, or SCICMD Registers, respectively. Only one message type can be enabled.

Bits	Default, Access	Description
7		Reserved
6	0b R/W	**SERR on HI_A Target Abort Enable.** 0 = No SERR generation 1 = Generate SERR if bit 6 is set in HIA_FERR or HIA_NERR
5		Reserved
4	0b R/W	**SERR on HI_A Data Parity Error Detected Enable.** 0 = No SERR generation 1 = Generate SERR if bit 4 is set in HIA_FERR or HIA_NERR
3:1		Reserved
0	0b R/W	**SEER on HI_A Data Address/Comment Error Detected Enable.** 0 = No SERR generation 1 = Generate SERR if bit 0 is set in HIA_FERR or HIA_NERR

3.6.19 SB_FERR—System Bus First Error Register (D0:F1)

Address Offset:	60h
Default Value:	00h
Sticky	Yes
Attribute:	R/WC
Size:	8 bits

This register stores the first error related to the system bus interface. Any future errors (next errors) will be set in the SB_NERR Register. No further error bits in this register will be set until the existing error bit is cleared.

Note: Software must write a 1 to clear bits that are set.

Bits	Default, Access	Description
7	0b R/WC	**System Bus BINIT# Detected.** 0 = No system bus BINT# detected. 1 = This bit is set on an electrical high-to-low transition (0-to-1) of BINIT#.
6	0b R/WC	**System Bus XERR# Detected.** 0 = No system bus XERR# detected. 1 = This bit is set on an electrical high-to-low transition (0 to 1) of xERR# on the system bus. xERR# is either IERR# or BERR# from the SB and is up to system designer to determine which to use.
5	0b R/WC	**Non-DRAM Lock Error (NDLOCK).** 0 = No DRAM lock error detected. 1 = MCH detected a lock operation to memory space that did not map into DRAM.
4	0b R/WC	**System Bus Address Above TOM (SBATOM).** 0 = No system bus address above TOM detected. 1 = MCH detected an address above DRB7, which is the Top of Memory and above 4 GB. If the system has less than 4 GB of DRAM, then addresses between DRB7 and 4 GB are sent to HI_A.
3	0b R/WC	**System Bus Data Parity Error (SBDPAR).** 0 = No system bus data parity error detected. 1 = The MCH has detected a data parity error on the system bus.
2	0b R/WC	**System Bus Address Strobe Glitch Detected (SBAGL).** 0 = No system bus address strobe glitch detected. 1 = The MCH has detected a glitch on one of the system bus address strobes.
1	0b R/WC	**System Bus Data Strobe Glitch Detected (SBDGL).** 0 = No system bus data strobe glitch detected. 1 = The MCH has detected a glitch on one of the system bus data strobes.
0	0b R/WC	**System Bus Request/Address Parity Error (SBRPAR).** 0 = No system bus request/address parity error detected. 1 = MCH detected a parity error on either the address or request signals of the system bus.

3.6.20 SB_NERR—System Bus Next Error Register (D0:F1)

Address Offset:	62h
Default Value:	00h
Sticky	Yes
Attribute:	R/WC
Size:	8 bits

The first system bus error will be stored in the SB_FERR Register. This register stores all future system bus errors. Multiple bits in this register may be set.

Note: Software must write a 1 to clear bits that are set.

Bits	Default, Access	Description
7	0b R/WC	**System Bus BINIT# Detected.** 0 = No system bus BINIT# detected. 1 = This bit is set on an electrical high-to-low transition (0 to 1) of BINIT#.
6	0b R/WC	**System Bus XERR# Detected.** 0 = No system bus XERR# detected. 1 = This bit is set on an electrical high-to-low transition (0 to 1) of XERR# on the system bus.
5	0b R/WC	**Non-DRAM Lock Error (NDLOCK).** 0 = No non-DRAM lock error detected. 1 = The MCH has detected a lock operation to memory space that did not map into DRAM.
4	0b R/WC	**System Bus Address Above TOM (SBATOM).** 0 = No system bus address above TOM detected. 1 = MCH detected an address above DRB7, which is the Top of Memory and above 4 GB.
3	0b R/WC	**System Bus Data Parity Error (SBDPAR).** 0 = No system bus data parity error detected. 1 = MCH detected a data parity error on the system bus.
2	0b R/WC	**System Bus Address Strobe Glitch Detected (SBAGL).** 0 = No system bus address strobe glitch detected. 1 = MCH detected a glitch on one of the system bus address strobes.
1	0b R/WC	**System Bus Data Strobe Glitch Detected (SBDGL).** 0 = No System Bus Data Strobe Glitch detected. 1 = MCH detected a glitch on one of the system bus data strobes.
0	0b R/WC	**System Bus Request/Address Parity Error (SBRPAR).** 0 = No system bus request/address parity error detected. 1 = MCH detected a parity error on either the address or request signals of the system bus.

3.6.21 SCICMD_SB—SCI Command Register (D0:F1)

Address Offset: 68h
Default Value: 00h
Sticky No
Attribute: R/W
Size: 8 bits

This register determine whether SCI will be generated when the associated flag is set in either the SB_FERR or SB_NERR Register. When an error flag is set in the SB_FERR or SB_NERR Register, it can generate an SERR, SMI, or SCI when enabled in the SERRCMD, SMICMD, or SCICMD Registers, respectively. Only one message type can be enabled.

Bits	Default, Access	Description
7	0b R/W	**SCI on System Bus BINIT# Detected Enable.** 0 = No SCI generation 1 = Generate SCI if bit 7 is set in SB_FERR or SB_NERR
6	0b R/W	**SCI on System Bus xERR# Detected Enable.** 0 = No SCI generation 1 = Generate SCI if bit 6 is set in SB_FERR or SB_NERR
5	0b R/W	**SCI on Non-DRAM Lock Error Enable.** 0 = No SCI generation 1 = Generate SCI if bit 5 is set in SB_FERR or SB_NERR
4	0b R/W	**SCI on System Bus Address Above TOM Enable.** 0 = No SCI generation 1 = Generate SCI if bit 4 is set in SB_FERR or SB_NERR
3	0b R/W	**SCI on System Bus Data Parity Error Enable.** 0 = No SCI generation 1 = Generate SCI if bit 3 is set in SB_FERR or SB_NERR
2	0b R/W	**SCI on System Bus Address Strobe Glitch Detected Enable.** 0 = No SCI generation 1 = Generate SCI if bit 2 is set in SB_FERR or SB_NERR
1	0b R/W	**SCI on System Bus Data Strobe Glitch Detected Enable.** 0 = No SCI generation 1 = Generate SCI if bit 1 is set in SB_FERR or SB_NERR
0	0b R/W	**SCI on System Bus Request/Address Parity Error Enable.** 0 = No SCI generation 1 = Generate SCI if bit 0 is set in SB_FERR or SB_NERR

3.6.22 SMICMD_SB—SMI Command Register (D0:F1)

Address Offset:	6Ah
Default Value:	00h
Sticky	No
Attribute:	R/W
Size:	8 bits

This register determines whether SMI will be generated when the associated flag is set in either the SB_FERR or SB_NERR Register. When an error flag is set in the SB_FERR or SB_NERR Register, it can generate an SERR, SMI, or SCI when enabled in the SERRCMD, SMICMD, or SCICMD Registers, respectively. Only one message type can be enabled.

Bits	Default, Access	Description
7	0b R/W	**SMI on System Bus BINIT# Detected Enable.** 0 = No SMI generation 1 = Generate SMI if bit 7 is set in SB_FERR or SB_NERR
6	0b R/W	**SMI on System Bus xERR# Detected Enable.** 0 = No SMI generation 1 = Generate SMI if bit 6 is set in SB_FERR or SB_NERR
5	0b R/W	**SMI on Non-DRAM Lock Error Enable.** 0 = No SMI generation 1 = Generate SMI if bit 5 is set in SB_FERR or SB_NERR
4	0b R/W	**SMI on System Bus Address Above TOM Enable.** 0 = No SMI generation 1 = Generate SMI if bit 4 is set in SB_FERR or SB_NERR
3	0b R/W	**SMI on System Bus Data Parity Error Enable.** 0 = No SMI generation 1 = Generate SMI if bit 3 is set in SB_FERR or SB_NERR
2	0b R/W	**SMI on System Bus Address Strobe Glitch Detected Enable.** 0 = No SMI generation 1 = Generate SMI if bit 2 is set in SB_FERR or SB_NERR
1	0b R/W	**SMI on System Bus Data Strobe Glitch Detected Enable.** 0 = No SMI generation 1 = Generate SMI if bit 1 is set in SB_FERR or SB_NERR
0	0b R/W	**SMI on System Bus Request/Address Parity Error Enable.** 0 = No SMI generation 1 = Generate SMI if bit 0 is set in SB_FERR or SB_NERR

3.6.23 SERRCMD_SB—SERR Command Register (D0:F1)

Address Offset: 6Ch
Default Value: 00h
Sticky No
Attribute: R/W
Size: 8 bits

This register determines whether SERR will be generated when the associated flag is set in either the SB_FERR or SB_NERR Register. When an error flag is set in the SB_FERR or SB_NERR Register, it can generate an SERR, SMI, or SCI when enabled in the SERRCMD, SMICMD, or SCICMD Registers, respectively. Only one message type can be enabled.

Bits	Default, Access	Description
7	0b R/W	**SERR on System Bus BINIT# Detected Enable.** 0 = No SERR generation 1 = Generate SERR if bit 7 is set in SB_FERR or SB_NERR
6	0b R/W	**SERR on System Bus xERR# Detected Enable.** 0 = No SERR generation 1 = Generate SERR if bit 6 is set in SB_FERR or SB_NERR
5	0b R/W	**SERR on Non-DRAM Lock Error Enable.** 0 = No SERR generation 1 = Generate SERR if bit 5 is set in SB_FERR or SB_NERR
4	0b R/W	**SERR on System Bus Address Above TOM Enable.** 0 = No SERR generation 1 = Generate SERR if bit 4 is set in SB_FERR or SB_NERR
3	0b R/W	**SERR on System Bus Data Parity Error Enable.** 0 = No SERR generation 1 = Generate SERR if bit 3 is set in SB_FERR or SB_NERR
2	0b R/W	**SERR on System Bus Address Strobe Glitch Detected Enable.** 0 = No SERR generation 1 = Generate SERR if bit 2 is set in SB_FERR or SB_NERR
1	0b R/W	**SERR on System Bus Data Strobe Glitch Detected Enable.** 0 = No SERR generation 1 = Generate SERR if bit 1 is set in SB_FERR or SB_NERR
0	0b R/W	**SERR on System Bus Request/Address Parity Error Enable.** 0 = No SERR generation 1 = Generate SERR if bit 0 is set in SB_FERR or SB_NERR

3.6.24 DRAM_FERR—DRAM First Error Register (D0:F1)

Address Offset:	80h
Default Value:	00h
Sticky	Yes
Attribute:	RO, R/WC
Size:	8 bits

This register stores the FIRST ECC error on the DRAM interface. Only 1 error bit will be set in this register. Any future errors (NEXT errors) will be set in the DRAM_NERR Register. No further error bits in this register will be set until the existing error bit is cleared.

Note: Software must write a 1 to clear bits that are set.

Bits	Default, Access	Description
7:2		Reserved
1	0b R/WC	**Uncorrectable Memory Error Detected.** 0 = No uncorrectable memory error detected. 1 = MCH detected an ECC error on the memory interface that is not correctable.
0	0b R/WC	**Correctable Memory Error Detected.** 0 = No correctable memory error detected. 1 = MCH detected and corrected an ECC error on the memory interface.

3.6.25 DRAM_NERR—DRAM Next Error Register (D0:F1)

Address Offset:	82h
Default Value:	00h
Sticky	Yes
Attribute:	RO, R/WC
Size:	8 bits

The FIRST memory ECC error will be stored in the DRAM_FERR Register. This register stores all future memory ECC errors. Multiple bits in this register may be set.

Note: Software must write a 1 to clear bits that are set.

Bits	Default, Access	Description
7:2		Reserved
1	0b R/WC	**Uncorrectable Memory Error Detected.** 0 = No uncorrectable memory error detected. 1 = The MCH has detected an ECC error on the memory interface that is not correctable.
0	0b R/WC	**Correctable Memory Error Detected.** 0 = No correctable memory error detected. 1 = The MCH has detected and corrected an ECC error on the memory interface.

3.6.26 SCICMD_DRAM —SCI Command Register (D0:F1)

Address Offset: 88h
Default Value: 00h
Sticky No
Attribute: RO, R/W
Size: 8 bits

This register determines whether SCI will be generated when the associated flag is set in the DRAM_FERR or DRAM_NERR Register. When an error flag is set in the DRAM_FERR or DRAM_NERR Registers, it can generate an SERR, SMI, or SCI when enabled in the SERRCMD, SMICMD, or SCICMD Registers, respectively. Only one message type can be enabled.

Bits	Default, Access	Description
7:2		Reserved
1	0b R/W	**SCI on Multiple-Bit DRAM ECC Error (DMERR).** 0 = Disable. 1 = Enable. The MCH generates an SCI when it detects a multiple-bit error reported by the DRAM controller.
0	0b R/W	**SCI on Single-Bit DRAM ECC Error (DSERR).** 0 = Disable. 1 = Enable. The MCH generates an SCI when the DRAM controller detects a single-bit error.

3.6.27 SMICMD_DRAM—SMI Command Register (D0:F1)

Address Offset: 8Ah
Default Value: 00h
Sticky No
Attribute: RO, R/W
Size: 8 bits

This register determines whether SMI will be generated when the associated flag is set in the DRAM_FERR or DRAM_NERR Register. When an error flag is set in the DRAM_FERR or DRAM_NERR Register, it can generate an SERR, SMI, or SCI when enabled in the SERRCMD, SMICMD, or SCICMD Registers, respectively. Only one message type can be enabled.

Bits	Default, Access	Description
7:2		Reserved
1	0b R/W	**SMI on Multiple-Bit DRAM ECC Error (DMERR).** 0 = Disable. 1 = Enable. The MCH generates an SMI when it detects a multiple-bit error reported by the DRAM controller.
0	0b R/W	**SMI on Single-Bit DRAM ECC Error (DSERR).** 0 = Disable. 1 = Enable. The MCH generates an SMI when the DRAM controller detects a single-bit error.

3.6.28 SERRCMD_DRAM—SEER Command Register (D0:F1)

Address Offset: 8Ch
Default Value: 00h
Sticky No
Attribute: RO, R/W
Size: 8 bits

This register determines whether SERR will be generated when the associated flag is set in the DRAM_FERR or DRAM_NERR Register. When an error flag is set in the DRAM_FERR or DRAM_NERR Registers, it can generate an SERR, SMI, or SCI when enabled in the SERRCMD, SMICMD, or SCICMD Registers, respectively. Only one message type can be enabled.

Bits	Default, Access	Description
7:2		Reserved
1	0b R/W	**SERR on Multiple-Bit DRAM ECC Error (DMERR).** 0 = Disable. 1 = Enable. The MCH generates an SERR when it detects a multiple-bit error reported by the DRAM controller.
0	0b R/W	**SERR on Single-Bit DRAM ECC Error (DSERR).** 0 = Disable. 1 = Enable. The MCH generates an SERR when the DRAM controller detects a single-bit error.

3.6.29 DRAM_CELOG_ADD—DRAM First Correctable Memory Error Address Register (D0:F1)

Address Offset: A0–A3h
Default Value: 0000 0000h
Sticky Yes
Attribute: RO
Size: 32 bits

This register contains the address of the first correctable memory error. This register is locked when bits in either the DRAM_FERR or DRAM_NERR Registers are set. If the bits in both registers are set to 0, the DRAM_CELOG_ADD can be updated; however, if a bit in either register is set to 1, then DRAM_CELOG_ADD will retain its value for logging purposes. This register is only valid if a bit in either the DRAM_FERR or DRAM_NERR Register is set.

Bits	Default, Access	Description
31:28		Reserved
27:6	0000h RO	**CE Address.** This field contains address bits 33:12 of the first correctable memory error. The address bits are a physical address.
5:0		Reserved

3.6.30 DRAM_UELOG_ADD—DRAM First Uncorrectable Memory Error Address Register (D0:F1)

Address Offset: B0–B3h
Default Value: 0000 0000h
Sticky Yes
Attribute: RO
Size: 32 bits

This register contains the address of the first uncorrectable memory error. When a bit in either the DRAM_FERR or DRAM_NERR Register is set, this register is locked. This register is only valid if a bit in either the DRAM_FERR or DRAM_NERR Register is set.

Bits	Default, Access	Description
31:28		Reserved
27:6	0000b RO	**UE Address.** This field contains address bits 33:12 of the first uncorrectable memory error. The address bits are a physical address.
5:0		Reserved

3.6.31 DRAM_CELOG_SYNDROME—DRAM First Correctable Memory Error Register (D0:F1)

Address Offset: D0–D1h
Default Value: 0000h
Sticky Yes
Attribute: RO
Size: 16 bits

This register contains the syndrome of the first correctable memory error. This register is locked when a bit in either the DRAM_FERR or DRAM_NERR Register is set. If the bits in both registers are set to 0, the DRAM_CELOG_SYNDROME can be updated; however, if a bit in either register is set to 1, then DRAM_CELOG_SYNDROME will retain its value for logging purposes. This register is only valid if a bit in either the DRAM_FERR or DRAM_NERR Register is set.

Bits	Default, Access	Description
15:0	0000h RO	ECC Syndrome for correctable error

3.7 PCI-to-AGP Bridge Registers (Device 1, Function 0)

The PCI-to-AGP registers are in Device 1 (D1), Function 0 (F0). Table 3-5 provides the register address map for this device, function.

Warning: Address locations that are not listed the table are considered reserved register locations. Writes to "Reserved" registers may cause system failure. Reads to "Reserved" registers may return a non-zero value.

Table 3-5. PCI-to-AGP Bridge Register Address Map (D1:F0)

Address Offset	Mnemonic	Register Name	Default Value	Access
00–01h	VID1	Vendor Identification	8086h	RO
02–03h	DID1	Device Identification	2552h	RO
04–05h	PCICMD1	PCI Command	0000h	RO, RW
06–07h	PCISTS1	PCI Status	00B0h	R/WC, RO
08h	RID1	Revision Identification	See register description	RO
0Ah	SUBC1	Sub Class Code	04h	RO
0Bh	BCC1	Base Class Code	06h	RO
0Dh	MLT1	Master Latency Timer	00h	RO,RW
0Eh	HDR1	Header Type	01h	RO
10–13h	APBASELO	AGP Aperture Base Address	0000 0008h	RO,RW
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	RW
1Ah	SUBUSN1	Subordinate Bus Number	00h	RW
1Bh	SMLT1	Secondary Bus Master Latency Timer	00h	RO,RW
1Ch	IOBASE1	I/O Base Address	F0h	RO,RW
1Dh	IOLIMIT1	I/O Limit Address	00h	RO,RW
1E–1Fh	SSTS1	Secondary Status	02A0h	RW
20–21h	MBASE1	Memory Base Address	FFF0h	RO, RW
22–23h	MLIMIT1	Memory Limit Address	0000h	RO, RW
24–25h	PMBASE1	Prefetchable Memory Base Address	FFF0h	RO, RW
26–27h	PMLIMIT1	Prefetchable Memory Limit Address	0000h	RO, RW
34h	CAPPTR	Capabilities Pointer	60h	RO
3Eh	BCTRL1	Bridge Control	00h	RO, RW
40h	ERRCMD1	Error Command	00h	RO, RW
42h	ERRSTS1	Error Status	00h	RO, R/WC
60–63h	AGPCAPID1	AGP Capability Identifier	0035 0002h	RO
64–67h	AGPSTAT1	AGP Status	1F00 xx1xh	RO
68–6Bh	AGPCMD	AGP Command	0000 0000h	RO, RW
70–73h	AGPCTR1L	AGP Control Register	0000 0000h	RO, RW
74–75h	APSIZE1	AGP Aperture Size	0000h	RO, RW
78–7Bh	ATTBASE1	AGP GART Pointer	0000 0000h	RO, RW

3.7.1 VID1—Vendor Identification Register (D1:F0)

Address Offset: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register combined with the Device Identification register uniquely identify any PCI device.

Bits	Default, Access	Description
15:0	8086h RO	**Vendor Identification Device 1 (VID1).** This register field contains the PCI standard identification for Intel, 8086h.

3.7.2 DID1—Device Identification Register (D1:F0)

Address Offset: 02–03h
Default Value: 2552h
Attribute: RO
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device.

Bits	Default, Access	Description
15:0	2552h RO	**Device Identification Number (DID).** This is a 16-bit value assigned to the MCH device 1.

3.7.3 PCICMD1—PCI Command Register (D1:F0)

Address Offset: 04–05h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bits	Default, Access	Description
15:10		Reserved
9	0b RO	**Fast Back-to-Back Enable (FB2B).** Hardwired to 0. Not Applicable.
8	0b R/W	**SERR Message Enable (SERRE).** This bit is a global enable bit for Device 1 SERR messaging. The MCH communicates the SERR# condition by sending an SERR message to the Intel® ICH4. 0 = SERR message is not generated by the MCH for Device 1. 1 = MCH is enabled to generate SERR messages over HI for specific Device 1 error conditions that are individually enabled in the BCTRL1 register. The error status is reported in the PCISTS1 register.
7	0b RO	**Address/Data Stepping (ADSTEP).** Hardwired to 0. Address/data stepping is not implemented in the MCH.
6	0b RO	**Parity Error Enable (PERRE).** Hardwired to 0. Parity checking is not supported on the primary side of this device.
5		Reserved
4	0b RO	**Memory Write and Invalidate Enable (MWIE).** Hardwired to 0. Not implemented.
3	0b RO	**Special Cycle Enable (SCE).** Hardwired to 0. Not implemented.
2	0b R/W	**Bus Master Enable (BME).** 0 = AGP Master initiated Frame# cycles are ignored by the MCH. The result is a master abort. Ignoring incoming cycles on the secondary side of the PCI-to-PCI bridge effectively disabled the bus master on the primary side. (Default) 1 = AGP master-initiated Frame# cycles are accepted by the MCH if they hit a valid address decode range. This bit has no affect on AGP Master originated SBA or PIPE# cycles.
1	0b R/W	**Memory Access Enable (MAE).** 0 = Disable. All of device 1's memory space is disabled. 1 = Enable. Enables the Memory and Pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	0b R/W	**I/O Access Enable (IOAE).** 0 = Disable. All of device 1's I/O space is disabled. 1 = Enable. Enables the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.

3.7.4 PCISTS1—PCI Status Register (D1:F0)

Address Offset: 06–07h
Default Value: 00A0h/00B0h
Attribute: RO, R/WC
Size: 16 bits

PCISTS1 is a 16-bit status register that reports the occurrence of error conditions associated with primary side of the virtual PCI-to-PCI bridge embedded within the MCH.

Bits	Default, Access	Description
15	0b RO	**Detected Parity Error (DPE).** Hardwired to 0. Parity is not supported on the primary side of this device.
14	0b R/WC	**Signaled System Error (SSE).** ‘ 0 = MCH Device 1 did **Not** generated an SERR message over HI_A for any enabled Device 1 error condition. 1 = MCH Device 1 generated an SERR message over HI_A for any enabled Device 1 error condition. Device 1 error conditions are enabled in the ERRCMD, PCICMD1 and BCTRL1 registers. Device 1 error flags are read/reset from the ERRSTS and SSTS1 register. **NOTE:** Software clears this bit by writing a 1 to it.
13	0b RO	**Received Master Abort Status (RMAS).** Hardwired to 0. The concept of a master abort does not exist on primary side of this device.
12	0b RO	**Received Target Abort Status (RTAS).** Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	0b RO	**Signaled Target Abort Status (STAS).** Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	00b RO	**DEVSEL# Timing (DEVT).** Hardwired to 00. The MCH does not support subtractive decoding devices on bus 0. therefore, this bit is hardwired to 00 to indicate that device 1 uses the fastest possible decode.
8	0b RO	**Data Parity Detected (DPD).** Hardwired to 0. Parity is not supported on the primary side of this device.
7	1b RO	**Fast Back-to-Back (FB2B).** Hardwired to 1. This indicate that the AGP interface always supports fast back to back writes.
6		Reserved
5	1b RO	**66/60 MHz capability (CAP66).** Hardwired to 1. This indicates that the AGP/PCI bus is 66 MHz capable.
4	0b or 1b RO	**Capability List (CLIST).** When this bit is set to 1, it indicates to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the AGP 8x Capability standard register resides. This bit is read only, and is set by BIOS.
3:0		Reserved

3.7.5 RID1—Revision Identification Register (D1:F0)

Address Offset: 08h
Default Value: see table below
Attribute: RO
Size: 8 bits

This register contains the revision number of the MCH device 1. These bits are read only and writes to this register have no effect.

Bits	Default, Access	Description
7:0	00h RO	**Revision Identification Number (RID).** This is an 8-bit value that indicates the revision identification number for the MCH device 1. It is always the same as the value in RID. 03h = B-0 Stepping

3.7.6 SUBC1—Sub-Class Code Register (D1:F0)

Address Offset: 0Ah
Default Value: 04h
Attribute: RO
Size: 8 bits

This register contains the Sub-Class Code for the MCH device 1.

Bits	Default, Access	Description
7:0	04h RO	**Sub-Class Code (SUBC).** This is an 8-bit value that indicates the category of Bridge into which the device 1 of the MCH falls. 04h = PCI to PCI bridge.

3.7.7 BCC1—Base Class Code Register (D1:F0)

Address Offset: 0Bh
Default Value: 06h
Attribute: RO
Size: 8 bits

This register contains the Base Class Code of the MCH device 1.

Bits	Default, Access	Description
7:0	06h RO	**Base Class Code (BASEC).** This is an 8-bit value that indicates the Base Class Code for the MCH device 1. 06h = Bridge device

3.7.8 MLT1—Master Latency Timer (Scratch Pad) Register (D1:F0)

Address Offset: 0Dh
Default Value: 00h
Attribute: R/W, RO
Size: 8 bits

This functionality is not applicable. It is described here since these bits should be implemented as a read/write to prevent standard PCI-to-PCI bridge configuration software from getting “confused.”

Bits	Default, Access	Description
7:3	00000b R/W	**Scratch pad MLT (NA7.3).** These bits return the value with which they are written; however, they have no internal function and are implemented as a scratch pad merely to avoid confusing software.
2:0		Reserved

3.7.9 HDR1—Header Type Register (D1:F0)

Address Offset: 0Eh
Default Value: 01h
Attribute: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bits	Default, Access	Description
7:0	01h RO	**Header Type Register (HDR).** This read only field always returns 01h to indicate that MCH device 1 is a single function device with bridge header layout.

3.7.10 APBASELO—AGP Aperture Base Address Register (D1:F0)

Address Offset:	10–13h
Default Value:	0000 0008h
Attribute:	R/W, RO
Size:	32 bits

Note that the intention is that the APSIZE register force individual bits to Read Only as 0, although the E7505 (and other chips) implementation only causes them to be Read Only, and does not force them to 0. The default is 0, so the difference would only occur if the aperture was set to a small size, specific APBASE bits were set to ones, and the aperture size was then increased. APBASE bits affected by the APSIZE change would then be Read Only as whatever value they had previously been written. While this could cause bits to read back as 1 instead of 0, the actual aperture decode will be done properly according to the APSIZE register. Software can avoid this situation by writing the APBASE register to 0 prior to increasing the aperture size via APSIZE. The aperture should be disabled prior to any change in APBASE or APSIZE. **Set by BIOS.**

Bits	Default, Access	Description
31:28	0h R/W	**Upper Programmable Base Address (UPBITS).** These bits are part of the aperture base set by configuration software to locate the base address of the graphics aperture. They correspond to bits 31:28 of the base address in the processor's address space that will cause a graphics aperture translation to be inserted into the path of any memory read or write.
27:22	00h R/W or RO depending on aperture size	**Middle Hardwired/Programmable Base Address (MIDBITS).** These bits are part of the aperture base set by configuration software to locate the base address of the graphics aperture. They correspond to bits 27:4 of the base address in the processor's address space that will cause a graphics aperture translation to be inserted into the path of any memory read or write. These bits can individually behave as read only if programmed to do so by the APSIZE bits of the APSIZE register. This will cause configuration software to understand that the granularity of the graphics aperture base address is either finer or more coarse, depending on the bits set by MCH-specific configuration software in APSIZE. **NOTE:** Not forced to 0 when read only.
21:4	00000h RO	Hardwired to 0s. This forces minimum AGP aperture size to be 4 MB or greater.
3	1b RO	**Prefetchable.** Hardwired to 1. This identifies the Graphics AGP aperture range as prefetchable (i.e., there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and Core-logic may merge host processor writes into this range without causing errors).
2:1	“00”b RO	**Type.** Hardwired to 00. The AGP allows the target to support a 32-bit Base Address register for APBASE. 00 = 32-bit Base Address register; NGP aperture can be located anywhere within a 32-bit address space
0	0b RO	**Memory.** Hardwired to 0. This indicates that the Graphics AGP aperture must reside in “Memory” space – as defined by the PCI specification.

3.7.11 PBUSN1—Primary Bus Number Register (D1:F0)

Address Offset: 18h
Default Value: 00h
Attribute: RO
Size: 8 bits

This register identifies that virtual PCI-to-PCI bridge is connected to bus #0.

Bits	Default, Access	Description
7:0	00h RO	**Primary Bus Number (BUSN).** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 00h.

3.7.12 SBUSN1—Secondary Bus Number Register (D1:F0)

Address Offset: 19h
Default Value: 00h
Attribute: RO, R/W
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the virtual PCI-to-PCI bridge (i.e., to AGP). This number is programmed by the PCI configuration software to allow mapping of configuration cycles to AGP.

Bits	Default, Access	Description
7:0	00h R/W	**Secondary Bus Number (BUSN).** This field is programmed by configuration software with the bus number assigned to AGP.

3.7.13 SUBUSN1—Subordinate Bus Number Register (D1:F0)

Address Offset: 1Ah
Default Value: 00h
Attribute: R/W
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below AGP. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to AGP.

Bits	Default, Access	Description
7:0	00h R/W	**Subordinate Bus Number (BUSN).** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the device 1 bridge. When only a single PCI device resides on the AGP segment, this register contains the same value as the SBUSN1 register.

3.7.14 SMLT1—Secondary Bus Master Latency Timer Register (D1:F0)

Address Offset: 1Bh
Default Value: 00h
Attribute: R/W, RO
Size: 8 bits

This register controls the bus tenure of the MCH on AGP/PCI the same way device 0 MLT controls the access to the PCI_A bus.

Bits	Default, Access	Description
7:3	00000b R/W	**Secondary MLT Counter Value (MLT).** Programmable, default = 0 (SMLT disabled)
2:0		Reserved

3.7.15 IOBASE1—I/O Base Address Register (D1:F0)

Address Offset: 1Ch
Default Value: F0h
Attribute: R/W, RO
Size: 8 bits

This register control the processor-to-AGP I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A11:0 are treated as 0. Thus, the bottom of the defined I/O address range will be aligned to a 4-KB boundary.

Bits	Default, Access	Description
7:4	Fh R/W	**I/O Address Base (IOBASE).** These bits correspond to A15:12 of the I/O addresses passed by bridge 1 to AGP.
3:0		Reserved

3.7.16 IOLIMIT1—I/O Limit Address Register (D1:F0)

Address Offset: 1Dh
Default Value: 00h
Attribute: R/W, RO
Size: 8 bits

This register controls the processor-to-AGP I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT1

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A11:0 are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-KB aligned address block.

Bits	Default, Access	Description
7:4	0h R/W	**I/O Address Limit (IOLIMIT).** This field corresponds to A15:12 of the I/O address limit of device 1. Devices between this upper limit and IOBASE1 will be passed to AGP.
3:0		Reserved

3.7.17 SSTS1—Secondary Status Register (D1:F0)

Address Offset: 1E–1Fh
Default Value: 02A0h
Attribute: R/W
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with the secondary side (i.e., AGP side) of the virtual PCI-to-PCI bridge in the MCH.

Note: Software writes a 1 to clear bits that are set.

Bits	Default, Access	Description
15	0b R/WC	**Detected Parity Error (DPE).** 0 = No parity error detected in the address or data phase of AGP bus transactions. 1 = MCH detected a parity error in the address or data phase of AGP bus transactions.
14	0b R/WC	**Received System Error (RSE).** 0 = No SERR# assertion detected. 1 = MCH detects SERR# assertion on the secondary side of this device.
13	0b R/WC	**Received Master Abort Status (RMAS).** 0 = MCH Does **Not** terminate a Host-to-AGP with an unexpected master abort. 1 = MCH terminates a Host-to-AGP with an unexpected master abort.
12	0b R/WC	**Received Target Abort Status (RTAS).** 0 = MCH-initiated transaction on AGP is **Not** terminated with a target abort. 1 = MCH-initiated transaction on AGP is terminated with a target abort.
11	0b RO	**Signaled Target Abort Status (STAS).** Hardwired to 0. The MCH does not generate target abort on AGP.
10:9	01b RO	**DEVSEL# Timing (DEVT).** Hardwired to 01. This 2-bit field indicates the timing of the DEVSEL# signal when the MCH responds as a target on AGP; a value of 01(medium) indicate the time when a valid DEVSEL# can be sampled by the initiator of the PCI cycle.
8	0b RO	**Master Data Parity Error Detected (DPD).** Hardwired to 0. MCH does not implement G_PERR# signal on AGP.
7	1b RO	**Fast Back-to-Back (FB2B).** Hardwired to 1. MCH, as a target, supports fast back-to-back transactions on AGP.
6		Reserved
5	1b RO	**66/60 MHz capability (CAP66).** Hardwired to 1. This indicates that the AGP bus is capable of 66 Mhz operation.
4:0		Reserved

3.7.18 MBASE1—Memory Base Address Register (D1:F0)

Address Offset: 20–21h
Default Value: FFF0h
Attribute: R/W, RO
Size: 16 bits

This register controls the processor-to-AGP non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A31:20 of the 32-bit address. The bottom 4 bits of this register are read only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A19:0 are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bits	Default, Access	Description
15:4	FFFh R/W	**Memory Address Base (MBASE).** This field corresponds to A31:20 of the lower limit of the memory range that will be passed by the device 1 bridge to AGP.
3:0		Reserved

3.7.19 MLIMIT1—Memory Limit Address Register (D1:F0)

Address Offset:	22–23h
Default Value:	0000h
Attribute:	R/W, RO
Size:	16 bits

This register controls the processor-to-AGP non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A31:20 of the 32-bit address. The bottom 4 bits of this register are read only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A19:0 are assumed to be FFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable AGP address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved processor-to-AGP memory access performance.

Note: Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges (prevent overlap with each other and/or with the ranges covered with the main memory). There is no provision in the MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bits	Default, Access	Description
15:4	000h R/W	**Memory Address Limit (MLIMIT).** These bits corresponds to A31:20 of the memory address that corresponds to the upper limit of the range of memory accesses that will be passed by the device 1 bridge to AGP.
3:0		Reserved

3.7.20 PMBASE1—Prefetchable Memory Base Address Register (D1:F0)

Address Offset:	24–25h
Default Value:	FFF0h
Attribute:	R/W, RO
Size:	16 bits

This register controls the processor-to-AGP prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A31:20 of the 32-bit address. The bottom 4 bits of this register are read only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A19:0 are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bits	Default, Access	Description
15:4	FFFFh R/W	**Prefetchable Memory Address Base (PMBASE).** These bits corresponds to A31:20 of the lower limit of the address range passed by bridge device 1 across AGP.
3:0		Reserved

3.7.21 PMLIMIT1—Prefetchable Memory Limit Address Register (D1:F0)

Address Offset: 26–27h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

This register controls the processor-to-AGP prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A31:20 of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A19:0 are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Note: Prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bits	Default, Access	Description
15:4	000h R/W	**Prefetchable Memory Address Limit (PMLIMIT).** This field corresponds to A31:20 of the upper limit of the address range passed by bridge device 1 across AGP.
3:0		Reserved

3.7.22 CAPPTR—Capabilities Pointer Register (D1:F0)

Address Offset: 34h
Default Value: 60h
Attribute: RO
Size: 8 bits

The CAPPTR register provides an address pointer to the location where the AGP standard registers are located.

Bits	Default, Access	Description
7:0	60h RO	**Standard AGP Register Block Pointer (REGBLOK).** This pointer indicates to software where it can find the beginning of the AGP register block.

3.7.23 BCTRL1—Bridge Control Register (D1:F0)

Address Offset: 3Eh
Default Value: 00h
Attribute: R/W, RO
Size: 8 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-to-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., AGP) as well as some bits that affect the overall behavior of the virtual PCI-to-PCI bridge embedded within MCH (e.g., VGA compatible address ranges mapping).

Bits	Default, Access	Description
7	0b RO	**Fast Back-to-Back Enable (FB2BEN).** Hardwired to 0. The MCH does not generate fast back-to-back cycles as a master on AGP.
6	0b RO	**Secondary Bus Reset (SRESET).** Hardwired to 0. MCH does not support generation of reset via this bit on the AGP.
5	0b RO	**Master Abort Mode (MAMODE).** Hardwired to 0. When acting as a master on AGP, the MCH will drop writes and return all 1s during reads when a Master Abort occurs.
4		Reserved
3	0b R/W	**VGA Enable (VGAEN).** This bit, along with the MDAP bit in the MCHCFG register (offset 50h), controls the routing of processor-initiated transactions targeting VGA compatible I/O and memory address ranges. **Note that only one of device 1–2's VGAEN bits are allowed to be set. This must be enforced via software.** **VGAEN** / **MDAP** / **Description** 0 / 0 / All References to MDA and VGA space are routed to HI_A 0 / 1 / Illegal combination 1 / 0 / All VGA references are routed to this bus. MDA references are routed to HI_A 1 / 1 / All VGA references are routed to this bus. MDA references are routed to HI_A
2	0b R/W	**ISA Enable (ISAEN).** This bit modifies the response by the MCH to an I/O access issued by the processor that targets ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = Enable. All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions are mapped to AGP. (Default) 1 = Disable. MCH will not forward to AGP any I/O transactions addressing the last 768 bytes in each 1-KB block, even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to AGP, these cycles will be forwarded to HI_A where they can be subtractively or positively claimed by the ISA bridge.
1	0b R/W	**SERR Enable (SERREN).** This bit controls forwarding SERR# on the secondary interface to the primary interface. 0 = Disable. 1 = Enable. MCH generates SERR messages to HI_A when the SERR# pin on AGP/PCI is asserted and when the messages are enabled by the SERRE bit in the PCICMD1 register.
0	0b R/W	**Parity Error Response Enable (PEREN).** This bit controls MCH's response to data phase parity errors on AGP. Other types of error conditions can still be signaled via SERR messaging independent of this bit's state. 0 = Disable. Address and data parity errors on AGP are not reported via the MCH HI_A SERR messaging mechanism. 1 = Enable. G_PERR# is not implemented by the MCH. However, when this bit is set to 1, address and data parity errors detected on AGP are reported via the HI_A SERR messaging mechanism, if further enabled by SERRE1.

3.7.24 ERRCMD1—Error Command Register (D1:F0)

Address Offset: 40h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Set by drivers.

Bits	Default, Access	Description
7:4		Reserved
3	0b R/W	**SERR on AGP Access Outside of Graphics Aperture (OOGF).** 0 = Disable. Reporting of this condition is disabled. 1 = Enable. MCH generates a SERR special cycle over HI_A when an AGP access occurs to an address outside of the graphics aperture.
2	0b R/W	**SERR on Invalid AGP Access (IAAF).** 0 = Disable. The Invalid AGP Access condition is not reported. 0 = Enable. MCH generates a SERR special cycle over HI_A when an AGP access occurs to an address outside of the graphics aperture and either to the 640 KB – 1 MB range or above the top of low memory.
1	0b R/W	**SERR on Invalid Translation Table Entry (ITTEF).** 0 = Disable. Reporting of this condition is disabled. 1 = Enable. MCH generates a SERR special cycle over HI_A when an invalid translation table entry was returned in response to an AGP Access to the graphics aperture.
0	0b R/W	**SERR on Receiving Target Abort (SERTA).** SERR messaging for Device 1 is globally enabled in the PCICMD1 register. 0 = Disable. MCH does not assert a SERR message upon receipt of a target abort on AGP. 1 = Enable. MCH generates an SERR message over the hub interface upon receiving a target abort on AGP.

3.7.25 ERRSTS1—Error Status Register (D1:F0)

Address Offset: 42h
Default Value: 00h
Attribute: R/WC
Size: 8 bits

Set by drivers.

Note: Software writes a 1 to clear bits that are set.

Bits	Default, Access	Description
7:4		Reserved
3	0b R/WC	**AGP Access Outside of Graphics Aperture Flag (OOGF).** 1 = AGP access occurred to an address outside of the graphics aperture range. This bit will be set for accesses outside of the aperture for AGP 2.0 low- and high-priority cycles. It will not be set for AGP 3.0 async cycles.
2	0b R/WC	**Invalid AGP Access Flag (IAAF).** 1 = AGP access was attempted outside of the graphics aperture and either to the 640 KB – 1 MB range or above the top of low memory.
1	0b R/WC	**Invalid Graphics Aperture Translation Table Entry (ITTEF).** 1 = Invalid translation table entry was returned in response to an AGP access to the graphics aperture.
0		Reserved

3.7.26 AGPCAPID1—AGP Capability Identifier Register (D1:F0)

Address Offset: 60–63h
Default Value: 0035 0002h
Attribute: RO
Size: 32 bits

This register provides standard identifier for AGP capability. **Read by drivers.**

Bits	Default, Access	Description
31:24		Reserved
23:20	3h RO	**Major AGP Revision Number (MAJREV).** These bits provide a major revision number of AGP specification to which this version of MCH conforms. This field is hardwired to value of 0011b (i.e., implying *AGP Specification 3.0*).
19:16	5h RO	**Minor AGP Revision Number (MINREV).** These bits provide a minor revision number of AGP specification to which this version of MCH conforms. This number is hardwired to value of 0101 which implies that the revision is x.5. Together with major revision number this field identifies the MCH as an *AGP Specification 3.0* compliant device.
15:8	00h RO	**Next Capability Pointer (NCAPTR).** AGP capability is the first and the last capability described via the capability pointer mechanism; therefore, these bits are hardwired to 0 to indicate the end of the capability linked list.
7:0	02h RO	**AGP Capability ID (CAPID).** This field identifies the linked list item as containing AGP registers. This field has a value of 0000_0010b assigned by the PCI SIG. This value may be changed by the AGP BIOS Configuration register 1.

3.7.27 AGPSTAT1—AGP Status Register (D1:F0)

Address Offset: 64–67h
Default Value: see table below
Attribute: RO
Size: 32 bits

This register reports AGP device capability/status. **Read by drivers.**

Bits	Default, Access	Description
31:24	1Fh RO	**Request Queue (RQ).** Hardwired to 1Fh. This field contains the maximum number of AGP command requests the MCH is configured to manage. 1Fh = 32 outstanding AGP command requests maximum can be handled by the MCH.
23:16		Reserved
15:13	010b RO	**Async Request Size (ARQSZ).** This value is LOG2 of the optimum asynchronous request size in bytes minus 4 to be used with the MCH. 010 = 64 byte MCH cache line size.
12:10	000b RO	**Calibration Period.** 000 = 4 ms
9	1b RO	**Side Band Addressing Support (SBA).** Hardwired to 1. The MCH supports side band addressing. AGP 8x requires sideband addressing. This bit is reserved in the *AGP Specification 3.0*, and read only as a 1 to be compatible with the Device 0 register.
8	0b RO	**Inside the Aperture GART entry coherency** (I**TA_COH).** Hardwired to 0. The MCH does not support coherency based on the coherency bit in the GART entries.
7	0b RO	**64-bit GART support (GART64).** Hardwired to 0. The MCH supports 32 bit GART entries only. The 32 bit GART entries allows 36 bit support.
6	0b RO	**Host Translation support (HTRANS#).** Hardwired to 0. The MCH supports translating accesses from the host processor through the aperture.
5	0b RO	**Greater Than Four Gigabyte Support (GT4GIG).** Hardwired to 0. The MCH does not support addresses greater than 4-GB AGP.
4	1b RO	**Fast Write Support (FW).** Hardwired to 1. The MCH supports Fast Writes from the processor-to-AGP master. This bit is reserved in the *AGP Specification 3.0*, and read only as a 1 to be compatible with the Device 0 register.
3	x RO	**AGP 3.0 mode.** This bit is set by the hardware on reset based on the AGP 8x detection via the VREF Comparator. 0 = AGP 2.0 signaling mode (1.5 V). 1 = Graphics card is AGP 8x mode
2:0	111b or 01x RO	**Data Rate Support (RATE).** The value of this field is determined by the AGP 3.0 signaling mode bit above. In AGP 3.0 signaling mode (AGP 3.0 signaling mode = 1) these bits are 01X, indicating that 3.0 signaling mode is supported. Bit 0 is determined by BIOS. In AGP 2.0 signaling mode, these bits are 111 indicating that 1x, 2x, and 4x modes are all supported. **BIt 2** / **Bit 1** / **Bit 0** **2.0 Signaling (1.5 V)** Data Rate: 4x / 2x / 1x MCH Value: 1 (supported) / 1 (supported) / 1 (supported) **3.0 Signaling (0.8 V)** Data Rate: reserved / 8x / 4x MCH Value: 0 / 1 (supported) / Programmable **NOTE:** Signaling Mode is determined by bit 3 (AGP 3.0 signaling mode, above)

3.7.28 AGPCMD—AGP Command Register (D1:F0)

Address Offset: 68–6Bh
Default Value: 0000 0000h
Attribute: RO, R/W
Size: 32 bits

This register provides control of the AGP operational parameters. Set by drivers.

Bits	Default, Access	Description
31:13		Reserved
12:10	000b R/W	**Programmed Calibration Period (PCAL_Cycle).** These bits are programmed with the period for core-logic initiated bus cycles for calibrating the I/O buffers for both master and target. The default value is based on the MCH requirement. This value is updated with the smaller of the value in CAL_CYCLE from the master's and target's AGPSTAT register. Note that the MCHTST register bits 31:30 must be set to 2 ms for the setting in this register to be correct. 000 = 4 ms 001 = 16 ms 010 = 64 ms 011 = 256 ms 100–111 = Reserved for future use
9	0b R/W	**Side Band Addressing Enable (SBAEN).** 0 = Disable 1 = Enable. Side band addressing mechanism is enabled. **NOTE:** In AGP 3.0 signaling mode this bit is ignored as sideband addressing is the only allowed mechanism
8	0b R/W	**AGP Enable (AGPEN).** This bit enables/disables AGP. This bit also determines which device register set (Device 0 or Device 1) is used for AGP. 0 = Disable. MCH ignores all AGP operations, including the sync cycle. Any AGP operations received while this bit is set to 1 will be serviced even if this bit is reset to 0. If this bit transitions from 1-to-0 on a clock edge in the middle of an SBA command being delivered in 1x mode, the command will be issued. Device 0 register set is used. 1 = Enable. MCH responds to AGP operations delivered via PIPE# (AGP 2.0 signaling mode), or to operations delivered via SBA if the AGP side band enable bit is also set to 1. Device 1 register set is used. **NOTE:** This bit and the AGPEN bit in device 0 should not be set at the same time.
7	0b RO	**64-bit GART Support (GART64B).** Hardwired to 0. This indicates that the MCH supports only 32-bit GART entries (which are sufficient for 36-bit addressing). This bit also determines which register set (Device 0 set or Device 1 set) is used for AGP. When this bit is a 0, the Device 0 register set is used.
6		Reserved
5	0b RO	**Over 4-GB Support (OVER4G).** Hardwired to 0. MCH does not support addresses greater than 4 GB in AGP.

Bits	Default, Access	Description
4	0b R/W	**Fast Write Enable (FWEN).** 0 = Disable. When this bit it is 0 or when the data rate bits are set to 1x mode, the Memory Write transactions from the MCH to the AGP master use standard PCI protocol. 1 = Enable. MCH uses the Fast Write protocol for memory write transactions from the MCH to the AGP master. Fast Writes occur at the data transfer rate selected by the data rate bits (2:0) in this register. **NOTE:** In 8x mode this bit is ignored since AGP 8x requires fast writes be supported. This bit is functional in all modes except 1x mode.
3		Reserved
2:0	000b R/W	**Data Rate Enable (DRATE).** The setting of these bits determines the AGP data transfer rate. One (and only one) bit in this field must be set to indicate the desired data transfer rate. The same bit must be set on both master and target. The encoding is determined by the AGP 3.0 signaling mode bit in the AGPSTAT register. **Encoding** / **AGP 2.0 Signaling** / **AGP 3.0 Signaling** 000 / 1x Transfer mode / 4x Transfer mode 010 / 2x Transfer mode / 8x Transfer mode 100 / 4x Transfer mode / reserved

3.7.29 AGPCTRL1—AGP Control Register (D1:F0)

Address Offset: 70–73h
Default Value: 0000 0000h
Attribute: RO, R/W
Size: 32 bits

This register provides for additional control of the AGP interface. **Set by drivers.**

Bits	Default, Access	Description
31:10		Reserved
9	0b	**Calibration Disable.** 0 = Enable. 1 = Disable. Calibration cycle operation is disabled by the core logic. Note that calibration cycle should be automatically disabled by core-logic when not in AGP 3.0 signaling mode.
8		Reserved
7	0b R/W	**GTLB Enable (GTLBEN).** 0 = Disable (default). GTLB is flushed by clearing the valid bits associated with each entry. In this mode of operation all accesses that require translation bypass the GTLB. All requests that are positively decoded to the graphics aperture force the MCH to access the translation table in main memory before completing the request. Translation table entry fetches will not be cached in the GTLB. When an invalid translation table entry is read, this entry will still be cached in the GTLB (ejecting the least recently used entry). 1 = Enable. Enables normal operations of the Graphics Translation Look aside Buffer. **NOTE:** This bit can be changed dynamically (i.e., while an access to GTLB occurs); however, the completion of the configuration write that asserts or deasserts this bit will be delayed pending a complete flush of all dirty entries from the write buffer. This delay will be incurred because this bit is used as a mechanism to signal the chipset that the graphics aperture translation table is about to be modified or has completed modifications. In the first case, all dirty entries need to be flushed before the translation table is changed. In the second case, all dirty entries need to be flushed because one of them is likely to be a translation table entry which must be made visible to the GTLB by flushing it to memory.
6:0		Reserved

3.7.30 APSIZE1—AGP Aperture Size Register (D1:F0)

Address Offset:	74–75h
Default Value:	0000h
Attribute:	R/W
Size:	16 bits

This register determines the effective size of the Graphics Aperture used for a particular MCH configuration. This register can be updated by the MCH-specific BIOS configuration sequence before the PCI standard bus enumeration sequence takes place. If the register is not updated then a default value will select an aperture of maximum size (i.e., 256 MB). The size of the table that will correspond to a 256-MB aperture is not practical for most applications; therefore, these bits must be programmed to a smaller practical value that will force adequate address range to be requested via APBASE register from the PCI configuration software. **Set by BIOS.**

<table>
<tr><th>Bits</th><th>Default, Access</th><th>Description</th></tr>
<tr><td>15:6</td><td></td><td>Reserved</td></tr>
<tr><td>5:0</td><td>00 0000b
R/W</td><td>
Graphics Aperture Size (APSIZE). This register determines the aperture size. It controls bits in the APBASE register, determining which bits are read/write or read only such that PCI plug and play software will determine the proper size.
0 = When a bit in this register is a 0, the corresponding bit in the APBASE register will become read only as a 0.
1 = When a bit in this register is a 1, the corresponding bit in the APBASE register will be read/write.
<table>
<tr><td>APSIZE1 bit</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td></tr>
<tr><td>APBASE1 bit</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td></tr>
<tr><td>Aperture size when bits are 0</td><td>8 M (4 M, when a 1)</td><td>16 M</td><td>32 M</td><td>64 M</td><td>128 M</td><td>256 M</td></tr>
</table>
There must be a single contiguous range of aperture sizes from the table below (i.e., No gaps).
<table>
<tr><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th><th>Hex</th><th>Aperture Size</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>F3F</td><td>4 MB</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>F3E</td><td>8 MB</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>F3C</td><td>16 MB</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>F38</td><td>32 MB</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>F30</td><td>64 MB</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>F20</td><td>128 MB</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>F00</td><td>256 MB</td></tr>
</table>
</td></tr>
</table>

3.7.31 ATTBASE1—AGP GART Pointer Register (D1:F0)

Address Offset: 78–7Bh
Default Value: 0000 0000h
Attribute: R/W, RO
Size: 32 bits

This register determines the starting address of the GART table. It must be on a 4-KB boundary, regardless of its size. The size of the table is determined by the APSIZE1 register as shown in the table below. **Set by drivers.**

Bits	Default, Access	Description
31:12	00000h R/W	**Graphics Aperture Remapping Table Starting Address (GART).** Bits 31:12 correspond to address bits 31:12.
11:0		Reserved

3.8 Hub Interface_B PCI-to-PCI Bridge Registers (Device 2, Function 0)

The Hub Interface_B (HI_B) registers are in Device 2 (D2), Function 0 (F0). Table 3-6 provides the register address map for this device, function.

Warning: Address locations that are not listed the table are considered reserved register locations. Writes to "Reserved" registers may cause system failure. Reads to "Reserved" registers may return a non-zero value.

Table 3-6. Hub Interface_B PCI-to-PCI Register Map (D2:F0)

Address Offset	Mnemonic	Register Name	Default Value	Access
00–01h	VID2	Vendor Identification	8086h	RO
02–03h	DID2	Device Identification	2553h	RO
04–05h	PCICMD2	PCI Command	0000h	RO, RW
06–07h	PCIST2	PCI Status	00A0h	R/WC, RO
08h	RID2	Revision Identification	See register description	RO
0Ah	SUBC2	Sub Class Code	04h	RO
0Bh	BCC2	Base Class Code	06h	RO
0Dh	MLT2	Master Latency Timer (scratch pad)	00h	RO,RW
0Eh	HDR2	Header Type	01h or 81h	RO
18h	PBUSN2	Primary Bus Number	00h	RO
19h	SBUSN2	Secondary Bus Number	00h	RW
1Ah	SUBUSN2	Subordinate Bus Number	00h	RW
1Ch	IOBASE2	I/O Base Address	00h	RO
1Dh	IOLIMIT2	I/O Limit Address	F0h	RO,RW
1E–1Fh	SEC_STS2	Secondary Status	00h	RW
20–21h	MBASE2	Memory Base Address	02A0h	RO,R/WC
22–23h	MLIMIT2	Memory Limit Address	FFF0h	RO, RW
24–25h	PMBASE2	Prefetchable Memory Base Address	0000h	RO, RW
26–27h	PMLIMIT2	Prefetchable Memory Limit Address	FFF0h	RO, RW
3Eh	BCTRL2	Bridge Control	0000h	RO, RW

3.8.1 VID2—Vendor Identification Register (D2:F0)

Address Offset: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register combined with the Device Identification register uniquely identify any PCI device.

Bits	Default, Access	Description
15:0	8086h RO	**Vendor Identification Device 2 (VID2).** This register field contains the PCI standard identification for Intel, 8086h.

3.8.2 DID2—Device Identification Register (D2:F0)

Address Offset: 02–03h
Default Value: 2553h
Attribute: RO
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device.

Bits	Default, Access	Description
15:0	2553h RO	**Device Identification Number (DID).** This is a 16-bit value assigned to the MCH device 2, function 0.

3.8.3 PCICMD2—PCI Command Register (D2:F0)

Address Offset: 04–05h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Many of these bits are not applicable since the primary side of this device is not an actual PCI bus.

Bits	Default, Access	Description
15:10		Reserved
9	0b RO	**Fast Back-to-Back Enable (FB2B).** Hardwired to 0. Not Applicable.
8	0b R/W	**SERR Message Enable (SERRE).** This bit is a global enable bit for Device 2 SERR messaging. The MCH does not have an SERR# signal. The MCH communicates the SERR# condition by sending an SERR message to the Intel® ICH4. 0 = Disable. SERR message is not generated by the MCH for Device 2. 1 = Enable. MCH is enabled to generate SERR messages over HI_A for specific Device 2 error conditions.
7	0b RO	**Address/Data Stepping (ADSTEP).** Hardwired to 0. Not applicable.
6	0b RO	**Parity Error Enable (PERRE).** Hardwired to 0. Parity checking is not supported on the primary side of this device.
5		Reserved
4	0b RO	**Memory Write and Invalidate Enable (MWIE).** Hardwired to 0. Not applicable.
3	0b RO	**Special Cycle Enable (SCE).** Hardwired to 0. Not applicable.
2	0b R/W	**Bus Master Enable (BME).** This bit does not have a function. It is a Read/Write bit for compatibility with compliance testing software.
1	0b R/W	**Memory Access Enable (MAE).** 0 = Disable. All of device 2's memory space is disabled. 1 = Enable. Enables the Memory and Pre-fetchable memory address ranges defined in the MBASE2, MLIMIT2, PMBASE2, and PMLIMIT2 registers.
0	0b R/W	**IO Access Enable (IOAE).** 0 = Disable. All of device 2's I/O space is disabled. 1 = Enable. Enables the I/O address range defined in the IOBASE2 and IOLIMIT2 registers.

3.8.4 PCISTS2—PCI Status Register (D2:F0)

Address Offset: 06–07h
Default Value: 00A0h
Attribute: RO, R/WC
Size: 16 bits

PCISTS2 is a 16-bit status register that reports the occurrence of error conditions associated with the primary side of the virtual PCI-to-PCI bridge embedded within the MCH.

Note: Software writes a 1 to clear set bits.

Bits	Default, Access	Description
15	0b RO	**Detected Parity Error (DPE).** Hardwired to 0. Parity is not supported on the primary side of this device.
14	0b R/WC	**Signaled System Error (SSE).** 0 = No MCH Device 1 generated SERR message over HI_A. 1 = MCH Device 2 generated an SERR message over HI_A for any enabled Device 2 error condition.
13	0b RO	**Received Master Abort Status (RMAS).** Hardwired to 0. The concept of master abort does not exist on primary side of this device.
12	0b RO	**Received Target Abort Status (RTAS).** Hardwired to 0. The concept of target abort does not exist on primary side of this device.
11	0b RO	**Signaled Target Abort Status (STAS).** Hardwired to 0. The concept of target abort does not exist on primary side of this device.
10:9	00b RO	**DEVSEL# Timing (DEVT).** Hardwired to 00. The MCH does not support subtractive decoding devices on bus 0. Therefore, this bit field is hardwired to 00 to indicate that device 2 uses the fastest possible decode.
8	0b RO	**Master Data Parity Error Detected (DPD).** Hardwired to 0. Parity is not supported on the primary side of this device.
7	1b RO	**Fast Back-to-Back (FB2B).** Hardwired to 1. This indicates that fast back to back writes are always supported on this interface. While fast back to back selection has no meaning on the hub interface, this bit is 1 to prevent disabling of this function on downstream interfaces.
6		Reserved
5	1b RO	**66/60 MHz capability (CAP66).** Hardwired to 1. HI_B is capable of delivering data at a rate equal to that of any PCI66 device. Indicates to configuration software that downstream devices may also be effectively enabled for 66 MHz operation.
4:0		Reserved

3.8.5 RID2—Revision Identification Register (D2:F0)

Address Offset: 08h
Default Value: see table below
Attribute: RO
Size: 8 bits

This register contains the revision number of the MCH device 2.

Bits	Default, Access	Description
7:0	00h RO	**Revision Identification Number (RID).** This is an 8-bit value that indicates the revision identification number for the MCH device 2. It is always the same as the value in RID. 03h = B-0 Stepping

3.8.6 SUBC2—Sub-Class Code Register (D2:F0)

Address Offset: 0Ah
Default Value: 04h
Attribute: RO
Size: 8 bits

This register contains the Sub-Class Code for the MCH device 2.

Bits	Default, Access	Description
7:0	04h RO	**Sub-Class Code (SUBC).** This is an 8-bit value that indicates the category of Bridge into which device 2 of the MCH falls. 04h = PCI to PCI Bridge.

3.8.7 BCC2—Base Class Code Register (D2:F0)

Address Offset: 0Bh
Default Value: 06h
Attribute: RO
Size: 8 bits

This register contains the Base Class Code of the MCH device 2.

Bits	Default, Access	Description
7:0	06h RO	**Base Class Code (BASEC).** This is an 8-bit value that indicates the Base Class Code for the MCH device 2. 06h = Bridge device

3.8.8 MLT2—Master Latency Timer (Scratch Pad) Register (D2:F0)

Address Offset: 0Dh
Default Value: 00h
Attribute: R/W, RO
Size: 8 bits

This functionality is not applicable. It is described here since these bits should be implemented as a read/write to prevent standard PCI-to-PCI bridge configuration software from getting "confused."

Bits	Default, Access	Description
7:3	00000b R/W	**Scratch pad MLT (NA7.3).** These bits return the value with which they are written; however, they have no internal function and are implemented as a scratch pad to avoid confusing software.
2:0		Reserved

3.8.9 HDR2—Header Type Register (D2:F0)

Address Offset: 0Eh
Default Value: 01h or 81h
Attribute: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bits	Default, Access	Description
7:0	01h or 81h RO	**Header Type Register (HDR). This read only field indicates whether Device 2 is a multi-function device.** 01 = Single Function device (Function 1 is disabled in Device 0, offset E0h) with bridge layout. 81 = Multi Function device (Function 1 is enabled in Device 0, offset E0h) with bridge layout.

3.8.10 PBUSN2—Primary Bus Number Register (D2:F0)

Address Offset: 18h
Default Value: 00h
Attribute: RO
Size: 8 bits

This register identifies that virtual PCI-to-PCI bridge is connected to bus #0.

Bits	Default, Access	Description
7:0	00h RO	**Primary Bus Number (BUSN).** Hardwired to 00h. Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since device 2 is an internal device and its primary bus is always 0, these bits are read only as 00h.

3.8.11 SBUSN2—Secondary Bus Number Register (D2:F0)

Address Offset: 19h
Default Value: 00h
Attribute: R/W
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the virtual PCI-to-PCI bridge (the HI_B connection). This number is programmed by the PCI configuration software to allow mapping of configuration cycles to a second bridge device connected to HI_B.

Bits	Default, Access	Description
7:0	00h R/W	**Secondary Bus Number (BUSN).** This field is programmed by configuration software with the lowest bus number of the busses connected to HI_B. Since both bus 0, device 2 and the PCI-to-PCI bridge on the other end of the hub interface are considered by configuration software to be PCI bridges, this bus number will always correspond to the bus number assigned to HI_B.

3.8.12 SUBUSN2—Subordinate Bus Number Register (D2:F0)

Address Offset: 1Ah
Default Value: 00h
Attribute: R/W
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below the secondary hub interface. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to devices subordinate to the secondary hub interface port.

Bits	Default, Access	Description
7:0	00h R/W	**Subordinate Bus Number (BUSN).** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the device 2 bridge.

3.8.13 IOBASE2—I/O Base Address Register (D2:F0)

Address Offset: 1Ch
Default Value: F0h
Attribute: R/W, RO
Size: 8 bits

This register control the processor-to-HI_B I/O access routing based on the following formula:

IO_BASE2 ≤ address ≤ IO_LIMIT2

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A11:0 are treated as 0. Thus, the bottom of the defined I/O address range will be aligned to a 4-KB boundary.

Bits	Default, Access	Description
7:4	Fh R/W	**I/O Address Base (IOBASE2).** These bits corresponds to A15:12 of the I/O addresses passed by the device 2 bridge to HI_B
3:0		Reserved

3.8.14 IOLIMIT2—I/O Limit Address Register (D2:F0)

Address Offset: 1Dh
Default Value: 00h
Attribute: R/W
Size: 8 bits

This register controls the processor-to-HI_B I/O access routing based on the following formula:

IO_BASE2 ≤ address ≤ IO_LIMIT2

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A11:0 are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-KB aligned address block.

Bits	Default, Access	Description
7:4	0h R/W	**I/O Address Limit (IOLIMIT2).** These bits corresponds to A15:12 of the I/O address limit of device 2. Devices between this upper limit and IOBASE2 will be passed to HI_B.
3:0		Reserved

3.8.15 SEC_STS2—Secondary Status Register (D2:F0)

Address Offset:	1E–1Fh
Default Value:	02A0h
Attribute:	R/WC, RO
Size:	16 bits

SSTS2 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e., HI_B side) of the virtual PCI-to-PCI bridge in the MCH.

Note: Software writes a 1 to clear bits that are set.

Bits	Default, Access	Description
15	0b R/WC	**Detected Parity Error (2DPE).** 0 = No error for reported condition 1 = MCH detected a parity error in the address or data phase of HI_B bus transactions.
14	0b R/WC	**Received System Error (2RSE).** 0 = No error for reported condition 1 = MCH receives an SERR message on HI_B.
13	0b R/WC	**Received Master Abort Status (2RMAS).** 0 = No received Master Abort completion packet on HI_B. 1 = MCH received a Master Abort completion packet on HI_B.
12	0b R/WC	**Received Target Abort Status (2RTAS).** 0 = No received Target Abort completion packet on HI_B. 1 = MCH received a Target Abort completion packet on HI_B.
11	0b RO	**Signaled Target Abort Status (STAS).** Hardwired to 0. MCH does not generate target aborts on HI_B.
10:9	01b RO	**DEVSEL# Timing (DEVT).** Hardwired to 01. This concept is not supported on HI_B.
8	0b RO	**Master Data Parity Error Detected (DPD).** Hardwired to 0. The MCH does not implement PERR messaging on HI_B.
7	1b RO	**Fast Back-to-Back (FB2B).** Hardwired to 0. This concept is not supported on HI_B.
6		Reserved
5	1b RO	**66/60 MHz capability (CAP66).** Hardwired to 1. This indicates that HI_B is enabled for 66 MHz operation.
4:0		Reserved

3.8.16 MBASE2—Memory Base Address Register (D2:F0)

Address Offset: 20–21h
Default Value: FFF0h
Attribute: R/W, RO
Size: 16 bits

This register controls the processor-to-HI_B non-prefetchable memory access routing based on the following formula:

MEMORY_BASE2 ≤ address ≤ MEMORY_LIMIT2

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A31:20 of the 32-bit address. The bottom 4 bits of this register are read only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A19:0 are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bits	Default, Access	Description
15:4	FFFh R/W	**Memory Address Base (MBASE).** These bits corresponds to A31:20 of the lower limit of the memory range that will be passed by the device 2 bridge to HI_B
3:0		Reserved

3.8.17 MLIMIT2—Memory Limit Address Register (D2:F0)

Address Offset: 22–23h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

This register controls the processor-to-HI_B non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A31:20 of the 32-bit address. The bottom four bits of this register are read only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A19:0 are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Bits	Default, Access	Description
15:4	000h R/W	**Memory Address Limit (MILIMIT).** These bits corresponds to A31:20 of the memory address that corresponds to the upper limit of the range of memory accesses that will be passed by the device 2 bridge to HI_B.
3:0		Reserved

3.8.18 PMBASE2—Prefetchable Memory Base Address Register (D2:F0)

Address Offset: 24–25h
Default Value: FFF0h
Attribute: R/W, RO
Size: 16 bits

This register controls the processor-to-HI_B prefetchable memory accesses. The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A31:20 of the 36-bit address. For the purpose of address decode, bits A19:0 are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bits	Default, Access	Description
15:4	FFFh R/W	**Prefetchable Memory Address Base (PMBASE).** These bits corresponds to A31:20 of the lower limit of the address range passed by bridge device 2 across HI_B.
3:0		Reserved. Hardwired to 0h. The MCH does not support Out Bound 64-bit addressing.

3.8.19 PMLIMIT2—Prefetchable Memory Limit Address Register (D2:F0)

Address Offset: 26–27h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

This register controls the processor-to-HI_B prefetchable memory accesses. The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A31:20 of the 36-bit address. For the purpose of address decode, bits A19:0 are assumed to be FFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Bits	Default, Access	Description
15:4	000h R/W	**Prefetchable Memory Address Limit (PMLIMIT).** These bits corresponds to A31:20 of the upper limit of the address range passed by bridge device 2 across HI_B
3:0		Reserved. Hardwired to 0h. The MCH does not support Out Bound 64-bit addressing.

3.8.20 BCTRL2—Bridge Control Register (D2:F0)

Address Offset: 3Eh
Default Value: 00h
Attribute: RO, R/W
Size: 8 bits

This register provides extensions to the PCICMD2 register that are specific to PCI-to-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., HI_B) as well as some bits that affect the overall behavior of the virtual PCI-to-PCI bridge in the MCH (e.g., VGA compatible address range mapping).

Bits	Default, Access	Description
7	0b RO	**Fast Back-to-Back Enable (FB2BEN).** Hardwired to 0. The MCH does not generate fast back-to-back cycles as a master on HI_B.
6	0b RO	**Secondary Bus Reset (SRESET).** Hardwired to 0. MCH does not support generation of reset via this bit on the HI_B.
5	0b RO	**Master Abort Mode (MAMODE).** Hardwired to 0. Thus, the MCH, when acting as a master on HI_B, will drop writes and return all 1s during reads when a Master Abort occurs.
4		Reserved
3	0b R/W	**VGA Enable (VGAEN).** This bit controls the routing of processor-initiated transactions targeting VGA compatible I/O and memory address ranges. 0 = Disable. 1 = Enable. **NOTE:** Only one PCI-to-PCI Bridge VGAEN bits are allowed to be set. This must be enforced via software.
2	0b R/W	**ISA Enable (ISAEN).** This bit modifies the response by the MCH to an I/O access issued by the processor that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = Disable (default). All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions will be mapped to HI_B. 1 = MCH does not forward to HI_B any I/O transactions addressing the last 768 bytes in each 1-KB block, even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to HI_B, these cycles are forwarded to HI_A where they can be subtractively or positively claimed by the ISA bridge.
1	0b R/W	**SERR Enable (2SERRE).** This bit enables or disables forwarding of SERR messages from HI_B to HI_A, where they can be converted into interrupts that are eventually delivered to the processor. 0 = Disable. 1 = Enable.
0	0b R/W	**Parity Error Response Enable (2PERRE).** This bit controls MCH's response to data phase parity errors on HI_B. 0 = Address and data parity errors on HI_B are not reported via the MCH HI_A SERR messaging mechanism. Other types of error conditions can still be signaled via SERR messaging independent of this bit's state. 1 = Address and data parity errors on HI_B are reported via the HI_A SERR messaging mechanism, if further enabled by SERRE2.

3.9 Hub Interface_B PCI-to-PCI Bridge Error Reporting Registers (Device 2, Function 1)

The Hub Interface_B (HI_B) error reporting registers are in Device 2 (D2), Function 1 (F1). Table 3-7 provides the register address map for this device, function.

Warning: Address locations that are not listed the table are considered reserved register locations. Writes to “Reserved” registers may cause system failure. Reads to “Reserved” registers may return a non-zero value.

Table 3-7. Hub Interface_B – PCI-to-PCI Bridge Error Reporting Register Address Map (D2:F1)

Address Offset	Mnemonic	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	2554h	RO
04–05h	PCICMD	PCI Command	0000h	RO, RW
06–07h	PCISTS	PCI Status	0000h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
0Ah	SUBC	Sub Class Code	00h	RO
0Bh	BCC	Base Class Code	FFh	RO
0Eh	HDR	Header Type	0000h	R/WO
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	R/WO
80h	HIB_FERR	HI_B First Errors	00h	R/WC
82h	HIB_NERR	HI_B Next Errors	00h	R/WC
A0h	SERRCMD2	SERR Command	00h	RO, RW
A2h	SMICMD2	SMI Command	00h	RO, RW
A4h	SCICMD2	SCI Command	00h	RO, RW

3.9.1 VID—Vendor Identification Register (D2:F1)

Address Offset: 00–01h
Default Value: 8086h
Sticky No
Attribute: RO
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register combined with the Device Identification register uniquely identify any PCI device.

Bits	Default, Access	Description
15:0	8086h RO	**Vendor Identification (VID).** This register field contains the PCI standard identification for Intel, 8086h.

3.9.2 DID—Device Identification Register (D2:F1)

Address Offset: 02–03h
Default Value: 2554h
Sticky No
Attribute: RO
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device.

Bits	Default, Access	Description
15:0	2554h RO	**Device Identification Number (DID).** This is a 16 bit value assigned to the MCH Host-HI_B Function 1.

3.9.3 PCICMD—PCI Command Register (D2:F1)

Address Offset: 04–05h
Default Value: 0000h
Sticky No
Attribute: RO, R/W
Size: 16 bits

Bits	Default, Access	Description
15:9		Reserved
8	0b R/W	**SERR Enable (SERRE).** This bit is a global enable bit for Device 2 SERR messaging. The MCH does not have an SERR# signal. The MCH communicates the SERR condition by sending an SERR message over HI_A to the Intel® ICH4. 0 = Disable. SERR message is not generated by the MCH for Device 2 1 = Enable. MCH is enabled to generate SERR messages over HI_A for specific Device 2 error conditions that are individually enabled in the SERRCMD2 register. The error status is reported in the FERR/NERR and PCISTS registers.
7:0		Reserved

3.9.4 PCISTS—PCI Status Register (D2:F1)

Address Offset: 06–07h
Default Value: 0000h
Sticky No
Attribute: RO, R/WC
Size: 16 bits

Bits	Default, Access	Description
15		Reserved
14	0b R/WC	**Signaled System Error (SSE).** Software sets this bit to 0 by writing a 1 to it. 0 = MCH Device 2 Did **Not** generate SERR message over HI-A. 1 = MCH Device 2 generated an SERR message over HI_A for any enabled Device 2 error condition. Device 2 error conditions are enabled in the PCICMD and SERRCMD2 registers. Device 2 error flags are read/reset from the PCISTS or FERR/NERR registers.
13:0		Reserved

3.9.5 RID—Revision Identification Register (D2:F1)

Address Offset:	08h
Default Value:	see table below
Sticky	No
Attribute:	RO
Size:	8 bits

This register contains the revision number of the MCH Device 0. These bits are read only and writes to this register have no effect.

Bits	Default, Access	Description
7:0	00h RO	**Revision Identification Number (RID).** This is an 8-bit value that indicates the revision identification number for the MCH Device 0. This number should always be the same as the RID for function 0. 03h = B-0 Stepping

3.9.6 SUBC—Sub-Class Code Register (D2:F1)

Address Offset:	0Ah
Default Value:	00h
Sticky	No
Attribute:	RO
Size:	8 bits

Bits	Default, Access	Description
7:0	00h RO	**Sub-Class Code (SUBC).** This is an 8-bit value that indicates the category of undefined. The code is 00h.

3.9.7 BCC—Base Class Code Register (D2:F1)

Address Offset:	0Bh
Default Value:	FFh
Sticky	No
Attribute:	RO
Size:	8 bits

Bits	Default, Access	Description
7:0	FFh RO	**Base Class Code (BASEC).** This is an 8-bit value that indicates the Base Class Code for the MCH. FFh =Non-defined" device. Since this function is used for error conditions, it does not fall into any other class.

3.9.8 HDR—Header Type Register (D2:F1)

Address Offset: 0Eh
Default Value: 00h
Sticky No
Attribute: RO
Size: 8 bits

Bits	Default, Access	Description
7:0	00h RO	**PCI Header (HDR).** Reads and writes to this location have no effect.

3.9.9 SVID—Subsystem Vendor Identification Register (D2:F1)

Address Offset: 2C–2Dh
Default Value: 0000h
Sticky No
Attribute: R/WO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bits	Default, Access	Description
15:0	0000h R/WO	**Subsystem Vendor ID (SUBVID).** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

3.9.10 SID—Subsystem Identification Register (D2:F1)

Address Offset: 02E–2Fh
Default Value: 0000h
Sticky No
Attribute: R/WO
Size: 16 bits

This value is used to identify a particular subsystem.

Bits	Default, Access	Description
15:0	0000h R/WO	**Subsystem ID (SUBID).** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

3.9.11 HIB_FERR—HI_B First Error Register (D2:F1)

Address Offset:	80h
Default Value:	00h
Sticky	Yes
Attribute:	R/WC
Size:	8 bits

This register store the FIRST error related to the HI_B interface. Only one error bit will be set in this register. Any future errors (NEXT Errors) will be set in the HIB_NERR register. No further error bits in this register will be set until the existing error bit is cleared.

Note: Software must write a 1 to clear bits that are set.

Bits	Default, Access	Description
7		Reserved
6	0b R/WC	**MCH Received SERR From HI_B.** 0 = No SERR from HI_B detected. 1 = MCH detected a SERR on Hub Interface_B.
5	0b R/WC	**MCH Master Abort on HI_B (HIBMA).** MCH did a master abort to a HI_B request. 0 = No Master Abort on HI_B detected. 1 = MCH detected an invalid address that will be master aborted. This bit is set even when the MCH does not respond with the Master Abort completion packet.
4	0b R/WC	**Received Target Abort on HI_B.** 0 = No Target Abort on HI_B detected. 1 = MCH detected that an MCH originated cycle was terminated with a Target Abort completion packet.
3	0b R/WC	**Correctable Error on Header/Address from HI_B.** 0 = No correctable error on header/address from HI_B detected. 1 = Even when error correction is turned off, this bit may be set if a packet is received that has a single bit correctable error.
2	0b R/WC	**Correctable Error on Data from HI_B.** 0 = No correctable error on data from HI_B detected. 1 = Even when error correction is turned off, this bit may be set if a packet is received that has a single bit correctable error.
1	0b R/WC	**Uncorrectable Error on Header/Address from HI_B.** 0 = No uncorrectable error on header/address from HI_B detected. 1 = Even when error correction is turned off, this bit may be set if a packet is received that has a multi-bit uncorrectable error.
0	0b R/WC	**Uncorrectable Error on Data Transfer from HI_B.** 0 = No uncorrectable error on data from HI_B detected. 1 = Even when error correction is turned off, this bit may be set if a packet is received that has a multi-bit uncorrectable error.

3.9.12 HIB_NERR—HI_B Next Error Register (D2:F1)

Address Offset: 82h
Default Value: 00h
Sticky Yes
Attribute: R/WC
Size: 8 bits

The FIRST error related to HI_B will be stored in the HIB_FERR Register. This register store all future errors related to the HI_B. Multiple bits in this register may be set.

Note: Software must write a 1 to clear bits that are set.

Bits	Default, Access	Description
7		Reserved
6	0b R/WC	**MCH Received SERR from HI_B.** 0 = No SERR from HI_B received. 1 = MCH received SERR from HI_B.
5	0b R/WC	**MCH Master Abort on HI_B (HIBMA).** MCH did a Master Abort to a HI_B Request. 0 = No Master Abort on HI_B detected. 1 = The MCH detected an invalid address that will be master aborted. This bit is set even when the MCH does not respond with the Master Abort completion packet.
4	0b R/WC	**Received Target Abort on HI_B.** 0 = No Target Abort detected. 1 = The MCH has detected that an MCH originated cycle was terminated with a Target Abort completion packet.
3	0b R/WC	**Correctable Error on Header/Address from HI_B.** 0 = No correctable error on header/address from HI_B detected. 1 = Even when error correction is turned off, this bit may be set if a packet is received that has a single bit correctable error.
2	0b R/WC	**Correctable Error on Data from HI_B.** 0 = No correctable error on data from HI_B detected. 1 = Even when error correction is turned off, this bit may be set if a packet is received that has a single bit correctable error.
1	0b R/WC	**Uncorrectable Error on Header/Address from HI_B.** 0 = No uncorrectable error on header/address from HI_B detected. 1 = Even when error correction is turned off, this bit may be set if a packet is received that has a multi-bit uncorrectable error.
0	0b R/WC	**Uncorrectable Error on Data Transfer from HI_B.** 0 = No uncorrectable error on data from HI_B detected. 1 = Even when error correction is turned off, this bit may be set if a packet is received that has a multi-bit uncorrectable error.

3.9.13 SERRCMD2—SERR Command Register (D2:F1)

Address Offset: A0h
Default Value: 00h
Sticky No
Attribute: RO, R/W
Size: 8 bits

This register determines whether SERR will be generated when the associated flag is set in FERR or NERR. When an error flag is set in the FERR or NERR Register, it can generate an SERR, SMI, or SCI when enabled in the SERRCMD, SMICMD, or SCICMD Registers, respectively. Only one message type can be enabled.

Bits	Default, Access	Description
7:6		Reserved
5	R/W 0b	**SERR on MCH Master Abort to a HI_B Request Enable.** 0 = No SERR generation 1 = Generate SERR if bit 5 is set in HIB_FERR or HIB_NERR
4	R/W 0b	**SERR on Received Target Abort on HI_B Enable.** 0 = No SERR generation 1 = Generate SERR if bit 4 is set in HIB_FERR or HIB_NERR
3	R/W 0b	**SERR on Correctable Error on Header/Address from HI_B Enable.** 0 = No SERR generation 1 = Generate SERR if bit 3 is set in HIB_FERR or HIB_NERR
2	R/W 0b	**SERR on Correctable Error on Data from HI_B Enable.** 0 = No SERR generation 1 = Generate SERR if bit 2 is set in HIB_FERR or HIB_NERR
1	R/W 0b	**SERR on Uncorrectable Error on Header/Address from HI_B Enable.** 0 = No SERR generation 1 = Generate SERR if bit 1is set in HIB_FERR or HIB_NERR
0	R/W 0b	**SERR on Uncorrectable Error on Data Transfer from HI_B Enable.** 0 = No SERR generation 1 = Generate SERR if bit 0 is set in HIB_FERR or HIB_NERR

3.9.14 SMICMD2—SMI Command Register (D2:F1)

Address Offset: A2h
Default Value: 00h
Sticky No
Attribute: RO, R/W
Size: 8 bits

This register determines whether SMI will be generated when the associated flag is set in FERR or NERR. When an error flag is set in the FERR or NERR Register, it can generate an SERR, SMI, or SCI when enabled in the SERRCMD, SMICMD, or SCICMD Registers, respectively. Only one message type can be enabled.

Bits	Default, Access	Description
7		Reserved
6	R/W 0b	**SMI on MCH Received SERR from HI_B Enable.** 0 = No SMI generation 1 = Generate SMI if bit 6 is set in HIB_FERR or HIB_NERR
5	R/W 0b	**SMI on MCH Master Abort to a HI_B Request Enable.** 0 = No SMI generation 1 = Generate SMI if bit 5 is set in HIB_FERR or HIB_NERR
4	R/W 0b	**SMI on Received Target Abort on HI_B Enable.** 0 = No SMI generation 1 = Generate SERR if bit 4 is set in HIB_FERR or HIB_NERR
3	R/W 0b	**SMI on Correctable Error on Header/Address from HI_B Enable.** 0 = No SMI generation 1 = Generate SMI if bit 3 is set in HIB_FERR or HIB_NERR
2	R/W 0b	**SMI on Correctable Error on Data from HI_B Enable.** 0 = No SMI generation 1 = Generate SMI if bit 2 is set in HIB_FERR or HIB_NERR
1	R/W 0b	**SMI on Uncorrectable Error on Header/Address from HI_B Enable.** 0 = No SMI generation 1 = Generate SMI if bit 1is set in HIB_FERR or HIB_NERR
0	R/W 0b	**SMI on Uncorrectable Error on Data Transfer from HI_B Enable.** 0 = No SMI generation 1 = Generate SMI if bit 0 is set in HIB_FERR or HIB_NERR

3.9.15 SCICMD2—SCI Command Register (D2:F1)

Address Offset: A4h
Default Value: 00h
Sticky No
Attribute: RO, R/W
Size: 8 bits

This register determines whether SCI will be generated when the associated flag is set in the FERR or NERR Register. When an error flag is set in the FERR or NERR Register, it can generate an SERR, SMI, or SCI when enabled in the ERRCMD, SMICMD, or SCICMD Registers, respectively. Only one message type can be enabled.

Bits	Default, Access	Description
7		Reserved
6	R/W 0b	**SCI on MCH Received SERR from HI_B Enable.** 0 = No SCI generation 1 = Generate SCI if bit 6 is set in HIB_FERR or HIB_NERR
5	R/W 0b	**SCI on MCH Master Abort to a HI_B Request Enable.** 0 = No SCI generation 1 = Generate SCI if bit 5 is set in HIB_FERR or HIB_NERR
4	R/W 0b	**SCI on Received Target Abort on HI_B Enable.** 0 = No SCI generation 1 = Generate SCI if bit 4 is set in HIB_FERR or HIB_NERR
3	R/W 0b	**SCI on Correctable Error on Header/Address from HI_B Enable.** 0 = No SCI generation 1 = Generate SCI if bit 3 is set in HIB_FERR or HIB_NERR
2	R/W 0b	**SCI on Correctable Error on Data from HI_B Enable.** 0 = No SCI generation 1 = Generate SCI if bit 2 is set in HIB_FERR or HIB_NERR
1	R/W 0b	**SCI on Uncorrectable Error on Header/Address from HI_B Enable.** 0 = No SCI generation 1 = Generate SCI if bit 1is set in HIB_FERR or HIB_NERR
0	R/W 0b	**SCI on Uncorrectable Error on Data Transfer from HI_B Enable.** 0 = No SCI generation 1 = Generate SCI if bit 0 is set in HIB_FERR or HIB_NERR

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System Address Map 4

A system based on the E7505 chipset supports 16 GB–64 MB (see note) of host-addressable memory space and 64 KB + 3 of host-addressable I/O space. The I/O and memory spaces are divided by system configuration software into regions. The memory ranges are useful either as system memory or as specialized memory, while the I/O regions are used to control the operation of devices in the system.

Note: The maximum usable memory address decode is 15.94 GB (16 GB–64MB)

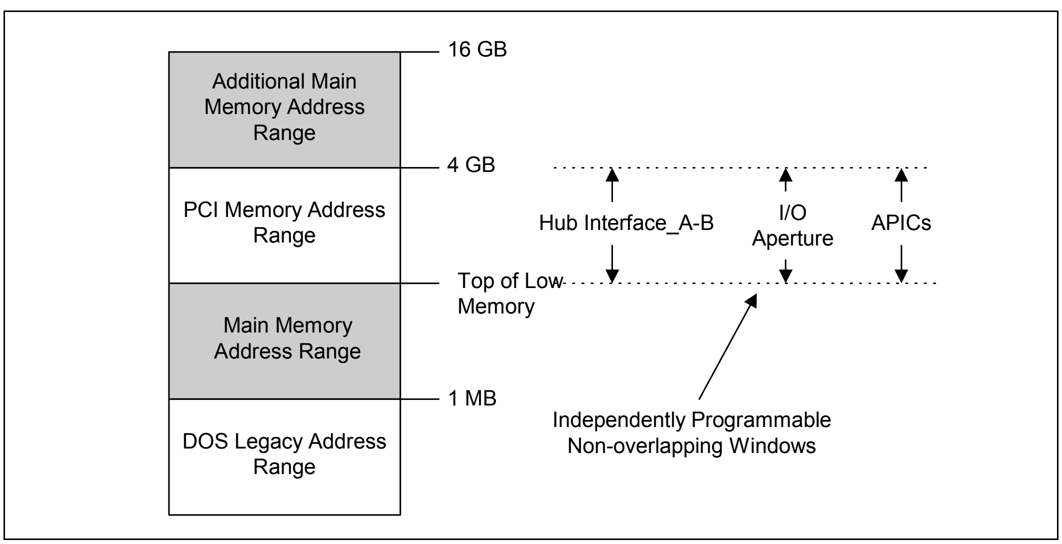
4.1 System Memory Spaces

There are four basic regions of memory in the system:

- High Memory Range. Memory above 4 GB. This memory range is for additional main memory (1_0000_0000h to 3_FFFF_FFFFh).
- Memory between the TOLM Register and 4 GB. This range is used for mapping APIC and Hub Interface_A–B. Programmable non-overlapping I/O windows can be mapped to this area.
- Memory between 1 MB and the Top of Low Memory (TOLM) Register. This is a main memory address range (0_0100_0000h to TOLM).
- DOS Compatible memory area. Memory below 1 MB (0_0000_0000h to 0_0009_FFFFh).

The DRAM that physically overlaps the PCI Memory Address Range is recovered by the system. For example, if there is 4 GB of physical DRAM and 1 GB of PCI space, then the system can address a total of 5 GB. In this instance the top GB of physical DRAM is addressed between 4 GB and 5 GB by the system.

Figure 4-1. System Memory Address Map



These address ranges are always mapped to system memory, regardless of the system configuration. Memory may be allocated from the main memory segment (0_0100_0000h to TOLM) for use by System Management Mode (SMM) hardware and software. The top of main memory is defined by the Top of Low Memory (TOLM) register. Note that the address of the highest 64-MB (dual channel) quantity of valid memory in the system is placed into the DRB7 register (32 MB for single channel). For systems with a total DRAM space and PCI memory-mapped space of less than 4 GB, this value will be the same as the one programmed into the TOLM register. For other memory configurations, the two are unlikely to be the same, since the PCI configuration portion of the BIOS software will program the TOLM register to the maximum value that is less than 4 GB and also allows enough room for all populated PCI devices. The MCH does not allow AGP memory or the aperture above 4 GB. Figure 4-2 shows the memory segments below 1 MB. Figure 4-3 shows the memory segments in the extended memory range (1 MB to 4 GB).

Figure 4-2. Detailed Memory Address Map (Below 1 MB)

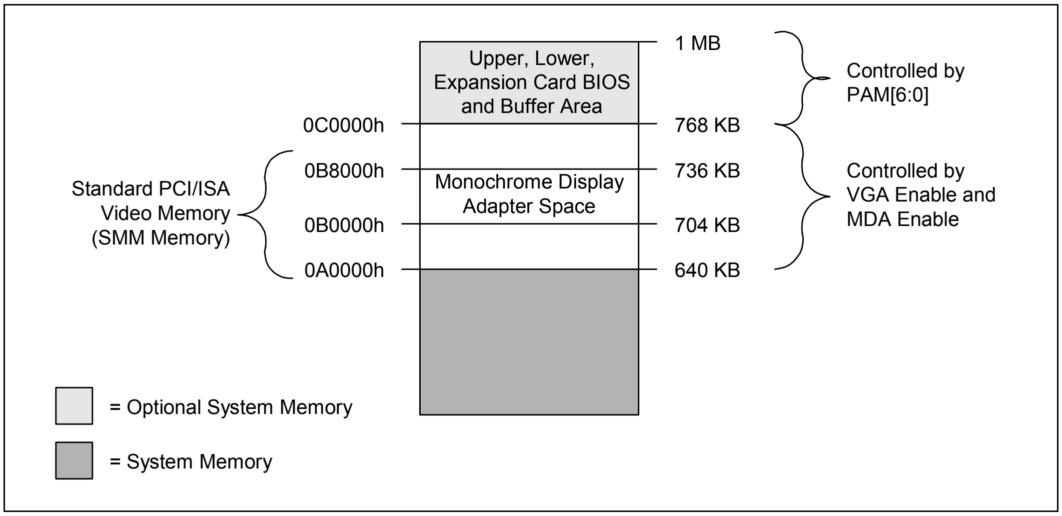
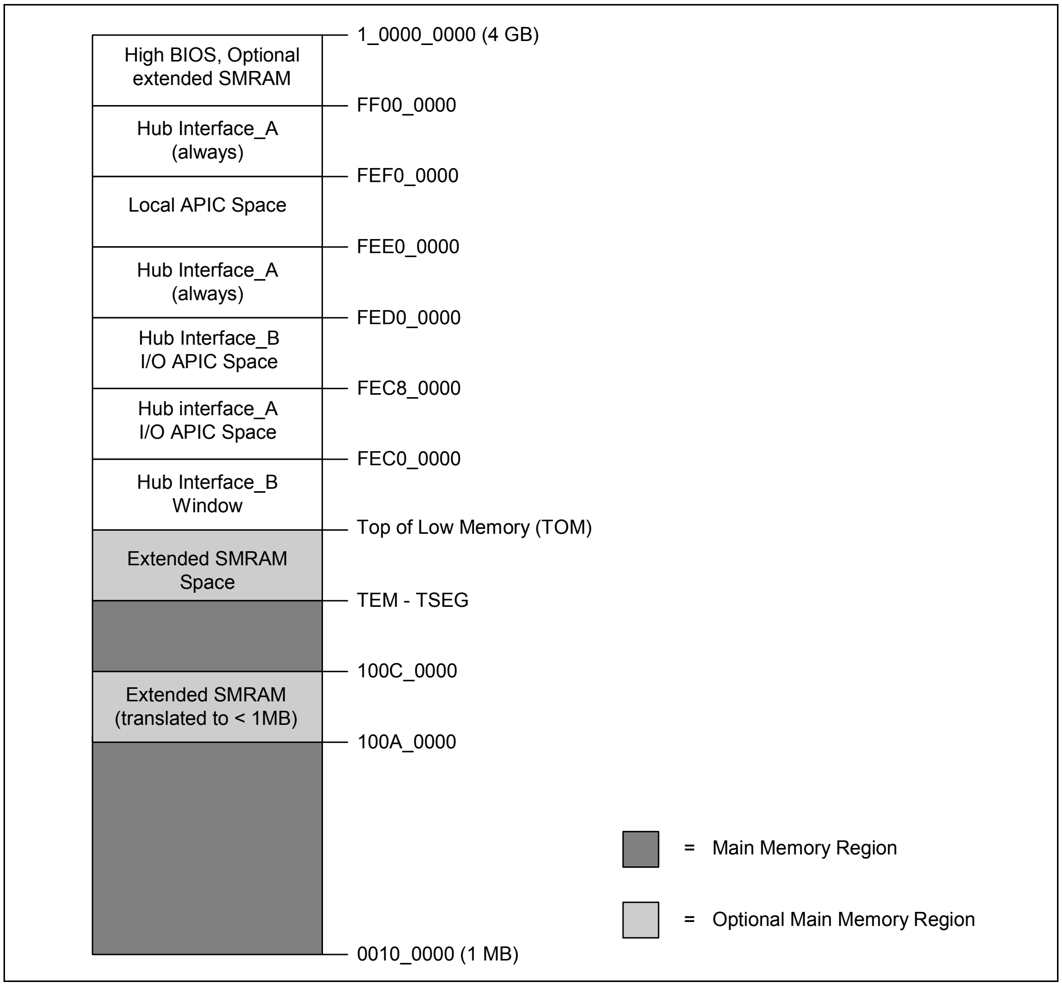


Figure 4-3. Detailed Extended Memory Address Map (1 MB to 4 GB)



4.1.1 VGA and MDA Memory Spaces

Video cards use these legacy address ranges to map a frame buffer or a character-based video buffer. The address ranges in this memory space are:

- VGAA 0_000A_0000h to 0_000A_FFFFh
- MDA 0_000B_0000h to 0_000B_7FFFh
- VGAB 0_000B_8000h to 0_000B_FFFFh

By default, accesses to these ranges are forwarded to HI_A. However, if the VGA_EN bit is set in the BCTRL configuration register, then transactions within the VGA and MDA spaces are sent to AGP or HI_B, respectively.

Note: The VGA_EN bit may be set in one and only one of the BCTRL Registers. Software must not set more than one of the VGA_EN bits.

If the configuration bit MCHCFG. MDAP is set, then accesses that fall within the MDA range will be sent to HI_A without regard for the VGAEN bits. Legacy support requires the ability to have a second graphics controller (monochrome) in the system. In a MCH based-system, accesses in the standard VGA range are forwarded to AGP or HI_B (depending on configuration bits). Since the monochrome adapter may be on the HI_A/PCI (or ISA) bus, the MCH must decode cycles in the MDA range and forward them to HI_A. This capability is controlled by a configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the MCH decodes I/O cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to HI_A.

An optimization allows the system to reclaim the memory displaced by these regions. If SMM memory space is enabled by SMRAM.G_SMRARE and either the SMRAM.D_OPEN bit is set or the processor bus receives an SMM-encoded request for code (not data), then the transaction is steered to system memory rather than HI_A. Under these conditions, both the VGAEN bits and the MDAP bit are ignored.

If any VGAEN is set, then all ISAEN must be set. The PCI specification defines VGAEN to be a 10-bit decode. Therefore, the other peer bridges must also be 10-bit decodes (ISAEN), so that two or more devices do not claim the same access.

4.1.2 PAM Memory Spaces

The address ranges in this space are:

- PAMC0 0_000C_0000 to 0_000C_3FFF
- PAMC4 0_000C_4000 to 0_000C_7FFF
- PAMC8 0_000C_8000 to 0_000C_BFFF
- PAMCC 0_000C_C000 to 0_000C_FFFF
- PAMD0 0_000D_0000 to 0_000D_3FFF
- PAMD4 0_000D_4000 to 0_000D_7FFF
- PAMD8 0_000D_8000 to 0_000D_BFFF
- PAMDC 0_000D_C000 to 0_000D_FFFF
- PAME0 0_000E_0000 to 0_000E_3FFF
- PAME4 0_000E_4000 to 0_000E_7FFF
- PAME8 0_000E_8000 to 0_000E_BFFF
- PAMEC 0_000E_C000 to 0_000E_FFFF
- PAMF0 0_000F_0000 to 0_000F_FFFF

The 256 KB PAM region is divided into three parts:

- ISA expansion region: 128 KB area between 0_000C_0000h and 0_000D_FFFFh
- Extended BIOS region: 64 KB area between 0_000E_0000h and 0_000E_FFFFh,
- System BIOS region: 64 KB area between 0_000F_0000h and 0_000F_FFFFh.

The ISA expansion region is divided into eight 16-KB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through MCH and are subtractively decoded to ISA space.

The extended System BIOS region is divided into four 16-KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to HI_A. Typically, this area is used for RAM or ROM.

The system BIOS region is a single 64-KB segment. This segment can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to HI_A. By manipulating the read/write attributes, the MCH can shadow BIOS into the main memory.

Note that the PAM region can be accessed by HI_A or B. All reads or writes from any HI that hits the PAM area is sent to DRAM. If the system is setup so that there are hub interface accesses to the PAM regions, then the PAM region being accessed must be programmed to be both readable and writable by the processor. If the accessed PAM region is programmed for either reads or writes to be forwarded to HI_A and there are hub interface accesses to that PAM, the system may fault.

4.1.3 I/O APIC Memory Space

The I/O APIC spaces are used to communicate with I/O APIC interrupt controllers that may be populated on HI_A through HI_B. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. The address ranges are:

- I/OAPIC0 (HI_A) 0_FEC0_0000h to 0_FEC7_FFFFh
- I/OAPIC1 (HI_B) 0_FEC8_0000h to 0_FEC8_0FFFh

Processor accesses to the IOAPIC0 region are always sent to HI_A. Processor accesses to the IOAPIC1 region are always sent to HI_B and so on.

4.1.4 System Bus Interrupt Memory Space

The System bus interrupt space (0_FEE0_0000h to 0_FEEF_FFFFh) is the address used to deliver interrupts to the System Bus. Any device on HI_A, HI_B may issue a DWord memory write to 0FEEx_xxxxh. The MCH will forward this memory write along with the data to the System Bus as an Interrupt Message Transaction. The MCH terminates the system bus transaction by providing the response and asserting TRDY#. This memory write cycle does not go to DRAM.

The processors may also use this region to send inter-processor interrupts (IPI) from one processor to another.

4.1.5 High SMM Memory Space

The HIGHSMM space (0_FEDA_0000h to 0_FEDB_FFFFh) allows cacheable access to the compatible SMM space by remapping valid SMM accesses between 0_FEDA_0000 and 0_FEDB_FFFFh to accesses between 0_000A_0000h and 0_000B_FFFFh. The accesses are remapped when SMRAM space is enabled; an appropriate access is detected on the system bus, and when ESMRAMC.H_SMRAME allows access to high SMRAM space. SMM memory accesses from any HI port are specially terminated: reads are provided with the value from address 0 while writes are ignored entirely.

4.1.6 AGP Aperture Space (Device 0 and Device 1 BAR)

Processors and AGP devices communicate through a special buffer called the “graphics aperture.” This aperture acts as a window into main DRAM memory and is defined by the APBASE and APSIZE configuration registers of the MCH. Note that the AGP aperture must be above the top of memory and must not intersect with any other address space.

- AGPAPP APBASE to APBASE + APSIZE
- AGPAPP1 APBASE1 to APBASE1 + APSIZE1

Note: Only one of the apertures (Device 0 or Device 1) will be used at any given time. This is determined by which Device’s AGP Enable bit is on. However, both apertures will take space in the memory map unless reclaimed.

4.1.6.1 AGP DRAM Graphics Aperture

The APBASE register follows the standard base address register template defined by the PCI 2.1 specification; however, the size of the range claimed by the APBASE register is programmed via the APSIZE register. System BIOS programs this register before PCI Enumeration to be 4 MB, 8 MB, 16 MB, 32 MB, 64 MB, 128 MB or 256 MB. Once programmed, the APSIZE register forces an appropriate number of the lower bits of the APBASE configuration register to read as 0 which in turns limits the BAR size by hardware design. The default value of APSIZE forces a 256-MB aperture. The aperture address range is aligned to a 4-MB boundary.

4.1.7 Device 2 Memory and Prefetchable Memory

Plug-and-play software configures the HI_B memory window to provide enough memory space for the devices behind this PCI-to-PCI Bridge. Accesses that have addresses that fall within this window are decoded and forwarded to HI_B for completion. The address ranges are:

- M2 MBASE2 to MLIMIT2
- PM2 PMBASE2 to PMLIMIT2

Note that these registers must be programmed with values that place the HI_B memory space window between the value in the TOLM Register and 4 GB. In addition, neither region should overlap with any other fixed or relocatable area of memory.

4.1.8 HI_A Subtractive Decode

All accesses that fall between the value programmed into the TOLM Register and 4 GB (i.e., TOLM and 4 GB) are subtractively decoded and forwarded to HI_A if they do not decode to a space that corresponds to another device.

4.2 I/O Address Space

The MCH does not support the existence of any other I/O devices on the system bus. The MCH generates HI_A–B bus cycles for all processor I/O accesses. The MCH contains two internal registers in the processor I/O space, Configuration Address Register (CONFIG_ADDRESS) and the Configuration Data Register (CONFIG_DATA). These locations are used to implement the configuration space access mechanism and are described in the Chapter 3.

The processor allows 64K+3 bytes to be addressed within the I/O space. The MCH propagates the processor I/O address without any translation to the targeted destination bus. Note that the upper three locations can be accessed only during I/O address wrap-around when signal A16# is asserted on the system bus. A16# is asserted on the system bus whenever a DWord I/O access is made from address 0FFFDh, 0FFFEh, or 0FFFFh. In addition, A16# is asserted when software attempts a two bytes I/O access from address 0FFFFh.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to HI_A–B. All I/O cycles receive a Defer Response. The MCH never posts an I/O write.

The MCH never responds to I/O or configuration cycles initiated on any of the hub interfaces. Hub interface transactions requiring completion are terminated with “master abort” completion packets on the hub interfaces. Hub interface I/O write transactions not requiring completion are dropped.

4.3 SMM Space

4.3.1 System Management Mode (SMM) Memory Range

The E7505 chipset supports the use of main memory as System Management RAM (SMM RAM), which enables the use of System Management Mode. The MCH supports three SMM options:

- Compatible SMRAM (C_SMRAM)
- High Segment (HSEG)
- Top of Memory Segment (TSEG).

System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system operating system so the processor has immediate access to this memory space upon entry to SMM. The MCH provides three SMRAM options:

- Below 1 MB option that supports compatible SMI handlers.
- Above 1 MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional larger write-thru cacheable TSEG area from 128 KB to 1 MB in size above 1 MB that is reserved below the 4 GB in system DRAM memory space. The above 1 MB solutions require changes to compatible SMRAM handler code to properly execute above 1 MB.

4.3.2 TSEG SMM Memory Space

The TSEG SMM space (TOLM – TSEG to TOLM) allows system management software to partition a region of main memory just below the top of low memory (TOLM) that is accessible only by system management software. This region may be 128 KB, 256 KB, 512 KB, or 1 MB in size, depending upon the ESMRAMC.TSEG_SZ field. This space must be below 4 GB, so it is below TOLM and not the top of physical memory, SMM memory is globally enabled by SMRAM.G_SMRAME. Requests may access SMM system memory when either SMM space is open (SMRAM.D_OPEN) or the MCH receives an SMM code request on its system bus. To access the TSEG SMM space, TSEG must be enabled by ESMRAMC.T_EN. When all of these conditions are met, a system bus access to the TSEG space (between TOLM–TSEG and TOLM) is sent to system memory. When the high SMRAM is not enabled or if the TSEG is not enabled, memory requests from all interfaces are forwarded to system memory. When the TSEG SMM space is enabled, and an agent attempts a non-SMM access to TSEG space, then the transaction is specially terminated.

Hub interface originated accesses are not allowed to SMM space.

4.3.3 High SMM Memory Space

The HIGHSMM space (0_FEDA_0000h to 0_FEDB_FFFFh) allows cacheable access to the compatible SMM space by remapping valid SMM accesses between 0_FEDA_0000h and 0_FEDB_FFFFh to accesses between 0_000A_0000h and 0_000B_FFFFh. The accesses are remapped when SMRAM space is enabled; an appropriate access is detected on the system bus, and when ESMRAMC.H_SMRAME allows access to high SMRAM space. SMM memory accesses from any hub interface are specially terminated: reads are provided with the value from address 0 while writes are ignored entirely.

4.3.4 SMM Space Restrictions

When any of the following conditions are violated, the results of SMM accesses are unpredictable and may cause undesirable system behavior:

1. The Compatible SMM space must not be setup as cacheable.
2. Both D_OPEN and D_CLOSE must not be set to 1 at the same time.
3. When TSEG SMM space is enabled, the TSEG space must not be reported to the operating system as available DRAM. This is a BIOS responsibility.

4.3.5 SMM Space Definition

SMM space is defined by its addressed SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High, and TSEG. The Compatible and TSEG SMM space is not remapped and, therefore, the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped, the addressed and DRAM SMM space is a different address range. Note that the High DRAM space is the same as the Compatible Transaction Address space. Table 4-1 describes three unique address ranges:

- Compatible Transaction Address
- High Transaction Address
- TSEG Transaction Address

Table 4-1. SMM Address Range

SMM Space Enabled	Transaction Address Space	DRAM Space
Compatible	A0000h to BFFFFh	A0000h to BFFFFh
High	0FEDA0000h to 0FEDBFFFFh	A0000h to BFFFFh
TSEG	(TOLM–TSEG_SZ) to TOLM	(TOLM–TSEG_SZ) to TOLM

NOTES:
1. High SMM: This is different than in previous chipsets. In previous chipsets the High segment was the 384 KB region from A_0000h to F_FFFFh. However, C_0000h to F_FFFFh was not practically useful so it is deleted in the MCH.
2. TSEG SMM: This is different than in previous chipsets. In previous chipsets the TSEG address space was offset by 256 MB to allow for simpler decoding and the TSEG was remapped to just under the TOLM. In the MCH the TSEG region is not offset by 256 MB and it is not remapped.

4.4 Memory Re-claim Background

The following memory-mapped I/O devices are typically located below 4 GB:

- High BIOS
- HSEG
- XAPIC
- Local APIC
- System Bus Interrupts
- HI_B BAR

In previous generation MCHs, the physical main memory overlapped by the logical address space allocated to these memory-mapped I/O devices was unusable. In workstation systems the memory allocated to memory-mapped I/O devices could easily exceed 1 GB. The result is that a large amount of physical memory would not be usable.

The MCH provides the capability to re-claim the physical memory overlapped by the memory mapped I/O logical address space. The MCH re-maps physical memory from the Top of Low Memory (TOLM) boundary up to the 4 GB boundary (or DRB7 if less than 4 GB) to an equivalent sized logical address range located just above the top of physical memory

4.4.1 Memory Re-mapping

An incoming address (referred to as a logical address) is checked to see if it falls in the memory re-map window. The bottom of the re-map window is defined by the value in the REMAPBASE Register. The top of the re-map window is defined by the value in the REMAPLIMIT Register. An address that falls within this window is remapped to the physical memory starting at the address defined by the TOLM Register.

Functional Description 5

This chapter covers the MCH functional units including: System Bus, AGP, DRAM, SMBus, power management, MCH clocking, MCH system reset and power sequencing.

5.1 System Bus Overview

5.1.1 Source Synchronous Transfers

The MCH is optimized for use with processors based on the Intel® NetBurst™ microarchitecture. The system bus used by the Intel NetBurst microarchitecture processors differs from the P6 micro-architecture processors system bus in the following ways:

- Source synchronous double-pumped address
- Source synchronous quad-pumped data
- System bus interrupt and sideband delivery

The MCH supports two processor configurations at 533 MHz and 400 MHz. The MCH integrates AGTL+ termination resistors on all of the AGTL+ signals. The cache line size is 64 bytes. The address signals are double pumped and a new address can be generated two times for every bus clock. The data is quad pumped and transfers data four times in one bus clock. Working together, the 4x data bus and 2x address bus provide a maximum data bus bandwidth of 4.26 GB/s. The MCH will also run with a System Bus clock of 100 MHz. The MCH supports 36-bit host addresses; this allows the processor to access the entire 16 GB–64 MB (see note) of the MCH's memory address space.

Note: Due to 8-bit register constraints, the maximum usable memory address decode is 15.94 GB (16 GB–64 MB).

5.1.2 IOQ (In Order Queue) Depth

The Scalable Bus supports up to 12 simultaneous outstanding transactions. The MCH also has a 12-deep IOQ; therefore, it does not need to limit the number of simultaneous outstanding transactions by asserting BNR#.

5.1.3 OOQ (Out of Order Queue) Depth

The MCH supports two outstanding deferred transaction on the System Bus. The two transactions must target different I/O interfaces as only one deferred transaction can be outstanding to any single I/O interface at a time.

5.1.4 Dynamic Bus Inversion

The MCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the MCH. The DINV[3:0]# signals indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase (see following table).

DINV[3:0]#	Data Bits
DINV0#	HD[15:0]#
DINV1#	HD[31:16]#
DINV2#	HD[47:32]#
DINV3#	HD[63:48]#

When the processor or the MCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus, the corresponding DINV# signal will be asserted and the data will be inverted prior to being driven on the bus. When the processor or the MCH receives data, it monitors DINV[3:0]# to determine if the corresponding data segment should be inverted.

Dynamic Bus Inversion (DBI) is a technique used to guarantee that a maximum of half the data signal values are active (1 internally or 0 on the System Bus). This mechanism groups the data bus into groups of 16 signals. In every group the number of active signals is counted, if more than eight active signals are present, the group's signals are inverted and the inversion indication (DINV internally, DINV# on the System Bus) is activated; otherwise, the group is not inverted.

DBI is used to minimize signal switching within a group of 16 data signals and minimize on-die terminations' power consumption. DBI specification requires that, for most of the time, there will be no more than 8 active data signals in a group of 16. It requires that there will **never** be more than 9 active data signals in a group of 16.

5.1.5 System Bus Interrupt

Interrupt-related messages are encoded on the system bus as "Interrupt Message Transactions." In the MCH platform system bus interrupts may originate from the processor on the system bus (IPIs- inter-processor interrupts), from a downstream device on the hub interface, or AGP. In the later case the MCH drives the "Interrupt Message Transaction" onto the system bus.

The ICH4 contains an IOxAPIC. Interrupts are generated to a processor in the form of upstream hub interface memory writes. The *PCI Local Bus Specification, Revision 2.2* defines MSIs (Message Signaled Interrupts) that are also in the form of memory writes. A PCI 2.2 device may generate an interrupt as an MSI cycle on its PCI bus instead of asserting a hardware signal to the IOxAPIC. The MSI may be directed to the IOxAPIC which in turn generates an interrupt as an upstream hub interface memory write. Alternatively, the MSI may be directed directly to the system bus. The target of an MSI is dependent on the address of the interrupt memory write. The MCH forwards inbound hub interface memory writes to address 0FEEx_xxxxh to the system bus as "Interrupt Message Transactions."

The MCH supports re-directing lowest priority delivery mode interrupts to the processor which is executing the lowest priority task thread. The MCH re-directs interrupts based on the task priority status of each processor thread. The task priority of each processor thread is periodically downloaded to the MCH via the xTPR (Task Priority Register) special transaction. The MCH re-directs hub interface and PCI originated interrupts as well as IPIs.

The MCH also broadcasts EOI cycles generated by a processor downstream to the hub interface.

5.2 Hub Interface_A (HI_A)

The MCH's 8-bit HI_A is used to connect to the ICH4. HI_A supports parallel termination. The MCH uses Hub Interface 1.5 electricals on HI_A. HI_A also supports 64 bit upstream addressing via the hub interface extended address mechanism.

5.3 Hub Interface_B (HI_B)

HI_B supports Hub Interface 2.0 only. The following assumptions apply to the HI_B:

- Supports HI 2.0 devices only
- Does not support 8-bit devices
- Does not operate in 1x mode
- Supports Hub Interface 2.0 Enhanced Parity (ECC) only
- Parallel termination only
- Does not support upstream writes or special cycles that require completion. The only upstream cycle that can require a completion is a read.
- HI_B is designed to connect to the P64H2 component.

5.4 AGP 8x Interface

The MCH supports AGP 8x with backwards compatibility to AGP 4x. The electrical signal levels supported by the MCH for the AGP 8x interface are 0.8 V levels for 8x, 4x (AGP 3.0) transfers. The MCH can also operate in 4x, 2x, and 1x (AGP 2.0) modes: these modes are only at 1.5 V signal levels.

Note: The MCH does **not** support 3.3 V signal levels.

The MCH has a 32-deep AGP request queue that is used for Asynchronous modes. The MCH integrates two fully-associative 10 entry Translation Look-aside Buffers; one for reads and one for writes.

5.4.1 Selecting between AGP 3.0 and AGP 2.0 Signaling Modes

The MCH supports both AGP 3.0 and AGP 2.0 specifications allowing a “Universal AGP 8x motherboard” implementation. The AGP 3.0 or AGP 2.0 signaling mode setting is determined by the type of graphic card installed in the system. The mode determination is decided during RESET by a hardware mechanism (see Section 5.4.9).

Note: The configured AGP mode determines the electrical signal levels and cannot be dynamically changed once the system power ups.

5.4.2 Dynamic Bus Inversion (DBI)

To mitigate the effects of simultaneous switching outputs, AGP 3.0 adopts a technique called Dynamic Bus Inversion (DBI) to limit the maximum number of simultaneous transitions on source synchronous data transfers. DBI impacts only GAD[31:0] and is used during source synchronous and common clock transfers. Two new signals are defined to support DBI. DBI_LO and DBI_HI are used to implement DBI on GAD[15:0] and GAD[31:16], respectively.

When the number of bit transitions in GAD[15:0] (or GAD[31:16]) from one source synchronous period to the next exceeds eight, the entire field is inverted by the transmitter to limit the maximum transitions to eight. For example, if GAD[15:0] changes from FF10h in source synchronous cycle A to 0000h in source synchronous cycle B, the DBI mechanism is triggered in cycle B; this inverts GAD[15:0] to produce FFFFh. In this example, the number of transitions without DBI is nine; the number with DBI is seven. To signal the receiver that GAD[15:0] are inverted in cycle B, DBI_LO is asserted high. The same mechanism is used on GAD[31:16]. DBI_HI is used to indicate the inversion. The receiver samples DBI_HI and DBI_LO to determine whether to invert GAD[31:0] before using it.

A similar technique applies to common clock and frame-based (PCI) address and data transfers. In these instances, DBI applies to transitions from one common clock period to the next.

DBI is supported when operating in 8x speed and in AGP 3.0 signaling mode. During 4x speed transfers or frame-based PCI transfers in the same signaling mode, DBI is **not** supported in transmit but is supported in receive. DBI is not supported when in AGP 2.0 or AGP 1.0 signaling modes.

5.4.3 AGP 3.0 and AGP 2.0 Signaling Mode Differences

Table 5-1. Key Differences Between AGP 3.0 and AGP 2.0 Signaling Modes

Parameter	AGP 3.0 Signaling Mode	AGP 2.0 Signaling Mode	Comments
Data Rate	8x or 4x	4x, 2x, or 1x	
Electricals	0.8 V swing, parallel termination	1.5 V swing serial termination	
Signal Polarity	Most controls signals active high	Most control signals active low	This change was necessary to eliminate current flow in the idle stare. Parallel termination has a large current flow for a high level.
Hi/ Low priority commands	Only low priority (renamed Async)	High and low priority commands supported	
Strobe Protocol	Strobe First-Strobe Second Protocol	Strobe-Strobe# protocol	
Long Transactions	Removed	Supported	
PIPE# Support	No	Yes	SBA required for AGP 3.0.
Calibration Cycle	Required	No	New to AGP 3.0.
Dynamic Bus Inversion	8x Yes 4x receive only	No	New to AGP 3.0.
Coherency	Required for AGP accesses outside of the aperture, and for FRAME-based accesses	Required only for FRAME based accesses	

5.4.4 AGP 3.0 Downshift (4x data rate) Mode

AGP 3.0 supports both 8x and 4x data rates. By supporting the 4x data rate, a system has the capability of supporting a legacy AGP 4x graphic card (1.5 V signal levels). In addition, there may be instances where system-related deficiencies may cause an 8x graphic card to downshift to the 4x data rate. All of the AGP 3.0 protocols are used during 4x data rate transfers.

Table 5-2. AGP 3.0 Downshift Mode Parameters

Parameter	AGP3.0 Signaling, 4x Data Rate	AGP3.0 Signaling, 8x Data Rate	AGP2.0 Signaling, all Data Rates
Data Rate	4x	8x	1x, 2x, 4x
VREF Level	0.35 V	0.35 V	0.75 V
Signaling	0.8 V	0.8 V	1.5 V
Polarity of GREQ, GGNT, GDEVSEL, GFRAME, GIRDT, GTRDY, GSTOP, RBF, WBF	Active High	Active High	Active Low
Polarity of SBA	inverted (000=idle)	inverted (000=idle)	normal (111=idle)
GC/BEx Polarity	GC#/BEx	GC#/BEx	GC/BEx#
Strobe Definition	Strobe first / Strobe second	Strobe first / Strobe second	Strobe/ Strobe#
DBI Used	In receive only	Yes	No
PIPE# Allowed	No	No	Yes
Commands Supported	AGP 3.0	AGP 3.0	AGP 2.0
Calibration Cycles Included	Yes	Yes	No

5.4.5 AGP Target Operations

As an initiator, the MCH does not initiate cycles using AGP enhanced protocols. The MCH supports AGP target interface to main memory only. The MCH supports interleaved AGP and PCI transactions.

Table 5-3. AGP 3.0 and AGP 2.0 Support Command Types

GC/BE[3:0]# (GC#/BE[3:0]) Encoding	AGP 3.0 Command	AGP 2.0 Command
0000	Read (Asynchronous)	Read (Low Priority)
0001	Reserved	Read (High Priority)
0010	Reserved	Reserved
0011	Reserved	Reserved
0100	Write (Asynchronous)	Write (Low Priority)
0101	Reserved	Write (High Priority)
0110	Reserved	Reserved
0111	Reserved	Reserved
1000	Reserved	Long Read (Low Priority)
1001	Reserved	Long Read (High Priority)
1010	Flush	Flush (Low Priority)
1011	Reserved	Reserved
1100	Fence (for reads & writes)	Fence (Low Priority)
1101	Reserved (was DAC cycle)	Reserved (was DAC cycle)
1110	Reserved	Reserved
1111	Reserved	Reserved

5.4.6 Coherency

Coherency with the processor caches depends on the mode of operation and the cycle type. The *AGP Specification 2.0* requires only that PCI semantic transactions are coherent. The *AGP Specification 3.0* requires that AGP semantic asynchronous transactions outside of the aperture be coherent as well as PCI semantic transactions. All other transactions are non-coherent in the MCH to improve performance. Table 5-4 summarizes the transaction coherency.

Table 5-4. AGP Summary of Transaction Coherency

Mode	Async	Access type	Aperture	Coherent	Comments
AGP 8x	Async	AGP	Inside	No	
AGP 8x	Async	AGP	Outside	Yes	
AGP4x/2x/1x	Hi/Lo Prio	AGP	Either	No	
All	N/A	PCI	Either	Yes	

5.4.7 AGP Aperture and GART

The MCH contains the AGP aperture and GART capabilities to allow address translation of AGP accesses. This capability is very similar to previous chipsets.

The AGP aperture may be anywhere from 4 MB to 256 MB in size in binary increments The default is 256 MB. It is placed above the top of low memory by the PCI plug-and-play software. The GART address is always naturally aligned to its size, as is required by PCI plug-and-play.

The MCH supports 4-K page sizes. Optional larger sizes of the *AGP Specification 3.0* are not supported.

A memory location must not be accessed through the aperture by one stream or master, and directly via its memory address by another stream or master. Coherency issues may result. Address 0000_0000h must not be allocated to AGP memory.

5.4.8 Peer-to-Peer Traffic

Peer writes from any hub interface to AGP are permitted. These will appear as PCI semantic write cycles to the AGP device and may appear as fast writes. Reads from any hub interface to AGP are **not** permitted. Neither reads nor writes from a PCI master are permitted to a hub interface.

5.4.9 AGP Electrical Characteristics

The MCH supports AGP 3.0 and AGP 2.0 signaling. The selected mode is determined by the voltage applied to the PREF_AGP[1:0] pins. It is set during RESET and can not change dynamically.

AGP 3.0 signaling uses 0.8 V levels. It is selected by PREF_AGP[1:0] being at 0.35 V. The VDDQ I/O supply voltage is nominally 1.5 V, allowing it to be common to AGP 3.0 or AGP 2.0 signaling. AGP 3.0 signaling uses a 50 Ω termination to ground on each end when not driving the interface, so the idle state of the signals is low. Most command and control signals are inverted in AGP 3.0 signaling compared to AGP 2.0 signaling; the control signal inversions minimizes static current flow during idle bus conditions.

AGP 2.0 signaling uses the full 1.5 V rail-to-rail swing. It is selected by PREF_AGP[1:0] being at 0.75 V during RESET.

Table 5-5. Data Rates and Signaling Levels Supported by the MCH

Data Rate	Signaling Level		
	AGP 3.0	1.5 V	3.3 V
PCI-66	Yes*	Yes	No
1x AGP	No	Yes	No
2x AGP	No	Yes	No
4x AGP	Yes	Yes	No
8x AGP	Yes	No	No

The AGP connector has two pins to determine the signaling mode. This flexibility allows both the motherboards and graphics cards to support both modes.

GC_DET# is grounded by the graphics card to indicate that it is an AGP 3.0-capable graphics controller and is floated by an AGP 2.0 graphics controller. An AGP 2.0-only motherboard ignores this signal. An AGP 3.0-capable motherboard uses this signal to select between a 0.35 V (AGP 3.0) or 0.75 V (AGP 2.0) VREF. This VREF is sent back to the graphics controller card. The graphic controller card can use the VREF level or the MB_DET# signal to determine the electrical mode.

MB_DET# is grounded by the motherboard to indicate that it is an AGP 3.0 capable motherboard, and is floated by an AGP 2.0 motherboard. An AGP 2.0 only graphics controller ignores this signal. An AGP 3.0 capable graphics controller uses the MB_DET# to select between 0.35 V (AGP 3.0) or 0.75 V (AGP 2.0) VREF. This VREF signal level is sent back to the motherboard. The motherboard board may use the VREF level or the GC_DET# signal to determine the electrical mode. An AGP 2.0 graphics card supplies 0.75 V on AGPVREFGC at all times. A universal card supplies 0.35 V or 0.75 V as selected by the MB_DET# signal.

An AGP 2.0 motherboard supplies 0.75 V AGPVREFGC at all times. A universal motherboard supplies 0.35 V or 0.75 V, as selected by the GC_DET# signal.

The above description describes the typical case. Actual usage of the GC_DET# signal and AGPVREFGC voltage by the motherboard is implementation dependant. Likewise, the actual usage of the MB_DET# signal and AGPVREFGC voltage by the graphics controller is implementation dependant. Optionally, the motherboard could use its own VREF which would be switched by the GC_DET#.

The motherboard design is aware of its own capabilities and determines the graphics controller's capabilities from GC_DET#, as well as receiving the proper VREF voltage. Likewise, the graphics controller design is also aware of its own capabilities and determines the motherboard's capabilities from MB_DET#, as well as receiving the proper VREF voltage.

5.4.10 AGP 3.0 Protocol

The MCH supports the AGP 8x protocol as specified in the *AGP Specification 3.0*. In AGP 8x mode, the PIPE# signal cannot be used to enqueue transactions. The AGP 8x data rate provides a theoretical maximum bandwidth of 2.13 GB/s. The actual bandwidth is determined by the memory hit rate and other traffic to the memory controller.

5.4.11 AGP 2.0 Protocol

In addition to the 1x and 2x AGP protocols, the MCH supports 4x AGP read/write data transfers and 4x sideband address generation. The 4x operation is compliant with the AGP 4x protocols as described in the *AGP Specification 3.0*.

5.4.12 Fast Writes

The Fast Write (FW) transaction is from the core logic to the AGP master acting as a PCI target. This type of access is required to pass data/control directly to the AGP master instead of placing the data into main memory and then having the AGP master read the data. For 1x transactions, the protocol follows the PCI bus specification. However, for higher speed transactions (2x, 4x, or 8x), FW transactions follow a combination for PCI and AGP bus protocols for data movement.

5.4.13 AGP Connector

The MCH only supports the AGP 1.5 V connector that permits a 1.5 V AGP 2.0 or AGP 3.0 graphics card to be supported by the system. The MCH is a "Universal AGP 8x" device supporting either 1.5 V or 0.8 V signaling. A keep-out keying mechanism in the AGP 1.5 V connector prevents a 3.3 V card from inadvertently being installed.

5.4.14 PCI Semantic Transactions on AGP

The MCH accepts and generates PCI semantic transactions on the AGP bus. The MCH guarantees that PCI semantic accesses to DRAM are kept coherent with the processor caches by generating snoops to the processor bus.

5.5 Main Memory Interface

The memory interface supports a dual channel DDR system memory with registered or unbuffered SDRAM DIMMs. The MCH only supports DDR-SDRAM type of memory. The MCH does **not** support SDR SDRAM (PC-100/133) type of memory. Table 5-6 defines the some of the terms used in this section

Table 5-6. DRAM Terminology

Term	Definition
DDR	Double Data Rate. This term describes the type of DRAMs that transfer two data items per clock on each pin. This is the only type of DRAM supported by the MCH.
DIMM	Dual Inline Memory Module. A PC board containing 4 to 36 DRAM chips that the end user can install into the DIMM sockets on the motherboard.
Single-Sided DIMM	Single-Sided DIMM usually describes a DIMM that contains one DRAM row. Usually, one row fits on a single side of the DIMM allowing the backside to be empty; when using x4 DRAM chips, both sides are required for a single row. This terminology is not used within this document.
Double-Sided DIMM	Double-Sided DIMM usually describes a DIMM that contains two DRAM rows. Generally, a Double-Sided DIMM contains two rows, with the exception noted above. This terminology is not used within this document.
Stacked DIMM	Stacked DIMM describes a dual row DIMM using x4 DRAM parts. The x4 parts require 18 chips for each row or 36 chips for two rows. A DIMM generally only has room for 18 DRAM chips; thus, the two DRAM rows are stacked on top of each other with specially pined out DRAMs such that the CS and CKE pins for the bottom row are on different pins than the CS and CKE pins for the top row. These DIMMs are used in workstations to maximize DRAM capacity. **They are only available on registered DIMMs.**
Registered DIMM	In a registered DIMM the address and control signals are buffered through a flip-flop (register) and the clock is buffered by a PLL circuit. A registered DIMM presents only one load on the clock, address, and command lines, but delays the address and command by one clock. There is no register on the data pins. These DIMMs are often used on workstations to achieve a higher memory capacity. They can carry a significant cost premium.
Unbuffered DIMM	In an unbuffered DIMM the clocks, address, and control signals of each DRAM chip are driven by the DRAM controller with no buffer or register. These are the standard DIMMs used on most desktop systems and many low end workstation and servers.
Buffered DIMM (not used)	There are no DIMMs with just a buffer that is not a flip-flop. This term should not be used.
Unregistered DIMM (not used)	The term “Unbuffered” should be used instead of Unregistered.
SPD	Serial Presence Detect. This is a serial EE ROM on all DIMMs that contain data such as the number of rows, DRAM type (technology, chip width, page size, timing parameters, etc.), manufacturer, and other information. This information is read by the BIOS via the SMBus controller on the ICH to determine what memory is installed in the system.
Row	A group of DRAM chips that fill out the data bus width of the system and are accessed in parallel by each DRAM command.Tthe MCH data width is 144 bits. A DIMM pair may contain either 1 or 2 rows.
Bank	DRAM chips are divided into multiple banks internally. Commodity parts are 4 bank, which is the only type the MCH supports. Each bank acts somewhat like a separate DRAM; opening and closing pages independently and allowing different pages to be open in each. Most commands to a DRAM target a specific bank; however, some commands (i.e., Precharge All) are targeted at all banks. Multiple banks allows higher performance by interleaving the banks and reducing page miss cycles.

Table 5-6. DRAM Terminology (Continued)

Term	Definition
Page	A page is a section of a DRAM bank that is opened by an activate command. Once opened, multiple locations (columns) of a page can be read or written without requiring a precharge and activate command.
Row Address	The row address is presented to the DRAMs during an Activate command and indicates which page to open within the specified bank (the bank number is also presented).
Column Address	The column address selects one DRAM location (or the starting location of a burst) from within the open page on a read or write command.
Channel	In the MCH, a DRAM Channel is the set of signals that connect to one set of DRAM DIMMs. The MCH has two DRAM channels, (a pair of DIMMs added at a time, one on each channel).

5.5.1 Frequency and Bandwidth

In the MCH, the same core clock frequency is used for the processor system bus and the memory interface. The system bus and memory interface frequencies must be operating synchronously (see Table 5-7).

Table 5-7. Supported System Bus and Memory Interface Configurations

System Bus Clock	System Bus Transfer/s	System Bus BW	DRAM Clock	DRAM Transfer/s	DDR BW
133 MHz	533 MT/s	4.27 GB/s	133 MHz	266 MT/s	4.27 GB/s
100 MHz	400 MT/s	3.2 GB/s	100 MHz	200 MT/s	3.2 GB/s

NOTE: A 266 MT/s DRAM can be used with a processor supporting a 400 MHz system bus, although the memory interface will be operating at 100 MHz and not 133 MHz.

5.5.2 Memory Operation

The MCH contains a dual-channel DDR interface, with each channel having 64 data bits and 8 ECC bits. The memory interface channels operate in “lock-step” with each other. The data is a double QWord interleaved between the channels with the low DQWord on channel A and the high DQWord on channel B. A burst of four data items, that takes two clocks, is required for one cache line (64 bytes). A 256-bit interface transfers the data at the core clock frequency internally, matching the memory bandwidth.

The memory must be populated in identical DIMM configurations (i.e., Slot 0 of channel A must contain the same configuration DIMM as Slot 0 of channel B). The configuration consists of the same number of rows (1 or 2), the same technology part (128 Mb, 256 Mb, 512 Mb, or 1 Gb), the same DRAM chip width (x4, x8, or 16), and the same speed.

Note: When the MCH is configured as a **Registered DIMM** platform only, the user must populate the memory modules in the following manner:

- Channel A and Channel B must contain the same memory configuration as described above.
- First populate the furthest DIMM slot (within the channel) respective to the MCH.

5.5.3 DRAM Technologies and Types Supported

- 128-Mb, 256-Mb, 512-Mb, and 1-Gb technology DRAMs
- x4, x8 registered
- x8, x16 unbuffered (Double-sided x16 is not supported)
- 4 bank devices only
- Page sizes supported: 4 KB, 8 KB, 16 KB, 32 KB, and 64 KB. They are selectable per row pair.

5.5.4 Memory Capacity

The maximum memory capacity supported by the MCH is 16 GB–64 MB (see note below). This can be achieved with the following configurations:

Note: Due to 8-bit register constraints, the maximum usable memory address decode is 15.94 GB (16 GB–64 MB).

Table 5-8. Maximum Supported Memory Configurations

DIMM Type	Frequency	Number of DIMMs per Channel	Address/CMD Loading	CS Loading	CKE Loading	Data Loading
Unbuffered	100 and 133	2 DIMMs double row	36 loads	8	8	4 Loads
Registered	100 and 133	3 DIMM double row	3 loads	1	3	6 loads

NOTES:
1. “Double row” implies that single or double row DIMMs are supported. “Single row” implies that only single row DIMMs are supported.
2. Loads listed above are “maximums.”
3. “Loading” does not include the MCH load.
4. The supported configuration limits are based on electricals. Logically the MCH supports three double-sided DIMMs per channel in all configurations

Note: Contact your Intel representative to verify the memory configurations validated with the MCH.

Table 5-9 shows memory per DIMM at each DRAM density:

Table 5-9. Memory per DIMM at Each DRAM Density

Parts	128 Mb	256 Mb	512 Mb	1 Gb	Comments
x16, single row	64 MB	128 MB	256 MB	512 MB	Available in unbuffered only. **NOTE:** Double-sided x16 is not supported
x8, single row	128 MB	256 MB	512 MB	1 GB	Unbuffered and registered
x8, double row	256 MB	512 MB	1 GB	2 GB	Unbuffered and registered
x4, single row	256 MB	512 MB	1 GB	2 GB	Available in registered only
x4, double row	512 MB	1 GB	2 GB	4 GB	Available in registered only (stacked chips)

5.5.5 Refresh

The MCH contains a multi-level refresh operation to reduce the refresh performance impact. Refresh events are queued and performed opportunistically, when the DRAM pipe is idle. Standard Auto Refresh operation is performed in a staggered manner for only populated pairs of rows. Self-refresh operation is supported as part of transition into or out of Suspend-To-RAM (STR).

5.5.6 Intel® x4 SDDC Technology ECC

The MCH supports Intel® x4 Single Device Data Correction (x4 SDDC) technology ECC. The ECC code spans 144 bits of data. ECC may be disabled by the System BIOS. No performance gain is achieved.

The x4 SDDC technology ECC performs the following:

- Corrects any number of errors contained in a 4-bit naturally aligned nibble.
- Detects all errors contained entirely with two 4-bit naturally aligned nibbles.
- Corrects errors caused by a complete failure of a x4 SDRAM part.

5.5.7 Memory Thermal Management

The MCH provides a thermal management method that selectively reduces reads and writes to DRAM when the access rate crosses the allowed thermal threshold. Read and write thermal management operate independently, and have their own 64-bit register to control operation. Memory reads typically causes power dissipation in the DRAM chips, while memory writes typically cause power dissipation in the MCH.

Determining When to Thermal Manage

Thermal management may be enabled by one of two mechanisms:

- Software forcing throttling via the SRT (SWT) bit.
- Counter Mechanism.

5.5.8 Clock Generation

The MCH drives the clocks to the DIMMs. Unbuffered DIMMs require 3 clock pair per DIMM while Registered DIMMs require one clock pair per DIMM. A 2-DIMM slot unbuffered motherboard requires 6 clock pair (per channel), while the 3-DIMM slot Registered motherboard requires 3 clock pair (per channel). Table 5-10 shows the clock connections.

Table 5-10. Clock Connections

Signal	2 DIMM MB	3 DIMM MB
CMDCLK7, CMDCLK7#	DIMM1 CK2, CK2#	No connect
CMDCLK6, CMDCLK6# / CS[5:4]#	DIMM0 CK2, CK2#	DIMM 2 CS[1:0]
CMDCLK5, CMDCLK5#	DIMM1 CK1, CK1#	No connect
CMDCLK4, CMDCLK4#	DIMM0 CK1, CK1#	No connect
CMDCLK3, CMDCLK3#	No connect	No connect
CMDCLK2, CMDCLK2#	No connect	DIMM2 CK0
CMDCLK1, CMDCLK1#	DIMM1 CK0, CK0#	DIMM1 CK0
CMDCLK0, CMDCLK0#	DIMM0 CK0, CK0#	DIMM0 CK0

5.6 System Manageability Bus 2.0

The MCH supports the following features:

- Address Resolution Protocol (ARP)
- Alert Standard Forum (ASF)
- Packet Error Checking (PEC)

SMBus Signaling

The System Management Bus (SMBus) is a two-wire interface where the system can communicate with other devices. A system using SMBus passes messages to and from devices. With SMBus, a device can provide manufacturer information, model/part number information, save its state for a suspend event, report different types of errors, accept control parameters, and return its status. Refer to the *SMBus Specification, Revision 2.0* for additional information.

5.7 Power Management

Power Management Support Overview

The MCH supports the following Processor/System States:

- Processor states: C0, C1
- ACPI System States: S0, S1, S3–S5

Specifications Supported

- ACPI Specification, Revision 1.0b
- ACPI Specification, Revision 2.0
- PCI Power Management Specification, Revision 1.0
- PC 2001 Specification

5.7.1 Processor States

C0 (Full On)

This is the only state that runs software. All clocks are running, STPCLK# is deasserted and the processor core is active. The processor can service snoops and maintain cache coherency in this state.

C1 (Auto-Halt)

The first level of power reduction occurs when the processor executes an Auto-Halt instruction. This stops the execution of the instruction stream and greatly reduces the processors power consumption. The processor can service snoops and maintain cache coherency in this state. The MCH is completely oblivious to this processor state.

C2

C2 is not supported by the MCH.

C3

C3 is not supported by the MCH.

5.7.2 Suspend States

S0 (Awake)

In this state all power planes are active. All of the ACPI software “C” states are embedded in this state.

S1 (Powered-on-Suspend)

The MCH implements a desktop S1 that simply puts the processor in stop-grant mode which is functionally identical as C2.

S3 (Suspend-to-RAM)

The final level of power savings for the MCH is achievable when the host clock, memory group, and I/O clock group clocks are shutdown and the MCH is powered down. This occurs when the system transitions to the S3 State. The MCH places all of the DRAM components into the Power-down State so that they will perform self-refresh.

S4 (Suspend-to-Disk), S5 (Soft-Off) State

The MCH does not distinguish between Suspend-to-Ram (S3), Suspend-to-Disk (S4), and Soft-Off (S5) states. From the MCH perspective, entry and exit to S4 or S5 states, is the same as entry and exit to S3 state.

5.7.3 Clock Control

The clocks in the platform fall into three categories:

- The first category consists of those clocks that turn on and off during normal operation (e.g., a serial port clock).
- The second category consists of clocks that never turn off. Only the 32.768 kHz RTC clock falls into this category.
- The third category consists of those clocks that must be active in normal operation but are actively controlled by the platform to manage power.

The platform separates the third category into two groups: the host clock group and the I/O clock group. All of the clocks in a group are controlled as a set (i.e., turning on and off together).

ACPI Clock Summary

The mapping between the ACPI states and the states of the system clocks is shown in Table 5-11. Note that the ten ACPI states only map to four distinct states of the system clocks. In both the G0/S0/C0 and G0/S0/C1 states all system clocks are on. Some clocks internal to the processor may be shut down in G0/S0/C1 as a result of the processor executing an auto-halt.

In G1/S3 through G2/S5 states all system clocks except for the RTC clock have been shutdown. The RTC clock is used to detect wake events when the system is in any of these states. The G3 state is hard off with the power supply mechanically isolated.

Table 5-11. ACPI State to Clock State Mapping

G State	S State	C State	Processor State	Processor Clock	MCH Clock	DRAM Clock	PCI Clock
G0	S0	C0	Full On	On	On	On	On
G0	S0	C1	Auto-Halt	On	On	On	On
G1	S1	N/A	C2	ON	ON	ON	ON
G1	S3	N/A	N/A	Off	Off	Off	Off
G1	S4	N/A	N/A	Off	Off	Off	Off
G2	S5	N/A	N/A	Off	Off	Off	Off
G3	N/A	N/A	N/A	Off	Off	Off	Off

The ACPI C-states refer to processor states. Since the MCH is closely coupled to the processor, the MCH's various power states defined in this document are also called C-states.

5.8 Clocking

The MCH is supported by the CK408 compliant clock synthesizer. For details, refer to the *Intel® Xeon™ Processor and Intel® E7505 Chipset Platform Design Guide* and the *CK408 Clock Synthesizer/Driver Specification*.

5.9 System Reset and Power Sequencing

For details, refer to the *Intel® Xeon™ Processor and Intel® E7505 Chipset Platform Design Guide*.

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Electrical Characteristics 6

This chapter provides the absolute maximum ratings, thermal characteristics, and DC characteristics for the MCH[1].

NOTE: 1.) VCC is set at 1.2 V or 1.3V depending on the part. Please refer to the E7505 Chipset Memory Controller Hub Specification Update for more information

6.1 Absolute Maximum Ratings

Table 6-1 lists the MCH's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. Functional operating parameters are listed in the DC tables.

Note: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "operating conditions" is not recommended and extended exposure beyond "operating conditions" may affect reliability.

Table 6-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
Tstorage	Storage Temperature	–55	150	°C	
$VCC_{MCH(1.2V)}$	1.2 V Supply Voltage with respect to VSS	–0.38	2.1	V	
$VCC_{MCH(1.3V)}$	1.3 V Supply Voltage with respect to VSS	–0.38	2.1	V	
VTT_{AGTL+}	Host AGTL+ Termination Voltage	–0.38	2.1	V	
VCC_{DDR}	DDR I/O Buffer Supply Voltage	–0.38	3.0	V	

NOTE:
1. Based on a No Heatsink condition.

6.2 Power Characteristics

Table 6-2. DC Characteristics Functional Operating Range

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$I_{CC(1.2V)}$	1.2 V MCH Core and HI			3.5	A	
$I_{CC(1.3V)}$	1.3 V MCH Core and HI			4.0	A	

Table 6-2. DC Characteristics Functional Operating Range

Iagp	1.5 V AGP			0.6	A	
I_{VTT}	1.525 V AGTL+			2.1	A	
I_{dd_DDR}	2.5 V Vdd DDR (2 channel)			6.8	A	

6.3 I/O Interface Signal Groupings

The signal description includes the type of buffer used for the particular signal:

- AGTL+ Open Drain AGTL+ interface signal. The MCH integrates AGTL+ termination resistors.
- CMOS 1.2 V CMOS buffers.
- SSTL-2 DDR Signaling Interface
- HI-2 Hub Interface buffer type
- AGP AGP Interface Buffer Type

Table 6-3. Signal Groups System Bus Interface

Signal Group	Signal Type	Signals	Notes
(a)	AGTL+ I/O	AP [1:0]#, ADS#, BNR#, DBSY#, DEP [3:0]#, DRDY#, HA [35:3]#, HADSTB [1:0] #, HD [63:0], HDSTBP [3:0]#, HDSTBN [3:0]#, HIT#, HITM#, HREQ [4:0]#, BREQ0#, DINV [3;0]#, HXRCOMP, HYRCOMP	
(b)	AGTL+ Output	BPRI#, CPURST#, DEFER#, HTRDY#, RS [2:0]#, RSP#	
(c)	AGTL+ Input	HLOCK#, XERR#, BINIT#	
(d)	Analog Input	HDVREF [3:0], HAVREF [1:0], CCVREF, HXSWNG, HYSWNG	
(e)	CLK Inputs	HCLKINN, HCLKINP	
(f)	AGTL+ Termination Voltage	VTT	

Table 6-4. Signal Groups DDR Interface

Signal Group	Signal Type	Signals	Notes
(g)	SSTL-2 I/O	DQ_x [63:0], CB_x [7:0], DQS_x [17:0], DRCOMP_x, ODTCOMP	1
(h)	SSTL-2 Output	CMDCLK_x[6:0], CMDCLK_x[6:0]#, CS_x[5:0], CS_x[5:0]#, MA_x[13:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x#, CKE_x[3:0], RCVENOUT_x#	1
(i)	SSTL-2 Input	DDRSTRAP	1
(j)	Analog Input	DVREF_x, DRCOMPVREF_x	1

NOTE: 1. x = A, B DDR channel

Table 6-5. Signal Groups AGP Interface

Signal Group	Signal Type	Signals	Notes
(k)	AGP I/O	GDEVSEL# (2.0), GDEVSEL (3.0), GAD[31:0], GC/BE[3:0]# (2.0), GC/BE[3:0] (3.0), GPAR, DBI_LO (3.0 only), AD_STB0 (2.0), AD_STBF0 (3.0), AD_STB0# (2.0), AD_STBS0 (3.0), AD_STB1 (2.0), AD_STBF1 (3.0), AD_STB1# (2.0), AD_STBS1 (3.0), PIPE# (2.0), DBI_HI (3.0), GIRDY# (2.0), GIRDY (3.0), GTRDY# (2.0), GTRDY (3.0), GSTOP# (2.0), GSTOP(3.0), PRCOMP_AGPx, GFRAME# (2.0), GFRAME (3.0)	
(l)	AGP Output	GGNT#(2.0), GGNT(3.0), ST[2:0]	
(m)	AGP Input	GREQ# (2.0), GREQ (3.0), SBA[7:0] (2.0), SBA[7:0]# (3.0), SB_STB (2.0), SB_STBF (3.0), SB_STB# (2.0), SB_STBS (3.0), WBF# (2.0), WBF (3.0), SERR# (2.0), SERR(3.0), RBF# (2.0), RBF (3.0)	
(n)	Analog Input	PREF_AGPx, PSWNG_AGPx	

Table 6-6. Signal Groups Hub Interface 2.0 (HI_B)

Signal Group	Signal Type	Signals	Notes
(o)	HI-2 I/O	HI_B[21:20,18:0], PSTRB_B[1:0], PSTRB_B[1:0]#, PRCOMP_B	1
(p)	Input Clock	CLK66	
(q)	Analog Input	PREF_B, PSWNG_B	1

NOTE: CLK66 is being shared on HI_A and HI_B

Table 6-7. Signal Groups Hub Interface 1.5 (HI_A)

Signal Group	Signal Type	Signals	Notes
(r)	HI-2 I/O	HI_A[11:10,7:0], PSTRBF_0, PSTRBS_0, PRCOMP_A	
(s)	HI-2 I/O	HI_A8	
(t)	HI-2 I/O	HI_A9	
(u)	Input Clock	CLK66	1
(v)	Analog Input	PVREF_A, PSWNG_A	

NOTE: 1. Clk 66 is being shared on HI_A and HI_B

Table 6-8. Signal Groups Reset and Miscellaneous

Signal Group	Signal Type	Signals	Notes
(x)	Miscellaneous CMOS Input	RSTIN#, PWRGOOD, XORMODE#	

6.4 DC Characteristics

This section provides DC Characteristics at VCC1_2 = 1.2 V ± 5%

and at VCC1_3 = 1.3 V ± 5%

Table 6-9. Operating Condition Supply Voltage

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
VTT	(f)	Host AGTL+ Termination Voltage	1.15		1.525	V	
VCC_{DDR}		DDR Buffer Voltage	2.375	2.5	2.625	V	
VCC_{MCH}		MCH Core Voltage	1.14	1.2	1.26	V	
VCC_{AGP}		AGP Voltage	1.425	1.5	1.575	V	
GTLREF		Host AGTL+ Reference Voltage		0.63 x VCC ±2%			

Table 6-10. System Bus Interface DC Characteristics

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
V_{IL_H}	(a), (c)	Host AGTL+ Input Low Voltage			(0.63 x VTT) – 0.1GTLREF	V	
V_{IH_H}	(a), (c)	Host AGTL+ Input High Voltage	(0.63 x VTT) + 0.1GTLREF			V	
V_{OL_H}	(a), (b)	Host AGTL+ Output Low Voltage		1/3 x VTT	(1/3 x VTT) + 0.1GTLREF	V	
V_{OH_H}	(a), (b)	Host AGTL+ Output High Voltage	VTT–0.1	VTT		V	
RTT		Host termination Resistance	46	50	54	W	
I_{OL_H}	(a), (b)	Host AGTL+ Output Low Leakage			(0.63 x VTTmax) / RTT min	A	
I_{L_H}	(a), (c)	Host AGTL+ Input Leakage Current	10			µA	
C_{PAD}	(a), (c)	Host AGTL+ Input Capacitance	1		3.5	pF	
CCVREF	(d)	Host Common clock Reference Voltage		0.63 x VTT		V	
HxVREF	(d)	Host Address and Data Reference Voltage		0.63 x VTT		V	
HXSWNG, HYSWNG	(d)	Host Compensation Reference Voltage		1/3 x VTT		V	

Table 6-11. DDR Interface DC Characteristics

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
V_{IL} (DC)	(g), (i)	DDR Input Low Voltage			DVREF_x – 0.150	V	
V_{IH} (DC)	(g), (i)	DDR Input High Voltage	DVREF_x + 0.150			V	
V_{IL} (AC)	(g), (i)	DDR Input Low Voltage			DVREF_x – 0.310		
V_{IH} (AC)	(g), (i)	DDR Input High Voltage	DVREF_x + 0.310				
V_{OL}	(g), (h)	DDR Output Low Voltage	0		0.5	V	1
V_{OH}	(g), (h)	DDR Output High Voltage	1.9		VCC2_5	V	1
C_{Out}	(g), (h)	DDR Output Pin Capacitance	2.5		5	pF	
I_{OL} (DC)	(g), (h)	DDR Output Low Current			-35	mA	
I_{OH}	(g), (h)	DDR Output High Current			35	mA	
I_{OL} (AC)	(g), (h)	DDR Output Low Current			50	mA	
I_{OH} (AC)	(g), (h)	DDR Output High Current			50	mA	
I_{Leak}	(g), (i)	DDR Input Leakage Current			50	UA	
C_{IN}	(g), (i)	DDR Input Pin Capacitance	2.5		5	pF	
DVREF_x	(j)	DDR Reference Voltage		VCC2_5/2		V	

NOTE: 1. Actual values dependant on termination resistor values and RCOMP strength modes.

Table 6-12. AGP Interface DC Characteristics

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
V_{IL_AGP}	(k),(m)	AGP Interface Input Low Voltage			0.25	V	
V_{IH_AGP}	(k),(m)	AGP Interface Input High Voltage	0.450			V	
V_{OL_AGP}	(k),(l)	AGP Interface Output Low Voltage	-0.3		0.05	V	
V_{OH_AGP}	(k),(l)	AGP Interface Output High Voltage	0.750		0.850	V	
Z_{PD}		Pull-Down Impedance	0.90Ztarg		1.10Ztarg	Ω	
Z_{PU}		Pull-Up Impedance	0.90Ztarg		1.10Ztarg	Ω	
V_{CC1_5}		I/O Supply Voltage	1.425	1.5	1.575	V	
PREF_AGPx	(n)	AGP Interface Reference Voltage	0.3325	0.35	0.3675	V	
PSWNG_AGPx	(n)	AGP Interface Swing Reference Voltage		0.8		V	

Table 6-13. Hub Interface 2.0 (HI_B) with Parallel Buffer Mode Configured for 50 Ω

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
V_{IL_HI}	(o)	Hub Interface Input Low Voltage	-0.3	0	HIVREF–0.1	V	
V_{IH_HI}	(o)	Hub Interface Input High Voltage	HIVREF+ 0.1	0.7	1.2	V	
V_{OL_HI}	(o)	Hub Interface Output Low Voltage		0	0.05	V	
V_{OH_HI}	(o)	Hub Interface Output High Voltage	0.75	0.8	0.85	V	
I_{IL_HI}	(o)	Hub Interface Input Leakage Current			25	µA	
C_{IN_HI}	(o)	Hub Interface Input Pin Capacitance			5	pF	
ΔC_{IN}		Strobe to Data Pin Capacitance Delta	-0.5		0.5	pF	
L_{PIN}		Pin Inductance (signal)			5	nH	
Z_{PD}		Pull-Down Impedance		50		Ω	
Z_{PU}		Pull-Up Impedance		25		Ω	
VCC		I/O Supply Voltage		1.2		V	
CClk		CLK66 Pin Capacitance	5		8	pF	
PREF_B	(q)	Hub Interface Reference Voltage	0.343	0.35	0.357	V	
PSWNG_B	(q)	Hub Interface Swing Reference Voltage		0.8		V	

Table 6-14. Hub Interface 1.5 (HI_A) with Parallel Buffer Mode Configured for 50 Ω

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
V_{IL_HI}	(r)	Hub Interface Input Low Voltage	-0.3	0	HIVREF–0.1	V	
V_{IH_HI}	(r)	Hub Interface Input High Voltage	HIVREF+ 0.1	0.7	1.2	V	
V_{OL_HI}	(r)	Hub Interface Output Low Voltage		0	0.05	V	
V_{OH_HI}	(r)	Hub Interface Output High Voltage	0.75	0.8	0.85	V	
I_{IL_HI}	(r)	Hub Interface Input Leakage Current			25	µA	
C_{IN_HI}	(r)	Hub Interface Input Pin Capacitance			5	pF	
ΔC_{IN}		Strobe to data Pin Capacitance delta	-0.5		0.5	pF	
L_{PIN}		Pin Inductance (signal)			5	nH	
Z_{PD}		Pull-Down Impedance		50		Ω	
Z_{PU}		Pull-Up Impedance		25		Ω	
VCCP		I/O Supply Voltage		1.2		V	
CClk		CLK66 Pin Capacitance	5		8	pF	
PREF_A	(v)	Hub Interface Reference Voltage	0.343	0.35	0.357	V	
PSWNG_A	(v)	Hub Interface Swing Reference Voltage		0.8		V	

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Ballout and Package Information 7

This chapter provides the ballout and mechanical specifications for the E7505 chipset MCH. This information is intended to help with component placement and board routing.

7.1 Ballout Assignment

Figure 7-1 is a footprint of the package ballout showing the layout coordinates for the component balls and general ballout location of the MCH interfaces. Figure 7-2 and Figure 7-3 provide the ballout footprint listing the signal names by ball number. Table 7-1 provides the ballout listed alphabetically by signal name. Table 7-2 provides the ballout listed by ball number.

Figure 7-1. MCH Ballout Showing 1005 Pins (Top View)

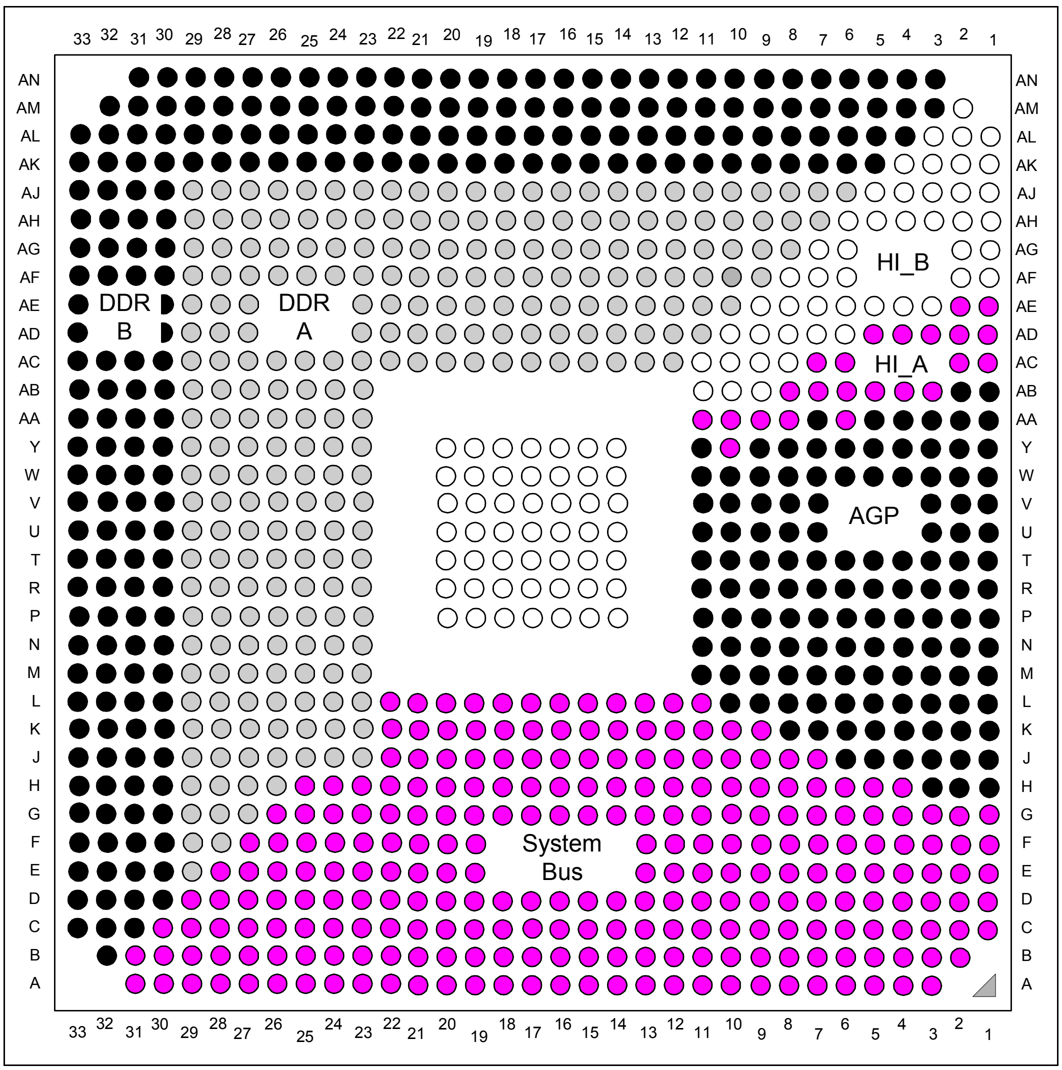


Figure 7-2. MCH Ballout (Left Half of Top View)

	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
AN			VSS	CB_B1	DQS_B17	VSS	CMDCLK _B0	DQ_B36	VSS	DQ_B34	MA_B0	VSS	DQ_B40	DQ_B44	VSS	DQ_B42	VSS
AM		VSS	VCCDDR	CB_B0	VCCDDR	CB_B3	CMDCLK _B0#	VSS	DQ_B33	DQS_B4	VCCDDR	MA_A10	VSS	VSS	DQ_B41	DQ_B46	VCCDDR
AL	VSS	VCCDDR	VSS	VSS	CB_B2	CB_B6	VSS	DQ_B32	DQS_B13	VSS	DQ_B35	MA_B10	VSS	DQ_B45	DQS_B14	VSS	DQ_B47
AK	DRCOMP _H	DRCOMP VREF_H	VCCDDR	CB_B5	DQS_B8	VSS	CB_B7	DQ_B37	VCCDDR	DQ_B38	DQ_B39	VSS	CMDCLK _A2	DQ_A45	VCCDDR	DQS_B5	DQ_B43
AJ	DRCOMP _V	VSS	DRCOMP VREF_V	CB_B4	VSS	CMDCLK _B1#	CMDCLK _B1	VSS	DQ_A36	DQ_A37	VSS	DQ_A39	CMDCLK _A2#	VSS	DQ_A41	DQ_A42	VSS
AH	VSS	RCVEN OUT_B#	RCVEN OUT_A#	VCCDDR	DQS_A17	DQS_A8	VCCDDR	VSS	MA_A0	VSS	DQ_A34	DQ_A38	VCCDDR	BA_A1	DQS_A14	VSS	DQ_A43
AG	ODTCOMP	DVREF_A	VSS	MA_A1	MA_B1	VSS	CB_A2	CB_A6	VSS	CMDCLK _A0#	DQS_A13	VSS	DQ_A35	BA_B1	VSS	DQS_A5	DQ_A46
AF	DVREF_B	VCCDDR	CMDCLK _B2	CMDCLK _B2#	VSS	VSS	CB_A0	CB_A1	CB_A7	CMDCLK _A0	VCCDDR	CMDCLK _A1#	DQS_A4	VSS	CMDCLK _A3	DQ_A44	VCCDDR
AE	VSS	DQ_B27	DQ_B31	VSS	DQ_A31	MA_B2	VSS	CB_A4	VSS	CB_A5	CB_A3	CMDCLK _A1	DQ_A32	DQ_A33	CMDCLK _A3#	DQ_A40	DQ_A47
AD	DQS_B12	DQ_B30	VSS	DQ_B26	DQ_A27	VCCDDR	MA_B3	MA_A2	CMDCLK _B3#	VCCDDR	VSS	VCCDDR	VSS	VCCDDR	VSS	VCCDDR	VSS
AC	DQ_B24	VSS	DQ_B25	DQS_B3	VSS	DQ_A26	DQ_A30	VSS	CMDCLK _B3	MA_A3	VCCDDR	VSS	VCCDDR	VSS	VCCDDR	VSS	VCCDDR
AB	VSS	DQ_B29	DQ_B28	VCCDDR	DQS_A3	DQS_A12	VSS	DQ_A29	DQ_A25	VCCDDR	VSS						
AA	MA_B6	MA_A6	VSS	MA_A4	MA_B4	VSS	VSS	DQ_A28	DQ_A24	VSS	VCCDDR						
Y	DQ_B19	VCCDDR	MA_B5	MA_A5	VSS	MA_B8	MA_A8	VCCDDR	VSS	VCCDDR	VSS			VCC[3]	VSS	VCC[3]	VSS
W	VSS	DQ_B18	DQ_B23	VSS	DQ_A19	DQ_A23	VSS	DQ_A22	DQ_A18	VSS	VCCDDR			VSS	VCC[3]	VSS	VCC[3]
V	DQS_B11	DQS_B2	VSS	DQ_B22	DQS_A2	VCCDDR	DQS_A11	DQ_A16	DQ_A20	VCCDDR	VSS			VCC[3]	VSS	VCC[3]	VSS
U	DQ_B16	VSS	DQ_B21	DQ_B17	VSS	DQ_A21	DQ_A17	VSS	VSS	VSS	VCCDDR			VSS	VCC[3]	VSS	VCC[3]
T	VSS	DQ_B20	MA_B9	VCCDDR	MA_A7	MA_B7	VSS	VSS	DQ_A12	VCCDDR	VSS			VCC[3]	VSS	VCC[3]	VSS
R	MA_B11	MA_A11	VSS	MA_A9	MA_B12	VSS	DQ_A11	DQ_A10	DQ_A9	VSS	VCCDDR			VSS	VCC[3]	VSS	VCC[3]
P	MA_A12	VCCDDR	DQ_B10	DQ_B11	VSS	DQ_A15	DQ_A14	VCCDDR	DQ_A8	VCCDDR	VSS			VCC[3]	VSS	VCC[3]	VSS
N	VSS	DQ_B14	DQ_B15	VSS	DQS_A1	DQS_A10	VSS	CKE_A2	CKE_B2	VSS	VCCDDR						
M	DQ_B13	DQS_B10	VSS	DQS_B1	DQ_A13	VCCDDR	VSS	DQ_A7	DQ_A4	VCCDDR	VSS						
L	DQ_B8	VSS	DQ_B9	VSS	VSS	CKE_B0	DQ_A3	VSS	DQ_A0	DDR _STRAP	VCCDDR	VSS	VTT	VSS	VTT	VSS	VTT
K	VSS	DQ_B12	CKE_A3	VCCDDR	CKE_A0	DQ_A6	VSS	DQS_A0	CMDCLK _A4	VCCDDR	VSS	VTT	VSS	VTT	VSS	VTT	VSS
J	CKE_A1	CKE_B1	VSS	CKE_B3	DQ_A2	VSS	DQ_A1	CMDCLK _A4#	VSS	RSTIN#	PWRGD	VSS	Reserved*	Reserved*	VSS	TESTIN#	HCLKINP
H	DQ_B3	VCCDDR	DQ_B7	DQ_B6	VSS	DQS_A9	CMDCLK _B4	VCCDDR	DINV0#	HD15#	VTT	HD24#	HDSTBP1#	VSS	HD44#	HD46#	VTT
G	VSS	DQ_B2	DQS_B0	VSS	DQ_A5	CMDCLK _B4#	VSS	HD4#	HD1#	VSS	HD14#	HDSTBN1#	VSS	HD31#	HD47#	VSS	HD50#
F	DQS_B9	DQ_B1	VSS	DQ_B5	VSS	VCCDDR	HD13#	HDSTBP0#	VSS	HDVREF0	HD26#	VTT	HDVREF1	HYRCOMP	VSS	HD49#	HD48#
E	DQ_B4	VSS	DQ_B0	VSS	VSS	HD9#	HDSTBN0#	VSS	HD12#	HD29#	VSS	HD30#	HYSWNG	VSS	HD42#	HD45#	VSS
D	VSS	CMDCLK _A5#	CMDCLK _A5	VCCDDR	HD6#	HD10#	VTT	HD11#	DINV1#	VSS	HD25#	HD28#	VTT	HD35#	HD38#	VSS	HD52#
C	CMDCLK _B5#	CMDCLK _B5	VSS	HD3#	HD2#	VSS	HD19#	HD21#	VSS	HD27#	HD34#	VSS	HD37#	HDSTBP2#	VSS	HD43#	HDSTBN3#
B		VCCDDR	HD0#	HD8#	VSS	HD17#	HD18#	VTT	HD22#	HD36#	VSS	HD33#	HDSTBN2#	VTT	HD41#	HD40#	VSS
A			HD7#	VTT	HD5#	HD16#	VSS	HD20#	HD23#	VSS	HD32#	HDVREF2	VSS	HD39#	DINV2#	VSS	HD51#
	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17

NOTES:

1. Signals marked with an "*" must have an accessible test point if XOR testing is implemented.
2. For AGP signals that have different names between AGP 2.0 and AGP 3.0, the name outside the parenthesis is the AGP 2.0 signal name and the name inside the parenthesis is the AGP 3.0 signal name.

Figure 7-3. MCH Ballout (Right Half of Top View)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VSS	WE_B#	CAS_A#	VSS	DQ_B53	DQ_B54	VSS	DQ_B55	MA_B13	VSS	VSS	DQS_B16	VSS	DQ_B59			AN
RAS_B#	WE_A#	VSS	DQ_B49	DQS_B6	VCCDDR	DQ_B51	MA_A13	VSS	DQ_B56	DQ_B61	VCCDDR	DQ_B58	DQ_B63	VSS		AM
RAS_A#	VSS	DQ_B52	DQ_B48	VSS	DQ_B50	Reserved	VSS	DQ_B60	DQ_B57	VSS	DQS_B7	DQ_B62	VSS	HI_B21	HI_B14	AL
VSS	DQ_A52	DQ_A53	VCCDDR	DQS_B15	CS_B1#	VSS	CS_B3#	DQS_A7	VCCDDR	CMDCLK _B7#	CMDCLK _B7	VSS	HI_B15	HI_B12	VSS	AK
VSS	DQS_A6	VSS	DQ_A54	CS_A1#	VSS	DQ_A61	DQS_A16	VSS	CMDCLK _A7#	CMDCLK _A7	VSS	PSWING_B	HI_B13	VCC[3]	HI_B11	AJ
VSS	VCCDDR	DQS_A15	CS_B0#	VSS	DQ_A60	DQ_A57	VCCDDR	CS_B4# / CMDCLK _B6#	CS_B5# / CMDCLK _B6	VSS	PU STRBS_B	PUSTRBF _B	VSS	HI_B9	HI_B10	AH
VSS	DQ_A50	DQ_A55	VSS	DQ_A56	DQ_A62	VSS	CS_A4# / CMDCLK _A6#	CS_A5# / CMDCLK _A6	VSS	PREF_B	HI_B17	VCC[3]	HI_B18	HI_B1	VSS	AG
BA_B0	DQ_A49	VSS	CS_A0#	DQ_A58	VCCDDR	CS_A2#	CS_A3#	VSS	PRCOMP_B	HI_B20	VSS	HI_B16	HI_B6	VSS	HI_B7	AF
BA_A0	DQ_A48	DQ_A51	CAS_B#	DQ_A63	DQ_A59	CS_B2#	VSS	PSTRBS_B	HI_B4	VCC[3]	HI_B5	PSTRBF_B	VSS	HI_A9	PREF_A	AE
VCCDDR	VSS	VCCDDR	VSS	VCCDDR	VSS	VCC[3]	HI_B8	HI_B0	VSS	HI_B3	PSTRBF_0	VCC[3]	HI_A2	PSWNG_A	VSS	AD
VSS	VCCDDR	VSS	VCCDDR	VSS	VCC[3]	VSS	HI_B2	VSS	HI_A4	HI_A10	VSS	HI_A3	HI_A1	VCC[3]	PRCOMP _A	AC
					VSS	VCC[3]	VSS	HI_A6	HI_A8	VCC[3]	PSTRBS_0	HI_A0	VSS	GTRDY# (GTRDY)	GSTOP# (GSTOP)	AB
					VCC[3]	VSS	HI_A7	HI_A5	VSS	HI_A11	GPAR	VSS	GAD0	GDEVSEL#(GDEVSEL)	VSS	AA
VCC[3]	VSS	VCC[3]			Reserved	VCC[3]	GCLKIN	VSS	Reserved	GFRAME# (GFRAME)	VSS	GAD1	GAD2	VSS	GAD3	Y
VSS	VCC[3]	VSS			Reserved	VSS	VSS	GAD8	GIRDY# (GIRDY)	VCCAGP	GAD6	GAD4	VSS	GAD5	GAD7	W
VCC[3]	VSS	VCC[3]			VSS	VCCAGP	SERR# (SERR)	GAD14	VSS	GAD10	GAD9	VCCAGP	AD_STB0 (AD_STBF0)	AD_STB0# (AD_STBS0)	VSS	V
VSS	VCCAHI	VSS			VCCAGP	VSS	GC/BE1# (GC#/BE1)	VCCAGP	GAD12	GAD11	VSS	PSWNG _AGP1	PREF _AGP0	VCCAGP	GC/BE0# (GC#/BE0)	U
VCC[3]	VSS	VCC[3]			VSS	VCCAGP	VSS	GC/BE2# (GC#/BE2)	GAD13	VSS	PRCOMP_ AGP0	GAD21	VSS	PREF_AGP1	GAD23	T
VSS	VCC[3]	VSS			VCCAGP	VSS	GAD16	GAD15	VSS	TESTSIG2*	TESTSIG1*	VSS	AD_STB1# (AD_STBS1)	GC/BE3# (GC#/BE3)	VSS	R
VCCAFSB	VSS	VCC[3]			VSS	VCCAGP	GAD17	VSS	GAD18	GAD20	VSS	PRCOMP _AGP1	AD_STB1 (AD_STBF1)	VSS	GAD25	P
					VCCAGP	VSS	VSS	GAD19	GAD22	VCCAGP	PSWNG _AGP0	GAD24	VSS	GAD28	GAD27	N
					VSS	VCCAGP	PIPE# (DBI_HI)	DBI_LO	VSS	GAD31	GAD26	VCCAGP	GAD29	GAD30	VSS	M
VSS	VTT	VSS	VTT	VSS	VTT	VSS	Reserved	VCCAGP	SBA6 (SBA6#)	SBA7 (SBA7#)	VSS	SBA5 (SBA5#)	SB_STB (SB_STBF)	VCCAGP	SBA4 (SBA4#)	L
VTT	VSS	VTT	VSS	VTT	VSS	VTT	VSS	GGNT# (GGNT)	SBA0 (SBA0#)	VSS	WBF# (WBF)	SBA2 (SBA2#)	VSS	SB_STB# (SB_STBS)	SBA3 (SBA3#)	K
HCLKINN	VSS	VSS	VSS	HA18#	HA19#	VSS	HA25#	HA28#	VSS	GREQ# (GREQ)	ST2	VSS	RBF# (RBF)	SBA1 (SBA1#)	VSS	J
DEFER#	HA3#	VSS	HREQ2#	HA17#	VTT	HA24#	HADSTB1#	VSS	HA30#	HA22#	VTT	BINIT#	ST1	VSS	ST0	H
HXSWNG	VSS	HREQ4#	HREQ1#	VSS	HA7#	HREQ0#	VSS	HA23#	HA29#	VSS	HA34#	CPURST#	VSS	VSS	XORMODE#	G
VTT	BPRI#	RS1#	VSS	BREQ0#	HA4#	VTT	HA9#	HAVREF0	VSS	HA21#	HA26#	VTT	AP0#	AP1#	VSS	F
HDSTBP3#	HITM#	VSS	RS2#	RS0#	VSS	HREQ3#	HA6#	VSS	HA11#	HA20#	VSS	HA35#	HA31#	VSS	RSP#	E
HD53#	VTT	HD57#	HIT#	VSS	HTRDY#	DEP1#	VTT	HA5#	HA8#	VSS	HA16#	HA27#	VTT	HAVREF1	XERR#	D
VSS	DINV3#	HD56#	VSS	HD59#	HXRCOMP	VSS	DEP0#	DEP2#	VSS	HADSTB0#	HA12#	VSS	HA33#	HA32#	VSS	C
HD55#	HD62#	VTT	HD58#	HD60#	VSS	BNR#	CCVREF	VTT	DBSY#	DEP3#	VSS	HA13#	HA14#	VTT		B
HD54#	VSS	HD61#	HD63#	VSS	HDVREF3	ADS#	VSS	DRDY#	HLOCK#	VSS	HA15#	HA10#	VSS			A
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

NOTES:
1. Signals marked with an "*" must have an accessible test point if XOR testing is implemented.
2. For AGP signals that have different names between AGP 2.0 and AGP 3.0, the name outside the parenthesis is the AGP 2.0 signal name and the name inside the parenthesis is the AGP 3.0 signal name.

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
AD_STB0# (AD_STBS0)	V2
AD_STB0 (AD_STBF0)	V3
AD_STB1# (AD_STBS1)	R3
AD_STB1 (AD_STBF1)	P3
ADS#	A10
AP0#	F3
AP1#	F2
BA_A0	AE16
BA_A1	AH20
BA_B0	AF16
BA_B1	AG20
BINIT#	H4
BNR#	B10
BPRI#	F15
BREQ0#	F12
CAS_A#	AN14
CAS_B#	AE13
CB_A0	AF27
CB_A1	AF26
CB_A2	AG27
CB_A3	AE23
CB_A4	AE26
CB_A5	AE24
CB_A6	AG26
CB_A7	AF25
CB_B0	AM30
CB_B1	AN30
CB_B2	AL29
CB_B3	AM28
CB_B4	AJ30
CB_B5	AK30
CB_B6	AL28
CB_B7	AK27
CCVREF	B9
CKE_A0	K29
CKE_A1	J33
CKE_A2	N26
CKE_A3	K31

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
CKE_B0	L28
CKE_B1	J32
CKE_B2	N25
CKE_B3	J30
CMDCLK_A0	AF24
CMDCLK_A0#	AG24
CMDCLK_A1	AE22
CMDCLK_A1#	AF22
CMDCLK_A2	AK21
CMDCLK_A2#	AJ21
CMDCLK_A3	AF19
CMDCLK_A3#	AE19
CMDCLK_A4	K25
CMDCLK_A4#	J26
CMDCLK_A5	D31
CMDCLK_A5#	D32
CMDCLK_A7	AJ6
CMDCLK_A7#	AJ7
CMDCLK_B0	AN27
CMDCLK_B0#	AM27
CMDCLK_B1	AJ27
CMDCLK_B1#	AJ28
CMDCLK_B2	AF31
CMDCLK_B2#	AF30
CMDCLK_B3	AC25
CMDCLK_B3#	AD25
CMDCLK_B4	H27
CMDCLK_B4#	G28
CMDCLK_B5	C32
CMDCLK_B5#	C33
CMDCLK_B7	AK5
CMDCLK_B7#	AK6
CPURST#	G4
CS_A0#	AF13
CS_A1#	AJ12
CS_A2#	AF10
CS_A3#	AF9
CS_A4#/CMDCLK_A6#	AG9

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
CS_A5#/CMDCLK_A6	AG8
CS_B0#	AH13
CS_B1#	AK11
CS_B2#	AE10
CS_B3#	AK9
CS_B4#/CMDCLK_B6#	AH8
CS_B5#/CMDCLK_B6	AH7
DBI_LO	M8
DBSY#	B7
DDR_STRAP	L24
DEFER#	H16
DEP0#	C9
DEP1#	D10
DEP2#	C8
DEP3#	B6
DINV0#	H25
DINV1#	D25
DINV2#	A19
DINV3#	C15
DQ_A00	L25
DQ_A1	J27
DQ_A2	J29
DQ_A3	L27
DQ_A4	M25
DQ_A5	G29
DQ_A6	K28
DQ_A7	M26
DQ_A8	P25
DQ_A9	R25
DQ_A10	R26
DQ_A11	R27
DQ_A12	T25
DQ_A13	M29
DQ_A14	P27
DQ_A15	P28
DQ_A16	V26
DQ_A17	U27
DQ_A18	W25

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
DQ_A19	W29
DQ_A20	V25
DQ_A21	U28
DQ_A22	W26
DQ_A23	W28
DQ_A24	AA25
DQ_A25	AB25
DQ_A26	AC28
DQ_A27	AD29
DQ_A28	AA26
DQ_A29	AB26
DQ_A30	AC27
DQ_A31	AE29
DQ_A32	AE21
DQ_A33	AE20
DQ_A34	AH23
DQ_A35	AG21
DQ_A36	AJ25
DQ_A37	AJ24
DQ_A38	AH22
DQ_A39	AJ22
DQ_A40	AE18
DQ_A41	AJ19
DQ_A42	AJ18
DQ_A43	AH17
DQ_A44	AF18
DQ_A45	AK20
DQ_A46	AG17
DQ_A47	AE17
DQ_A48	AE15
DQ_A49	AF15
DQ_A50	AG15
DQ_A51	AE14
DQ_A52	AK15
DQ_A53	AK14
DQ_A54	AJ13
DQ_A55	AG14
DQ_A56	AG12

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
DQ_A57	AH10
DQ_A58	AF12
DQ_A59	AE11
DQ_A60	AH11
DQ_A61	AJ10
DQ_A62	AG11
DQ_A63	AE12
DQ_B0	E31
DQ_B1	F32
DQ_B2	G32
DQ_B3	H33
DQ_B4	E33
DQ_B5	F30
DQ_B6	H30
DQ_B7	H31
DQ_B8	L33
DQ_B9	L31
DQ_B10	P31
DQ_B11	P30
DQ_B12	K32
DQ_B13	M33
DQ_B14	N32
DQ_B15	N31
DQ_B16	U33
DQ_B17	U30
DQ_B18	W32
DQ_B19	Y33
DQ_B20	T32
DQ_B21	U31
DQ_B22	V30
DQ_B23	W31
DQ_B24	AC33
DQ_B25	AC31
DQ_B26	AD30
DQ_B27	AE32
DQ_B28	AB31
DQ_B29	AB32
DQ_B30	AD32

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
DQ_B31	AE31
DQ_B32	AL26
DQ_B33	AM25
DQ_B34	AN24
DQ_B35	AL23
DQ_B36	AN26
DQ_B37	AK26
DQ_B38	AK24
DQ_B39	AK23
DQ_B40	AN21
DQ_B41	AM19
DQ_B42	AN18
DQ_B43	AK17
DQ_B44	AN20
DQ_B45	AL20
DQ_B46	AM18
DQ_B47	AL17
DQ_B48	AL13
DQ_B49	AM13
DQ_B50	AL11
DQ_B51	AM10
DQ_B52	AL14
DQ_B53	AN12
DQ_B54	AN11
DQ_B55	AN9
DQ_B56	AM7
DQ_B57	AL7
DQ_B58	AM4
DQ_B59	AN3
DQ_B60	AL8
DQ_B61	AM6
DQ_B62	AL4
DQ_B63	AM3
DQS_A0	K26
DQS_A1	N29
DQS_A2	V29
DQS_A3	AB29
DQS_A4	AF21

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
DQS_A5	AG18
DQS_A6	AJ15
DQS_A7	AK8
DQS_A8	AH28
DQS_A9	H28
DQS_A10	N28
DQS_A11	V27
DQS_A12	AB28
DQS_A13	AG23
DQS_A14	AH19
DQS_A15	AH14
DQS_A16	AJ9
DQS_A17	AH29
DQS_B0	G31
DQS_B1	M30
DQS_B2	V32
DQS_B3	AC30
DQS_B4	AM24
DQS_B5	AK18
DQS_B6	AM12
DQS_B7	AL5
DQS_B8	AK29
DQS_B9	F33
DQS_B10	M32
DQS_B11	V33
DQS_B12	AD33
DQS_B13	AL25
DQS_B14	AL19
DQS_B15	AK12
DQS_B16	AN5
DQS_B17	AN29
DRCOMP_H	AK33
DRCOMP_V	AJ33
DRCOMPVREF_H	AK32
DRCOMPVREF_V	AJ31
DRDY#	A8
DVREF_A	AG32
DVREF_B	AF33

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
GAD0	AA3
GAD1	Y4
GAD2	Y3
GAD3	Y1
GAD4	W4
GAD5	W2
GAD6	W5
GAD7	W1
GAD8	W8
GAD9	V5
GAD10	V6
GAD11	U6
GAD12	U7
GAD13	T7
GAD14	V8
GAD15	R8
GAD16	R9
GAD17	P9
GAD18	P7
GAD19	N8
GAD20	P6
GAD21	T4
GAD22	N7
GAD23	T1
GAD24	N4
GAD25	P1
GAD26	M5
GAD27	N1
GAD28	N2
GAD29	M3
GAD30	M2
GAD31	M6
GC/BE0# (GC#/BE0)	U1
GC/BE1# (GC#/BE1)	U9
GC/BE2# (GC#/BE2)	T8
GC/BE3# (GC#/BE3)	R2
GCLKIN	Y9
GDEVSEL# (GDEVSEL)	AA2

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
GFRAME# (FRAME)	Y6
GGNT# (GGNT)	K8
GIRDY# (GIRDY)	W7
GPAR	AA5
GREQ# (GREQ)	J6
GSTOP# (GSTOP)	AB1
GTRDY# (GTRDY)	AB2
HA3#	H15
HA4#	F11
HA5#	D8
HA6#	E9
HA7#	G11
HA8#	D7
HA9#	F9
HA10#	A4
HA11#	E7
HA12#	C5
HA13#	B4
HA14#	B3
HA15#	A5
HA16#	D5
HA17#	H12
HA18#	J12
HA19#	J11
HA20#	E6
HA21#	F6
HA22#	H6
HA23#	G8
HA24#	H10
HA25#	J9
HA26#	F5
HA27#	D4
HA28#	J8
HA29#	G7
HA30#	H7
HA31#	E3
HA32#	C2
HA33#	C3

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
HA34#	G5
HA35#	E4
HADSTB0#	C6
HADSTB1#	H9
HAVREF0	F8
HAVREF1	D2
HCLKINN	J16
HCLKINP	J17
HD0#	B31
HD1#	G25
HD2#	C29
HD3#	C30
HD4#	G26
HD5#	A29
HD6#	D29
HD7#	A31
HD8#	B30
HD9#	E28
HD10#	D28
HD11#	D26
HD12#	E25
HD13#	F27
HD14#	G23
HD15#	H24
HD16#	A28
HD17#	B28
HD18#	B27
HD19#	C27
HD20#	A26
HD21#	C26
HD22#	B25
HD23#	A25
HD24#	H22
HD25#	D23
HD26#	F23
HD27#	C24
HD28#	D22
HD29#	E24

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
HD30#	E22
HD31#	G20
HD32#	A23
HD33#	B22
HD34#	C23
HD35#	D20
HD36#	B24
HD37#	C21
HD38#	D19
HD39#	A20
HD40#	B18
HD41#	B19
HD42#	E19
HD43#	C18
HD44#	H19
HD45#	E18
HD46#	H18
HD47#	G19
HD48#	F17
HD49#	F18
HD50#	G17
HD51#	A17
HD52#	D17
HD53#	D16
HD54#	A16
HD55#	B16
HD56#	C14
HD57#	D14
HD58#	B13
HD59#	C12
HD60#	B12
HD61#	A14
HD62#	B15
HD63#	A13
HDSTBN0#	E27
HDSTBN1#	G22
HDSTBN2#	B21
HDSTBN3#	C17

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
HDSTBP0#	F26
HDSTBP1#	H21
HDSTBP2#	C20
HDSTBP3#	E16
HDVREF0	F24
HDVREF1	F21
HDVREF2	A22
HDVREF3	A11
HI_A0	AB4
HI_A1	AC3
HI_A2	AD3
HI_A3	AC4
HI_A4	AC7
HI_A5	AA8
HI_A6	AB8
HI_A7	AA9
HI_A8	AB7
HI_A9	AE2
HI_A10	AC6
HI_A11	AA6
HI_B00	AD8
HI_B01	AG2
HI_B02	AC9
HI_B03	AD6
HI_B04	AE7
HI_B05	AE5
HI_B06	AF3
HI_B07	AF1
HI_B08	AD9
HI_B09	AH2
HI_B10	AH1
HI_B11	AJ1
HI_B12	AK2
HI_B13	AJ3
HI_B14	AL1
HI_B15	AK3
HI_B16	AF4
HI_B17	AG5

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
HI_B18	AG3
HI_B20	AF6
HI_B21	AL2
HIT#	D13
HITM#	E15
HLOCK#	A7
HREQ0#	G10
HREQ1#	G13
HREQ2#	H13
HREQ3#	E10
HREQ4#	G14
HTRDY#	D11
HXRCOMP	C11
HXSWNG	G16
HYRCOMP	F20
HYSWNG	E21
MA_A0	AH25
MA_A1	AG30
MA_A2	AD26
MA_A3	AC24
MA_A4	AA30
MA_A5	Y30
MA_A6	AA32
MA_A7	T29
MA_A8	Y27
MA_A9	R30
MA_A10	AM22
MA_A11	R32
MA_A12	P33
MA_A13	AM9
MA_B0	AN23
MA_B1	AG29
MA_B2	AE28
MA_B3	AD27
MA_B4	AA29
MA_B5	Y31
MA_B6	AA33
MA_B7	T28

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
MA_B8	Y28
MA_B9	T31
MA_B10	AL22
MA_B11	R33
MA_B12	R29
MA_B13	AN8
ODTCOMP	AG33
PIPE# (DBI_HI)	M9
PRCOMP_A	AC1
PRCOMP_AGP0	T5
PRCOMP_AGP1	P4
PRCOMP_B	AF7
PREF_A	AE1
PREF_AGP0	U3
PREF_AGP1	T2
PREF_B	AG6
PSTRBF_0	AD5
PSTRBF_B	AE4
PSTRBS_0	AB5
PSTRBS_B	AE8
PSWING_B	AJ4
PSWNG_A	AD2
PSWNG_AGP0	N5
PSWNG_AGP1	U4
PUSTRBF_B	AH4
PUSTRBS_B	AH5
PWRGD	J23
RAS_A#	AL16
RAS_B#	AM16
RBF# (RBF)	J3
RCVENOUT_A#	AH31
RCVENOUT_B#	AH32
Reserved	AL10
Reserved	L9
Reserved	Y7
Reserved	Y11
Reserved	W11
Reserved*	J21

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
Reserved*	J20
RS0#	E12
RS1#	F14
RS2#	E13
RSP#	E1
RSTIN#	J24
SB_STB# (SB_STBS)	K2
SB_STB (SB_STBF)	L3
SBA0 (SBA0#)	K7
SBA1 (SBA1#)	J2
SBA2 (SBA2#)	K4
SBA3 (SBA3#)	K1
SBA4 (SBA4#)	L1
SBA5 (SBA5#)	L4
SBA6 (SBA6#)	L7
SBA7 (SBA7#)	L6
SERR# (SERR)	V9
ST0	H1
ST1	H3
ST2	J5
TESTIN#	J18
TESTSIG1*	R5
TESTSIG2*	R6
VCC[3]	AA11
VCC[3]	AB10
VCC[3]	AB6
VCC[3]	AC11
VCC[3]	AC2
VCC[3]	AD10
VCC[3]	AD4
VCC[3]	AE6
VCC[3]	AG4
VCC[3]	AJ2
VCC[3]	P14
VCC[3]	P18
VCC[3]	R15
VCC[3]	R17
VCC[3]	R19

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
VCC3	T14
VCC3	T16
VCC3	T18
VCC3	U17
VCC3	U19
VCC3	V14
VCC3	V16
VCC3	V18
VCC3	W15
VCC3	W17
VCC3	W19
VCC3	Y10
VCC3	P20
VCC3	T20
VCC3	V20
VCC3	Y14
VCC3	Y16
VCC3	Y18
VCC3	Y20
VCCAFSB	P16
VCCAGP	L2
VCCAGP	L8
VCCAGP	M10
VCCAGP	M4
VCCAGP	N11
VCCAGP	N6
VCCAGP	P10
VCCAGP	R11
VCCAGP	T10
VCCAGP	U11
VCCAGP	U2
VCCAGP	U8
VCCAGP	V10
VCCAGP	V4
VCCAGP	W6
VCCAHI	U15
VCCDDR	AA23
VCCDDR	AB24

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
VCCDDR	AB30
VCCDDR	AC13
VCCDDR	AC15
VCCDDR	AC17
VCCDDR	AC19
VCCDDR	AC21
VCCDDR	AC23
VCCDDR	AD12
VCCDDR	AD14
VCCDDR	AD16
VCCDDR	AD18
VCCDDR	AD20
VCCDDR	AD22
VCCDDR	AD24
VCCDDR	AD28
VCCDDR	AF11
VCCDDR	AF17
VCCDDR	AF23
VCCDDR	AF32
VCCDDR	AH15
VCCDDR	AH21
VCCDDR	AH27
VCCDDR	AH30
VCCDDR	AH9
VCCDDR	AK13
VCCDDR	AK19
VCCDDR	AK25
VCCDDR	AK31
VCCDDR	AK7
VCCDDR	AL32
VCCDDR	AM11
VCCDDR	AM17
VCCDDR	AM23
VCCDDR	AM29
VCCDDR	AM31
VCCDDR	AM5
VCCDDR	B32
VCCDDR	D30

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
VCCDDR	F28
VCCDDR	H26
VCCDDR	H32
VCCDDR	K24
VCCDDR	K30
VCCDDR	L23
VCCDDR	M24
VCCDDR	M28
VCCDDR	N23
VCCDDR	P24
VCCDDR	P26
VCCDDR	P32
VCCDDR	R23
VCCDDR	T24
VCCDDR	T30
VCCDDR	U23
VCCDDR	V24
VCCDDR	V28
VCCDDR	W23
VCCDDR	Y24
VCCDDR	Y26
VCCDDR	Y32
VSS	A12
VSS	A15
VSS	A18
VSS	A21
VSS	A24
VSS	A27
VSS	A3
VSS	A6
VSS	A9
VSS	AA1
VSS	AA10
VSS	AA24
VSS	AA27
VSS	AA28
VSS	AA31
VSS	AA4

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
VSS	AA7
VSS	AB11
VSS	AB23
VSS	AB27
VSS	AB3
VSS	AB33
VSS	AB9
VSS	AC10
VSS	AC12
VSS	AC14
VSS	AC16
VSS	AC18
VSS	AC20
VSS	AC22
VSS	AC26
VSS	AC29
VSS	AC32
VSS	AC5
VSS	AC8
VSS	AD1
VSS	AD11
VSS	AD13
VSS	AD15
VSS	AD17
VSS	AD19
VSS	AD21
VSS	AD23
VSS	AD31
VSS	AD7
VSS	AE25
VSS	AE27
VSS	AE3
VSS	AE30
VSS	AE33
VSS	AE9
VSS	AF14
VSS	AF2
VSS	AF20

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
VSS	AF28
VSS	AF29
VSS	AF5
VSS	AF8
VSS	AG1
VSS	AG10
VSS	AG13
VSS	AG16
VSS	AG19
VSS	AG22
VSS	AG25
VSS	AG28
VSS	AG31
VSS	AG7
VSS	AH12
VSS	AH16
VSS	AH18
VSS	AH24
VSS	AH26
VSS	AH3
VSS	AH33
VSS	AH6
VSS	AJ11
VSS	AJ14
VSS	AJ16
VSS	AJ17
VSS	AJ20
VSS	AJ23
VSS	AJ26
VSS	AJ29
VSS	AJ32
VSS	AJ5
VSS	AJ8
VSS	AK1
VSS	AK10
VSS	AK16
VSS	AK22
VSS	AK28

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
VSS	AK4
VSS	AL12
VSS	AL15
VSS	AL18
VSS	AL21
VSS	AL24
VSS	AL27
VSS	AL3
VSS	AL30
VSS	AL31
VSS	AL33
VSS	AL6
VSS	AL9
VSS	AM14
VSS	AM2
VSS	AM20
VSS	AM21
VSS	AM26
VSS	AM32
VSS	AM8
VSS	AN10
VSS	AN13
VSS	AN16
VSS	AN17
VSS	AN19
VSS	AN22
VSS	AN25
VSS	AN28
VSS	AN31
VSS	AN4
VSS	AN6
VSS	AN7
VSS	B11
VSS	B17
VSS	B23
VSS	B29
VSS	B5
VSS	C1

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
VSS	C10
VSS	C13
VSS	C16
VSS	C19
VSS	C22
VSS	C25
VSS	C28
VSS	C31
VSS	C4
VSS	C7
VSS	D12
VSS	D18
VSS	D24
VSS	D33
VSS	D6
VSS	E11
VSS	E14
VSS	E17
VSS	E2
VSS	E20
VSS	E23
VSS	E26
VSS	E29
VSS	E30
VSS	E32
VSS	E5
VSS	E8
VSS	F1
VSS	F13
VSS	F19
VSS	F25
VSS	F29
VSS	F31
VSS	F7
VSS	G12
VSS	G15
VSS	G18
VSS	G21

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
VSS	G24
VSS	G27
VSS	G2
VSS	G3
VSS	G30
VSS	G33
VSS	G6
VSS	G9
VSS	H14
VSS	H2
VSS	H20
VSS	H29
VSS	H8
VSS	J1
VSS	J10
VSS	J13
VSS	J14
VSS	J15
VSS	J19
VSS	J22
VSS	J25
VSS	J28
VSS	J31
VSS	J4
VSS	J7
VSS	K11
VSS	K13
VSS	K15
VSS	K17
VSS	K19
VSS	K21
VSS	K23
VSS	K27
VSS	K3
VSS	K33
VSS	K6
VSS	K9
VSS	L10

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
VSS	L12
VSS	L14
VSS	L16
VSS	L18
VSS	L20
VSS	L22
VSS	L26
VSS	L29
VSS	L30
VSS	L32
VSS	L5
VSS	M1
VSS	M11
VSS	M23
VSS	M27
VSS	M31
VSS	M7
VSS	N10
VSS	N24
VSS	N27
VSS	N3
VSS	N30
VSS	N33
VSS	N9
VSS	P11
VSS	P15
VSS	P17
VSS	P19
VSS	P2
VSS	P23
VSS	P29
VSS	P5
VSS	P8
VSS	R1
VSS	R10
VSS	R14
VSS	R16
VSS	R18

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
VSS	R20
VSS	R24
VSS	R28
VSS	R31
VSS	R4
VSS	R7
VSS	T11
VSS	T15
VSS	T17
VSS	T19
VSS	T23
VSS	T26
VSS	T27
VSS	T3
VSS	T33
VSS	T6
VSS	T9
VSS	U10
VSS	U14
VSS	U16
VSS	U18
VSS	U20
VSS	U24
VSS	U25
VSS	U26
VSS	U29
VSS	U32
VSS	U5
VSS	V1
VSS	V11
VSS	V15
VSS	V17
VSS	V19
VSS	V23
VSS	V31
VSS	V7
VSS	W10
VSS	W14

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
VSS	W16
VSS	W18
VSS	W20
VSS	W24
VSS	W27
VSS	W3
VSS	W30
VSS	W33
VSS	W9
VSS	Y15
VSS	Y17
VSS	Y19
VSS	Y2
VSS	Y23
VSS	Y25
VSS	Y29
VSS	Y5
VSS	Y8
VTT	A30
VTT	B14
VTT	B2
VTT	B20
VTT	B26
VTT	B8
VTT	D15
VTT	D21
VTT	D27
VTT	D3
VTT	D9
VTT	F10
VTT	F16
VTT	F22
VTT	F4
VTT	H11
VTT	H17
VTT	H23
VTT	H5
VTT	K10

Table 7-1. MCH Ball List by Signal Name

Signal Name	Ball #
VTT	K12
VTT	K14
VTT	K16
VTT	K18
VTT	K20
VTT	K22
VTT	L11
VTT	L13
VTT	L15
VTT	L17
VTT	L19
VTT	L21
WBF# (WBF)	K5
WE_A#	AM15
WE_B#	AN15
XERR#	D1
XORMODE#	G1

NOTES:

1. Signals marked with an "*" must have an accessible test point if XOR testing is implemented.
2. For AGP signals that have different names between AGP 2.0 and AGP 3.0, the name outside the parenthesis is the AGP 2.0 signal name and the name inside the parenthesis is the AGP 3.0 signal name.
3. VCC applies to both 1.2 V and 1.3 V parts

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
A3	VSS
A4	HA10#
A5	HA15#
A6	VSS
A7	HLOCK#
A8	DRDY#
A9	VSS
A10	ADS#
A11	HDVREF3
A12	VSS
A13	HD63#
A14	HD61#
A15	VSS
A16	HD54#
A17	HD51#
A18	VSS
A19	DINV2#
A20	HD39#
A21	VSS
A22	HDVREF2
A23	HD32#
A24	VSS
A25	HD23#
A26	HD20#
A27	VSS
A28	HD16#
A29	HD5#
A30	VTT
A31	HD7#
B2	VTT
B3	HA14#
B4	HA13#
B5	VSS
B6	DEP3#
B7	DBSY#
B8	VTT
B9	CCVREF
B10	BNR#

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
B11	VSS
B12	HD60#
B13	HD58#
B14	VTT
B15	HD62#
B16	HD55#
B17	VSS
B18	HD40#
B19	HD41#
B20	VTT
B21	HDSTBN2#
B22	HD33#
B23	VSS
B24	HD36#
B25	HD22#
B26	VTT
B27	HD18#
B28	HD17#
B29	VSS
B30	HD8#
B31	HD0#
B32	VCCDDR
C1	VSS
C2	HA32#
C3	HA33#
C4	VSS
C5	HA12#
C6	HADSTB0#
C7	VSS
C8	DEP2#
C9	DEP0#
C10	VSS
C11	HXRCOMP
C12	HD59#
C13	VSS
C14	HD56#
C15	DINV3#
C16	VSS

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
C17	HDSTBN3#
C18	HD43#
C19	VSS
C20	HDSTBP2#
C21	HD37#
C22	VSS
C23	HD34#
C24	HD27#
C25	VSS
C26	HD21#
C27	HD19#
C28	VSS
C29	HD2#
C30	HD3#
C31	VSS
C32	CMDCLK_B5
C33	CMDCLK_B5#
D1	XERR#
D2	HAVREF1
D3	VTT
D4	HA27#
D5	HA16#
D6	VSS
D7	HA8#
D8	HA5#
D9	VTT
D10	DEP1#
D11	HTRDY#
D12	VSS
D13	HIT#
D14	HD57#
D15	VTT
D16	HD53#
D17	HD52#
D18	VSS
D19	HD38#
D20	HD35#
D21	VTT

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
D22	HD28#
D23	HD25#
D24	VSS
D25	DINV1#
D26	HD11#
D27	VTT
D28	HD10#
D29	HD6#
D30	VCCDDR
D31	CMDCLK_A5
D32	CMDCLK_A5#
D33	VSS
E1	RSP#
E2	VSS
E3	HA31#
E4	HA35#
E5	VSS
E6	HA20#
E7	HA11#
E8	VSS
E9	HA6#
E10	HREQ3#
E11	VSS
E12	RS0#
E13	RS2#
E14	VSS
E15	HITM#
E16	HDSTBP3#
E17	VSS
E18	HD45#
E19	HD42#
E20	VSS
E21	HYSWNG
E22	HD30#
E23	VSS
E24	HD29#
E25	HD12#
E26	VSS

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
E27	HDSTBN0#
E28	HD9#
E29	VSS
E30	VSS
E31	DQ_B0
E32	VSS
E33	DQ_B4
F1	VSS
F2	AP1#
F3	AP0#
F4	VTT
F5	HA26#
F6	HA21#
F7	VSS
F8	HAVREF0
F9	HA9#
F10	VTT
F11	HA4#
F12	BREQ0#
F13	VSS
F14	RS1#
F15	BPRI#
F16	VTT
F17	HD48#
F18	HD49#
F19	VSS
F20	HYRCOMP
F21	HDVREF1
F22	VTT
F23	HD26#
F24	HDVREF0
F25	VSS
F26	HDSTBP0#
F27	HD13#
F28	VCCDDR
F29	VSS
F30	DQ_B5
F31	VSS

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
F32	DQ_B1
F33	DQS_B9
G1	XORMODE#
G2	VSS
G3	VSS
G4	CPURST#
G5	HA34#
G6	VSS
G7	HA29#
G8	HA23#
G9	VSS
G10	HREQ0#
G11	HA7#
G12	VSS
G13	HREQ1#
G14	HREQ4#
G15	VSS
G16	HXSWNG
G17	HD50#
G18	VSS
G19	HD47#
G20	HD31#
G21	VSS
G22	HDSTBN1#
G23	HD14#
G24	VSS
G25	HD1#
G26	HD4#
G27	VSS
G28	CMDCLK_B4#
G29	DQ_A5
G30	VSS
G31	DQS_B0
G32	DQ_B2
G33	VSS
H1	ST0
H2	VSS
H3	ST1

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
H4	BINIT#
H5	VTT
H6	HA22#
H7	HA30#
H8	VSS
H9	HADSTB1#
H10	HA24#
H11	VTT
H12	HA17#
H13	HREQ2#
H14	VSS
H15	HA3#
H16	DEFER#
H17	VTT
H18	HD46#
H19	HD44#
H20	VSS
H21	HDSTBP1#
H22	HD24#
H23	VTT
H24	HD15#
H25	DINV0#
H26	VCCDDR
H27	CMDCLK_B4
H28	DQS_A9
H29	VSS
H30	DQ_B6
H31	DQ_B7
H32	VCCDDR
H33	DQ_B3
J1	VSS
J2	SBA1 (SBA1#)
J3	RBF# (RBF)
J4	VSS
J5	ST2
J6	GREQ# (GREQ)
J7	VSS
J8	HA28#

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
J9	HA25#
J10	VSS
J11	HA19#
J12	HA18#
J13	VSS
J14	VSS
J15	VSS
J16	HCLKINN
J17	HCLKINP
J18	TESTIN#
J19	VSS
J20	Reserved*
J21	Reserved*
J22	VSS
J23	PWRGD
J24	RSTIN#
J25	VSS
J26	CMDCLK_A4#
J27	DQ_A1
J28	VSS
J29	DQ_A2
J30	CKE_B3
J31	VSS
J32	CKE_B1
J33	CKE_A1
K1	SBA3 (SBA3#)
K2	SB_STB# (SB_STBS)
K3	VSS
K4	SBA2 (SBA2#)
K5	WBF# (WBF)
K6	VSS
K7	SBA0 (SBA0#)
K8	GGNT# (GGNT)
K9	VSS
K10	VTT
K11	VSS
K12	VTT
K13	VSS

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
K14	VTT
K15	VSS
K16	VTT
K17	VSS
K18	VTT
K19	VSS
K20	VTT
K21	VSS
K22	VTT
K23	VSS
K24	VCCDDR
K25	CMDCLK_A4
K26	DQS_A0
K27	VSS
K28	DQ_A6
K29	CKE_A0
K30	VCCDDR
K31	CKE_A3
K32	DQ_B12
K33	VSS
L1	SBA4 (SBA4#)
L2	VCCAGP
L3	SB_STB (SB_STBF)
L4	SBA5 (SBA5#)
L5	VSS
L6	SBA7 (SBA7#)
L7	SBA6 (SBA6#)
L8	VCCAGP
L9	Reserved
L10	VSS
L11	VTT
L12	VSS
L13	VTT
L14	VSS
L15	VTT
L16	VSS
L17	VTT
L18	VSS

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
L19	VTT
L20	VSS
L21	VTT
L22	VSS
L23	VCCDDR
L24	DDR_STRAP
L25	DQ_A0
L26	VSS
L27	DQ_A3
L28	CKE_B0
L29	VSS
L30	VSS
L31	DQ_B9
L32	VSS
L33	DQ_B8
M1	VSS
M2	GAD30
M3	GAD29
M4	VCCAGP
M5	GAD26
M6	GAD31
M7	VSS
M8	DBI_LO
M9	PIPE# (DBI_HI)
M10	VCCAGP
M11	VSS
M23	VSS
M24	VCCDDR
M25	DQ_A4
M26	DQ_A7
M27	VSS
M28	VCCDDR
M29	DQ_A13
M30	DQS_B1
M31	VSS
M32	DQS_B10
M33	DQ_B13
N1	GAD27

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
N2	GAD28
N3	VSS
N4	GAD24
N5	PSWNG_AGP0
N6	VCCAGP
N7	GAD22
N8	GAD19
N9	VSS
N10	VSS
N11	VCCAGP
N23	VCCDDR
N24	VSS
N25	CKE_B2
N26	CKE_A2
N27	VSS
N28	DQS_A10
N29	DQS_A1
N30	VSS
N31	DQ_B15
N32	DQ_B14
N33	VSS
P1	GAD25
P2	VSS
P3	AD_STB1 (AD_STBF1)
P4	PRCOMP_AGP1
P5	VSS
P6	GAD20
P7	GAD18
P8	VSS
P9	GAD17
P10	VCCAGP
P11	VSS
P14	VCC[3]
P15	VSS
P16	VCCAFSB
P17	VSS
P18	VCC[3]
P19	VSS

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
P20	VCC[3]
P23	VSS
P24	VCCDDR
P25	DQ_A8
P26	VCCDDR
P27	DQ_A14
P28	DQ_A15
P29	VSS
P30	DQ_B11
P31	DQ_B10
P32	VCCDDR
P33	MA_A12
R1	VSS
R2	GC/BE3# (GC#/BE3)
R3	AD_STB1# (AD_STBS1)
R4	VSS
R5	TESTSIG1*
R6	TESTSIG2*
R7	VSS
R8	GAD15
R9	GAD16
R10	VSS
R11	VCCAGP
R14	VSS
R15	VCC[3]
R16	VSS
R17	VCC[3]
R18	VSS
R19	VCC[3]
R20	VSS
R23	VCCDDR
R24	VSS
R25	DQ_A9
R26	DQ_A10
R27	DQ_A11
R28	VSS
R29	MA_B12

Table 7-2. MCH Ball List by Ball Number

Table 7-2. MCH Ball List by Ball Number
Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
R30	MA_A9
R31	VSS
R32	MA_A11
R33	MA_B11
T1	GAD23
T2	PREF_AGP1
T3	VSS
T4	GAD21
T5	PRCOMP_AGP0
T6	VSS
T7	GAD13
T8	GC/BE2# (GC#/BE2)
T9	VSS
T10	VCCAGP
T11	VSS
T14	VCC[3]
T15	VSS
T16	VCC[3]
T17	VSS
T18	VCC[3]
T19	VSS
T20	VCC[3]
T23	VSS
T24	VCCDDR
T25	DQ_A12
T26	VSS
T27	VSS
T28	MA_B7
T29	MA_A7
T30	VCCDDR
T31	MA_B9
T32	DQ_B20
T33	VSS
U1	GC/BE0# (GC#/BE0)
U2	VCCAGP
U3	PREF_AGP0
U4	PSWNG_AGP1
U5	VSS
U6	GAD11
U7	GAD12
U8	VCCAGP
U9	GC/BE1# (GC#/BE1)
U10	VSS
U11	VCCAGP
U14	VSS
U15	VCCAHI
U16	VSS
U17	VCC[3]
U18	VSS
U19	VCC[3]
U20	VSS
U23	VCCDDR
U24	VSS
U25	VSS
U26	VSS
U27	DQ_A17
U28	DQ_A21
U29	VSS
U30	DQ_B17
U31	DQ_B21
U32	VSS
U33	DQ_B16
V1	VSS
V2	AD_STB0# (AD_STBS0)
V3	AD_STB0 (AD_STBF0)
V4	VCCAGP
V5	GAD9
V6	GAD10
V7	VSS
V8	GAD14
V9	SERR# (SERR)
V10	VCCAGP
V11	VSS
V14	VCC[3]
V15	VSS
V16	VCC[3]
V17	VSS
V18	VCC[3]
V19	VSS
V20	VCC[3]
V23	VSS
V24	VCCDDR
V25	DQ_A20
V26	DQ_A16
V27	DQS_A11
V28	VCCDDR
V29	DQS_A2
V30	DQ_B22
V31	VSS
V32	DQS_B2
V33	DQS_B11
W1	GAD7
W2	GAD5
W3	VSS
W4	GAD4
W5	GAD6
W6	VCCAGP
W7	GIRDY# (GIRDY)
W8	GAD8
W9	VSS
W10	VSS
W11	Reserved
W14	VSS
W15	VCC[3]
W16	VSS
W17	VCC[3]
W18	VSS
W19	VCC[3]
W20	VSS
W23	VCCDDR
W24	VSS
W25	DQ_A18
W26	DQ_A22

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
W27	VSS
W28	DQ_A23
W29	DQ_A19
W30	VSS
W31	DQ_B23
W32	DQ_B18
W33	VSS
Y1	GAD3
Y2	VSS
Y3	GAD2
Y4	GAD1
Y5	VSS
Y6	GFRAME# (GFRAME)
Y7	Reserved
Y8	VSS
Y9	GCLKIN
Y10	VCC[3]
Y11	Reserved
Y14	VCC[3]
Y15	VSS
Y16	VCC[3]
Y17	VSS
Y18	VCC[3]
Y19	VSS
Y20	VCC[3]
Y23	VSS
Y24	VCCDDR
Y25	VSS
Y26	VCCDDR
Y27	MA_A8
Y28	MA_B8
Y29	VSS
Y30	MA_A5
Y31	MA_B5
Y32	VCCDDR
Y33	DQ_B19
AA1	VSS
AA2	GDEVSEL# (GDEVSEL)
AA3	GAD0
AA4	VSS
AA5	GPAR
AA6	HI_A11
AA7	VSS
AA8	HI_A5
AA9	HI_A7
AA10	VSS
AA11	VCC[3]
AA23	VCCDDR
AA24	VSS
AA25	DQ_A24
AA26	DQ_A28
AA27	VSS
AA28	VSS
AA29	MA_B4
AA30	MA_A4
AA31	VSS
AA32	MA_A6
AA33	MA_B6
AB01	GSTOP# (GSTOP)
AB02	GTRDY# (GTRDY)
AB03	VSS
AB04	HI_A0
AB05	PSTRBS_0
AB06	VCC[3]
AB07	HI_A8
AB08	HI_A6
AB09	VSS
AB10	VCC[3]
AB11	VSS
AB23	VSS
AB24	VCCDDR
AB25	DQ_A25
AB26	DQ_A29
AB27	VSS
AB28	DQS_A12
AB29	DQS_A3
AB30	VCCDDR
AB31	DQ_B28
AB32	DQ_B29
AB33	VSS
AC1	PRCOMP_A
AC2	VCC[3]
AC3	HI_A1
AC4	HI_A3
AC5	VSS
AC6	HI_A10
AC7	HI_A4
AC8	VSS
AC9	HI_B2
AC10	VSS
AC11	VCC[3]
AC12	VSS
AC13	VCCDDR
AC14	VSS
AC15	VCCDDR
AC16	VSS
AC17	VCCDDR
AC18	VSS
AC19	VCCDDR
AC20	VSS
AC21	VCCDDR
AC22	VSS
AC23	VCCDDR
AC24	MA_A3
AC25	CMDCLK_B3
AC26	VSS
AC27	DQ_A30
AC28	DQ_A26
AC29	VSS
AC30	DQS_B3
AC31	DQ_B25
AC32	VSS

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
AC33	DQ_B24
AD1	VSS
AD2	PSWNG_A
AD3	HI_A2
AD4	VCC[3]
AD5	PSTRBF_0
AD6	HI_B3
AD7	VSS
AD8	HI_B0
AD9	HI_B8
AD10	VCC[3]
AD11	VSS
AD12	VCCDDR
AD13	VSS
AD14	VCCDDR
AD15	VSS
AD16	VCCDDR
AD17	VSS
AD18	VCCDDR
AD19	VSS
AD20	VCCDDR
AD21	VSS
AD22	VCCDDR
AD23	VSS
AD24	VCCDDR
AD25	CMDCLK_B3#
AD26	MA_A2
AD27	MA_B3
AD28	VCCDDR
AD29	DQ_A27
AD30	DQ_B26
AD31	VSS
AD32	DQ_B30
AD33	DQS_B12
AE1	PREF_A
AE2	HI_A9
AE3	VSS
AE4	PSTRBF_B

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
AE5	HI_B5
AE6	VCC[3]
AE7	HI_B4
AE8	PSTRBS_B
AE9	VSS
AE10	CS_B2#
AE11	DQ_A59
AE12	DQ_A63
AE13	CAS_B#
AE14	DQ_A51
AE15	DQ_A48
AE16	BA_A0
AE17	DQ_A47
AE18	DQ_A40
AE19	CMDCLK_A3#
AE20	DQ_A33
AE21	DQ_A32
AE22	CMDCLK_A1
AE23	CB_A3
AE24	CB_A5
AE25	VSS
AE26	CB_A4
AE27	VSS
AE28	MA_B2
AE29	DQ_A31
AE30	VSS
AE31	DQ_B31
AE32	DQ_B27
AE33	VSS
AF1	HI_B7
AF2	VSS
AF3	HI_B6
AF4	HI_B16
AF5	VSS
AF6	HI_B20
AF7	PRCOMP_B
AF8	VSS
AF9	CS_A3#

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
AF10	CS_A2#
AF11	VCCDDR
AF12	DQ_A58
AF13	CS_A0#
AF14	VSS
AF15	DQ_A49
AF16	BA_B0
AF17	VCCDDR
AF18	DQ_A44
AF19	CMDCLK_A3
AF20	VSS
AF21	DQS_A4
AF22	CMDCLK_A1#
AF23	VCCDDR
AF24	CMDCLK_A0
AF25	CB_A7
AF26	CB_A1
AF27	CB_A0
AF28	VSS
AF29	VSS
AF30	CMDCLK_B2#
AF31	CMDCLK_B2
AF32	VCCDDR
AF33	DVREF_B
AG1	VSS
AG2	HI_B1
AG3	HI_B18
AG4	VCC[3]
AG5	HI_B17
AG6	PREF_B
AG7	VSS
AG8	CS_A5#/CMDCLK_A6
AG9	CS_A4#/CMDCLK_A6#
AG10	VSS
AG11	DQ_A62
AG12	DQ_A56
AG13	VSS
AG14	DQ_A55

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
AG15	DQ_A50
AG16	VSS
AG17	DQ_A46
AG18	DQS_A5
AG19	VSS
AG20	BA_B1
AG21	DQ_A35
AG22	VSS
AG23	DQS_A13
AG24	CMDCLK_A0#
AG25	VSS
AG26	CB_A6
AG27	CB_A2
AG28	VSS
AG29	MA_B1
AG30	MA_A1
AG31	VSS
AG32	DVREF_A
AG33	ODTCOMP
AH1	HI_B10
AH2	HI_B9
AH3	VSS
AH4	PUSTRBF_B
AH5	PUSTRBS_B
AH6	VSS
AH7	CS_B5#/CMDCLK_B6
AH8	CS_B4#/CMDCLK_B6#
AH9	VCCDDR
AH10	DQ_A57
AH11	DQ_A60
AH12	VSS
AH13	CS_B0#
AH14	DQS_A15
AH15	VCCDDR
AH16	VSS
AH17	DQ_A43
AH18	VSS
AH19	DQS_A14

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
AH20	BA_A1
AH21	VCCDDR
AH22	DQ_A38
AH23	DQ_A34
AH24	VSS
AH25	MA_A0
AH26	VSS
AH27	VCCDDR
AH28	DQS_A8
AH29	DQS_A17
AH30	VCCDDR
AH31	RCVENOUT_A#
AH32	RCVENOUT_B#
AH33	VSS
AJ1	HI_B11
AJ2	VCC[3]
AJ3	HI_B13
AJ4	PSWING_B
AJ5	VSS
AJ6	CMDCLK_A7
AJ7	CMDCLK_A7#
AJ8	VSS
AJ9	DQS_A16
AJ10	DQ_A61
AJ11	VSS
AJ12	CS_A1#
AJ13	DQ_A54
AJ14	VSS
AJ15	DQS_A6
AJ16	VSS
AJ17	VSS
AJ18	DQ_A42
AJ19	DQ_A41
AJ20	VSS
AJ21	CMDCLK_A2#
AJ22	DQ_A39
AJ23	VSS
AJ24	DQ_A37

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
AJ25	DQ_A36
AJ26	VSS
AJ27	CMDCLK_B1
AJ28	CMDCLK_B1#
AJ29	VSS
AJ30	CB_B4
AJ31	DRCOMPVREF_V
AJ32	VSS
AJ33	DRCOMP_V
AK1	VSS
AK2	HI_B12
AK3	HI_B15
AK4	VSS
AK5	CMDCLK_B7
AK6	CMDCLK_B7#
AK7	VCCDDR
AK8	DQS_A7
AK9	CS_B3#
AK10	VSS
AK11	CS_B1#
AK12	DQS_B15
AK13	VCCDDR
AK14	DQ_A53
AK15	DQ_A52
AK16	VSS
AK17	DQ_B43
AK18	DQS_B5
AK19	VCCDDR
AK20	DQ_A45
AK21	CMDCLK_A2
AK22	VSS
AK23	DQ_B39
AK24	DQ_B38
AK25	VCCDDR
AK26	DQ_B37
AK27	CB_B7
AK28	VSS
AK29	DQS_B8

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
AK30	CB_B5
AK31	VCCDDR
AK32	DRCOMPVREF_H
AK33	DRCOMP_H
AL1	HI_B14
AL2	HI_B21
AL3	VSS
AL4	DQ_B62
AL5	DQS_B7
AL6	VSS
AL7	DQ_B57
AL8	DQ_B60
AL9	VSS
AL10	Reserved
AL11	DQ_B50
AL12	VSS
AL13	DQ_B48
AL14	DQ_B52
AL15	VSS
AL16	RAS_A#
AL17	DQ_B47
AL18	VSS
AL19	DQS_B14
AL20	DQ_B45
AL21	VSS
AL22	MA_B10
AL23	DQ_B35
AL24	VSS
AL25	DQS_B13
AL26	DQ_B32
AL27	VSS
AL28	CB_B6
AL29	CB_B2
AL30	VSS
AL31	VSS
AL32	VCCDDR
AL33	VSS
AM2	VSS

Table 7-2. MCH Ball List by Ball Number

Ball #	Signal Name
AM3	DQ_B63
AM4	DQ_B58
AM5	VCCDDR
AM6	DQ_B61
AM7	DQ_B56
AM8	VSS
AM9	MA_A13
AM10	DQ_B51
AM11	VCCDDR
AM12	DQS_B6
AM13	DQ_B49
AM14	VSS
AM15	WE_A#
AM16	RAS_B#
AM17	VCCDDR
AM18	DQ_B46
AM19	DQ_B41
AM20	VSS
AM21	VSS
AM22	MA_A10
AM23	VCCDDR
AM24	DQS_B4
AM25	DQ_B33
AM26	VSS
AM27	CMDCLK_B0#
AM28	CB_B3
AM29	VCCDDR
AM30	CB_B0
AM31	VCCDDR
AM32	VSS
AN3	DQ_B59
AN4	VSS
AN5	DQS_B16
AN6	VSS
AN7	VSS
AN8	MA_B13
AN9	DQ_B55
AN10	VSS

Table 7-2. MCH Ball List by Ball Number

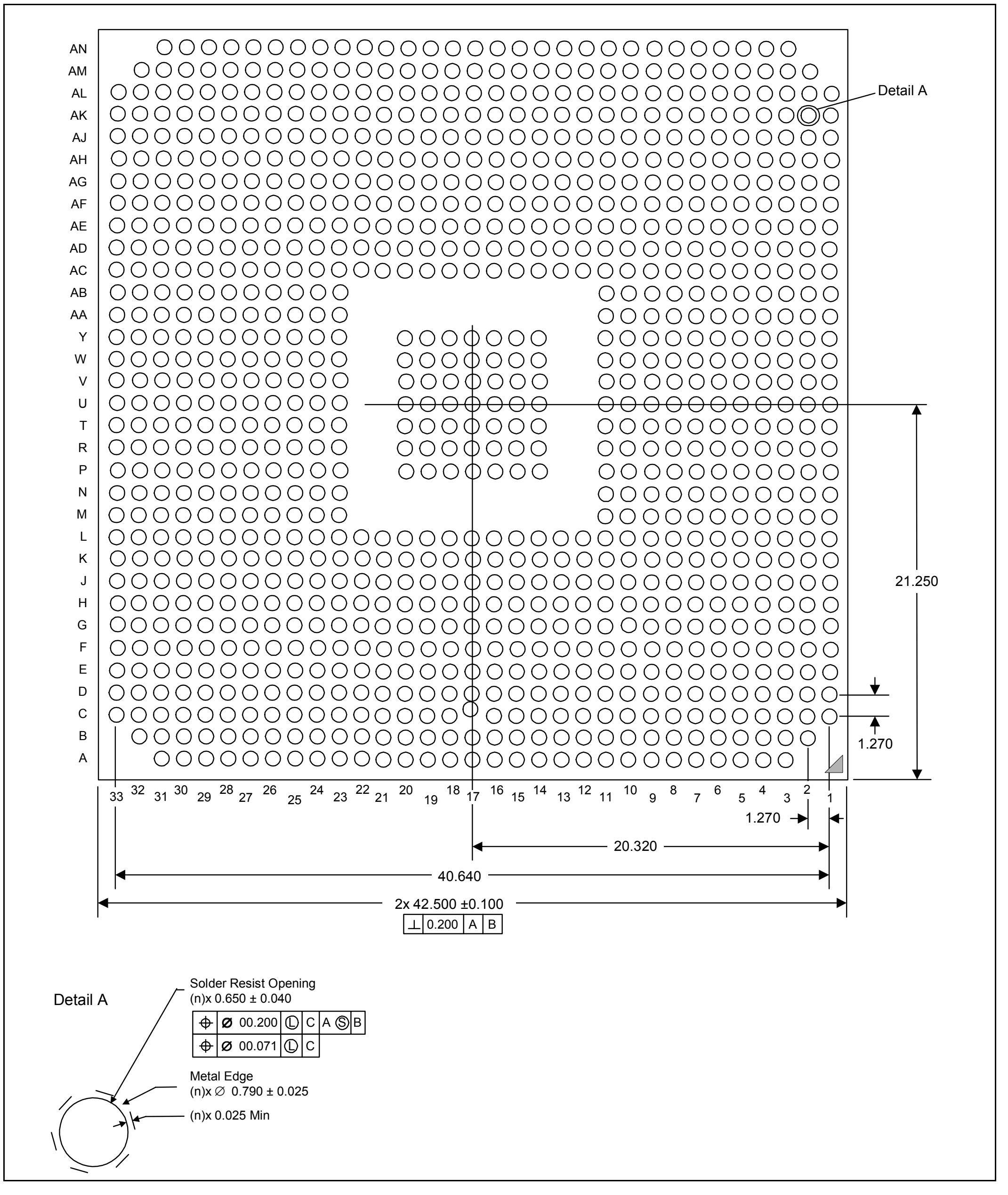
Ball #	Signal Name
AN11	DQ_B54
AN12	DQ_B53
AN13	VSS
AN14	CAS_A#
AN15	WE_B#
AN16	VSS
AN17	VSS
AN18	DQ_B42
AN19	VSS
AN20	DQ_B44
AN21	DQ_B40
AN22	VSS
AN23	MA_B0
AN24	DQ_B34
AN25	VSS
AN26	DQ_B36
AN27	CMDCLK_B0
AN28	VSS
AN29	DQS_B17
AN30	CB_B1
AN31	VSS

NOTES:
1. Signals marked with an "*" must have an accessible test point if XOR testing is implemented.
2. For AGP signals that have different names between AGP 2.0 and AGP 3.0, the name outside the parenthesis is the AGP 2.0 signal name and the name inside the parenthesis is the AGP 3.0 signal name.
3. VCC is set at 1.2 V or 1.3V depending on the part. Please refer to the E7505 Specification Update for more information

7.2 Package Specifications

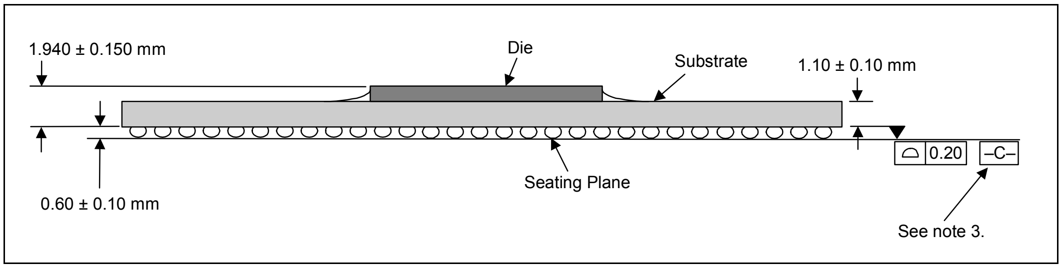
The MCH package is a 42.5 mm x 42.5 mm FCBGA with 1005 LANDS. Figure 7-4 and Figure 7-5 show the package dimensions for the MCH. For more detailed package information, refer to the *Intel® E7500/E7505 Chipset Thermal Design Guide*.

Figure 7-4. Package Dimensions (Bottom View)



NOTE:
1. All dimensions are in millimeters.
2. All dimensions and tolerances conform to ANSI Y14.5M-1982.

Figure 7-5. Package Dimensions (Top and Side Views)



NOTES:

1. All dimensions are in millimeters.
2. Substrate thickness and package overall height are thicker than standard 492-L-PBGA
3. Primary datum —C— and seating plane are defined by the spherical crowns of the solder balls.
4. All dimensions and tolerances conform to ANSI Y14.5M-1982.

7.3 Interface Trace Length Compensation

In this section, detailed information is given about the internal component package trace lengths to enable trace length compensation. Trace length compensation is required for platform design. These lengths must be considered when matching trace lengths as described in the *Intel® Xeon™ Processor and Intel® E7505 Chipset Platform Design Guide*. Note that these lengths represent the actual lengths from pad to ball.

Different length matching requirements must be followed for each platform interface. These guidelines are specified in the corresponding sections of the platform design guide. Use of the Length Matching Spreadsheet is recommended to provide lengths for major interfaces. Contact your Intel representative for information about the Length Matching Spreadsheet tool.

7.3.1 System Bus Signal Package Trace Length Data

Table 7-3 provides the MCH package trace length information for the system bus.

Table 7-3. MCH L_{PKG} Data for the System Bus

Signal	Ball No.	L_{PKG} (mils)
HADSTB0#	C6	788
HA3#	H15	358
HA4#	F11	464
HA5#	D8	691
HA6#	E9	545
HA7#	G11	446
HA8#	D7	665
HA9#	F9	545
HA10#	A4	938
HA11#	E7	670
HA12#	C5	794
HA13#	B4	885
HA14#	B3	905
HA15#	A5	914
HA16#	D5	740
HREQ0#	G10	593
HREQ1#	G13	341
HREQ2#	H13	395
HREQ3#	E10	532
HREQ4#	G14	368
HADSTB1#	H9	431
HA17#	H12	346
HA18#	J12	295
HA19#	J11	273
HA20#	E6	679
HA21#	F6	605
HA22#	H6	567
HA23#	G8	513
HA24#	H10	369
HA25#	J9	410
HA26#	F5	638
HA27#	D4	795
HA28#	J8	384
HA29#	G7	579
HA30#	H7	466
HA31#	E3	759.
HA32#	C2	891
HA33#	C3	845
HA34#	G5	613
HA35#	E4	749
HCLKINN	J16	289
HCLKINP	J17	286

Signal	Ball No.	L_{PKG} (mils)
HDSTBN0#	E27	606
HDSTBP0#	F26	517
HD0#	B31	848
HD1#	G25	777
HD2#	C29	746
HD3#	C30	781
HD4#	G26	634
HD5#	A29	852
HD6#	D29	714
HD7#	A31	921
HD8#	B30	838
HD9#	E28	626
HD10#	D28	648
HD11#	D26	608
HD12#	E25	521
HD13#	F27	536
HD14#	G23	698
HD15#	H24	588
DINV0#	H25	564
HDSTBN1#	G22	682
HDSTBP1#	H21	604
HD16#	A28	815
HD17#	B28	781
HD18#	B27	764
HD19#	C27	688
HD20#	A26	737
HD21#	C26	682
HD22#	B25	699
HD23#	A25	772
HD24#	H22	617
HD25#	D23	578
HD26#	F23	464
HD27#	C24	639
HD28#	D22	513
HD29#	E24	548
HD30#	E22	498
HD31#	G20	592
DINV1#	D25	599

Table 7-3. MCH L_{PKG} Data for the System Bus (Continued)

Signal	Ball No.	L_{PKG} (mils)
HDSTBN2#	B21	682
HDSTBP2#	C20	597
HD32#	A23	727
HD33#	B22	678
HD34#	C23	639
HD35#	D20	450
HD36#	B24	738
HD37#	C21	598
HD38#	D19	524.
HD39#	A20	700
HD40#	B18	623
HD41#	B19	604
HD42#	E19	475
HD43#	C18	533
HD44#	H19	376
HD45#	E18	503
HD46#	H18	370
HD47#	G19	350
DINV2#	A19	710

Signal	Ball No.	L_{PKG} (mils)
HDSTBN3#	C17	563
HDSTBP3#	E16	453
HD48#	F17	670
HD49#	F18	692
HD50#	G17	628
HD51#	A17	668
HD52#	D17	505
HD53#	D16	539
HD54#	A16	691
HD55#	B16	602
HD56#	C14	630
HD57#	D14	539
HD58#	B13	702
HD59#	C12	699
HD60#	B12	703
HD61#	A14	830
HD62#	B15	628
HD63#	A13	760
DINV3#	C15	611

7.3.2 DDR Channel A Signal Package Trace Length Data

Table 7-4 provides the MCH package trace length information for channel A of the DDR memory interface.

Table 7-4. MCH L_{PKG} Data for DDR Channel A

Signal	Ball No.	L_{PKG} (mils)
DQS_A0	K26	631
DQS_A9	H28	622
DQ_A0	L25	627
DQ_A1	J27	651
DQ_A2	J29	667
DQ_A3	L27	510
DQ_A4	M25	493
DQ_A5	G29	716
DQ_A6	K28	584
DQ_A7	M26	548
DQS_A1	N29	552
DQS_A10	N28	497
DQ_A8	P25	628
DQ_A9	R25	457
DQ_A10	R26	459
DQ_A11	R27	473
DQ_A12	T25	452
DQ_A13	M29	583
DQ_A14	P27	455
DQ_A15	P28	464
DQS_A4	AF21	578
DQS_A13	AG23	570
DQ_A32	AE21	629
DQ_A33	AE20	516
DQ_A34	AH23	648
DQ_A35	AG21	579
DQ_A36	AJ25	709
DQ_A37	AJ24	661
DQ_A38	AH22	602
DQ_A39	AJ22	516

Signal	Ball No.	L_{PKG} (mils)
DQS_A2	V29	549
DQS_A11	V27	482
DQ_A16	V26	538
DQ_A17	U27	742
DQ_A18	W25	496
DQ_A19	W29	507
DQ_A20	V25	484
DQ_A21	U28	607
DQ_A22	W26	486
DQ_A23	W28	530
DQS_A3	AB29	522
DQS_A12	AB28	601
DQ_A24	AA25	503
DQ_A25	AB25	457
DQ_A26	AC28	487
DQ_A27	AD29	568
DQ_A28	AA26	491
DQ_A29	AB26	549
DQ_A30	AC27	508
DQ_A31	AE29	706
DQS_A7	AK8	648
DQS_A16	AJ9	594
DQ_A56	AG12	491
DQ_A57	AH10	494
DQ_A58	AF12	511
DQ_A59	AE11	485
DQ_A60	AH11	473
DQ_A61	AJ10	560
DQ_A62	AG11	609
DQ_A63	AE12	504

Table 7-4. MCH L_{PKG} Data for DDR Channel A (Continued)

Signal	Ball No.	L_{PKG} (mils)
DQS_A5	AG18	517
DQS_A14	AH19	556
DQ_A40	AE18	475
DQ_A41	AJ19	635
DQ_A42	AJ18	665
DQ_A43	AH17	481
DQ_A44	AF18	486
DQ_A45	AK20	588
DQ_A46	AG17	585
DQ_A47	AE17	438

Signal	Ball No.	L_{PKG} (mils)
DQS_A6	AJ15	468
DQS_A15	AH14	567
DQ_A48	AE15	481
DQ_A49	AF15	489
DQ_A50	AG15	585
DQ_A51	AE14	412
DQ_A52	AK15	524
DQ_A53	AK14	548
DQ_A54	AJ13	601
DQ_A55	AG14	393

Signal	Ball No.	L_{PKG} (mils)
CS_A0#	AF13	292
CS_A1#	AJ12	570
CS_A2#	AF10	406
CS_A3#	AF9	417
CS_A4#	AG9	482
CS_A5#	AG8	484
CS_A6#	AJ7	654
CS_A7#	AJ6	655

Signal	Ball No.	L_{PKG} (mils)
CKE_A0	K29	679
CKE_A1	J33	894
CKE_A2	N26	530
CKE_A3	K31	683

Signal	Ball No.	L_{PKG} (mils)
MA_A0	AH25	591
MA_A1	AG30	777
MA_A2	AD26	354
MA_A3	AC24	374
MA_A4	AA30	520
MA_A5	Y30	504
MA_A6	AA32	666
MA_A7	T29	519
MA_A8	Y27	407
MA_A9	R30	523
MA_A10	AM22	706
MA_A11	R32	668
MA_A12	P33	766
MA_A13	AM9	744

Signal	Ball No.	L_{PKG} (mils)
DQS_A8	AH28	657
DQS_A17	AH29	696
CB_A0	AF27	721
CB_A1	AF26	636
CB_A2	AG27	711
CB_A3	AE23	555
CB_A4	AE26	535
CB_A5	AE24	533
CB_A6	AG26	541
CB_A7	AF25	558

Signal	Ball No.	L_{PKG} (mils)
CMDCLK_A0	AF24	508
CMDCLK_A0#	AG24	508
CMDCLK_A1	AE22	466
CMDCLK_A1#	AF22	467
CMDCLK_A2	AK21	548
CMDCLK_A2#	AJ21	553
CMDCLK_A3	AF19	356
CMDCLK_A3#	AE19	357

Signal	Ball No.	L_{PKG} (mils)
BA_A0	AE16	383
BA_A1	AH20	567

Signal	Ball No.	L_{PKG} (mils)
RAS_A#	AL16	537
CAS_A#	AN14	744
WE_A#	AM15	621

7.3.3 DDR Channel B Signal Package Trace Length Data

Table 7-5 provides the MCH package trace length information for channel B of the DDR memory interface.

Table 7-5. MCH L_{PKG} Data for DDR Channel B

Signal	Ball No.	L_{PKG} (mils)	Signal	Ball No.	L_{PKG} (mils)
DQS_B0	G31	860	DQS_B3	AC30	730
DQS_B9	F33	938	DQS_B12	AD33	741
DQ_B0	E31	801	DQ_B24	AC33	747
DQ_B1	F32	813	DQ_B25	AC31	619
DQ_B2	G32	868	DQ_B26	AD30	696
DQ_B3	H33	974	DQ_B27	AE32	878
DQ_B4	E33	978	DQ_B28	AB31	675
DQ_B5	F30	787	DQ_B29	AB32	750
DQ_B6	H30	900	DQ_B30	AD32	662
DQ_B7	H31	817	DQ_B31	AE31	646
DQS_B1	M30	861	DQS_B4	AM24	730
DQS_B10	M32	791	DQS_B13	AL25	830
DQ_B8	L33	781	DQ_B32	AL26	758
DQ_B9	L31	806	DQ_B33	AM25	809
DQ_B10	P31	675	DQ_B34	AN24	922
DQ_B11	P30	680	DQ_B35	AL23	802
DQ_B12	K32	854	DQ_B36	AN26	832
DQ_B13	M33	759	DQ_B37	AK26	840
DQ_B14	N32	777	DQ_B38	AK24	899
DQ_B15	N31	723	DQ_B39	AK23	813
DQS_B2	V32	787	DQS_B5	AK18	615
DQS_B11	V33	709	DQS_B14	AL19	666
DQ_B16	U33	704	DQ_B40	AN21	729
DQ_B17	U30	669	DQ_B41	AM19	667
DQ_B18	W32	865	DQ_B42	AN18	710
DQ_B19	Y33	712	DQ_B43	AK17	483
DQ_B20	T32	675	DQ_B44	AN20	728
DQ_B21	U31	645	DQ_B45	AL20	664
DQ_B22	V30	729	DQ_B46	AM18	616
DQ_B23	W31	692	DQ_B47	AL17	570

Table 7-5. MCH L_{PKG} Data for DDR Channel B (Continued)

Signal	Ball No.	L_{PKG} (mils)
DQS_B6	AM12	749
DQS_B15	AK12	781
DQ_B48	AL13	606
DQ_B49	AM13	700
DQ_B50	AL11	641
DQ_B51	AM10	729
DQ_B52	AL14	661
DQ_B53	AN12	845
DQ_B54	AN11	758
DQ_B55	AN9	753

DQS_B7	AL5	799
DQS_B16	AN5	948
DQ_B56	AM7	767
DQ_B57	AL7	707
DQ_B58	AM4	884
DQ_B59	AN3	944
DQ_B60	AL8	880
DQ_B61	AM6	775
DQ_B62	AL4	815
DQ_B63	AM3	873

CS_B0#	AH13	416
CS_B1#	AK11	565
CS_B2#	AE10	319
CS_B3#	AK9	707
CS_B4#	AH8	569
CS_B5#	AH7	568
CS_B6#	AK6	714
CS_B7#	AK5	715
CKE_B0	L28	601
CKE_B1	J32	817
CKE_B2	N25	424
CKE_B3	J30	676

MA_B0	AN23	1001
MA_B1	AG29	715
MA_B2	AE28	513
MA_B3	AD27	405
MA_B4	AA29	487
MA_B5	Y31	573
MA_B6	AA33	737
MA_B7	T28	512
MA_B8	Y28	463
MA_B9	T31	625
MA_B10	AL22	785
MA_B11	R33	735
MA_B12	R29	527
MA_B13	AN8	814

Signal	Ball No.	L_{PKG} (mils)
DQS_B8	AK29	917
DQS_B17	AN29	977
CB_B0	AM30	953
CB_B1	AN30	988
CB_B2	AL29	900
CB_B3	AM28	986
CB_B4	AJ30	766
CB_B5	AK30	792
CB_B6	AL28	797
CB_B7	AK27	798

CMDCLK_B0	AN27	853
CMDCLK_B0#	AM27	853
CMDCLK_B1	AJ27	787
CMDCLK_B1#	AJ28	789
CMDCLK_B2	AF31	914
CMDCLK_B2#	AF30	914
CMDCLK_B3	AC25	368
CMDCLK_B3#	AD25	368

BA_B0	AF16	453
BA_B1	AG20	504

RAS_B#	AM16	571
CAS_B#	AE13	285
WE_B#	AN15	682

7.3.4 Hub Interface_A Signal Package Trace Length Data

Table 7-6 provides the MCH package trace length information for Hub Interface_A.

Table 7-6. MCH L_{PKG} Data for Hub Interface_A

Signal	Ball No.	L_{PKG} (mils)
PSTRBF_0	AD5	627
PSTRBS_0	AB5	626
HI_A0	AB4	607
HI_A1	AC3	666
HI_A2	AD3	746
HI_A3	AC4	624
HI_A4	AC7	507
HI_A5	AA8	448
HI_A6	AB8	419
HI_A7	AA9	468
HI_A8	AB7	508
HI_A9	AE2	802
HI_A10	AC6	660
HI_A11	AA6	450

7.3.5 Hub Interface_B Signal Package Trace Length Data

Table 7-7 provides the MCH package trace length information for Hub Interface_B.

Table 7-7. MCH L_{PKG} Data for Hub Interface_B

Signal	Ball No.	L_{PKG} (mils)
PSTRBF_B	AE4	676
PSTRBS_B	AE8	676
PUSTRBF_B	AH4	728
PUSTRBS_B	AH5	716
HI_B0	AD8	578
HI_B1	AG2	853
HI_B2	AC9	559
HI_B3	AD6	586
HI_B4	AE7	563
HI_B5	AE5	673
HI_B6	AF3	742
HI_B7	AF1	878
HI_B8	AD9	603
HI_B9	AH2	861
HI_B10	AH1	926
HI_B11	AJ1	915
HI_B12	AK2	893
HI_B13	AJ3	887
HI_B14	AL1	956
HI_B15	AK3	802
HI_B16	AF4	676
HI_B17	AG5	793
HI_B18	AG3	759
HI_B20	AF6	610
HI_B21	AL2	918

7.3.6 AGP Signal Package Trace Length Data

Table 7-8 provides the MCH package trace length information for AGP. Note that only the AGP 2.0 signal names are shown.

Table 7-8. MCH L_{PKG} Data for AGP

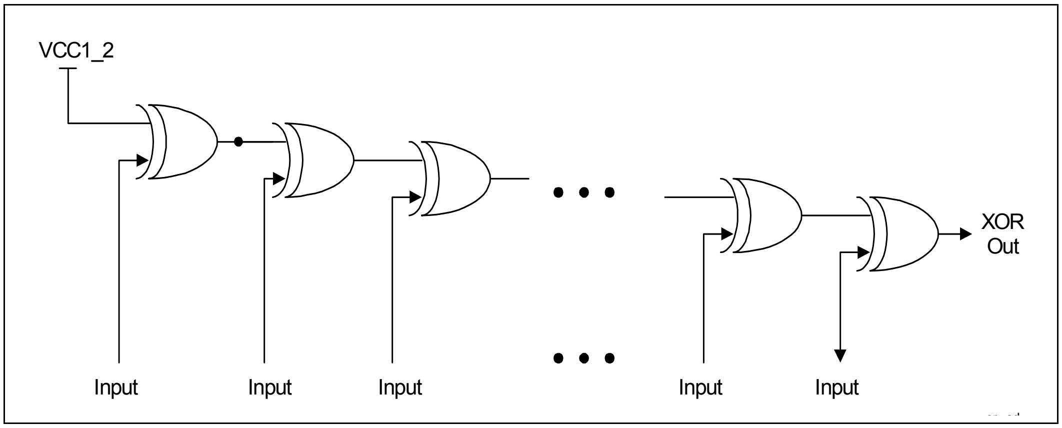
Signal	Ball No.	L_{PKG} (mils)
AD_STB0	V3	653
AD_STB0#	V2	647
GAD0	AA3	629
GAD1	Y4	578
GAD2	Y3	596
GAD3	Y1	769
GAD4	W4	550
GAD5	W2	706
GAD6	W5	829
GAD7	W1	708
GAD8	W8	568
GAD9	V5	455
GAD10	V6	510
GAD11	U6	430
GAD12	U7	434
GAD13	T7	455
GAD14	V8	475
GAD15	R8	448
GC/BE0#	U1	697
GC/BE1#	U9	455
AD_STB1	P3	668
AD_STB1#	R3	673
PIPE# (DBI_HI)	M9	475
DBI_LO	M8	445
GAD16	R9	476
GAD17	P9	481
GAD18	P7	375
GAD19	N8	391
GAD20	P6	455
GAD21	T4	602
GAD22	N7	397
GAD23	T1	715
GAD24	N4	526
GAD25	P1	760
GAD26	M5	517
GAD27	N1	735
GAD28	N2	644
GAD29	M3	612
GAD30	M2	682
GAD31	M6	462
GC/BE2#	T8	468
GC/BE3#	R2	682

Signal	Ball No.	L_{PKG} (mils)
SB_STB	L3	701
SB_STB#	K2	702
SBA0	K7	422
SBA1	J2	703
SBA2	K4	587
SBA3	K1	803
SBA4	L1	721
SBA5	L4	552
SBA6	L7	477
SBA7	L6	452
GDEVSEL#	AA2	665
GFRAME#	Y6	424
GGNT#	K8	383
GIRDY#	W7	404
GPAR	AA5	539
GREQ#	J6	509
GSTOP#	AB1	745
GTRDY#	AB2	675
RBF#	J3	677
SERR	V9	366
ST0	H1	788
ST1	H3	693
ST2	J5	538
WBF#	K5	540

Testability 8

For Automated Test Equipment (ATE), the MCH supports XOR-tree testing. XOR-tree testing allows board-level interconnections to be tested. An XOR-Tree is a chain of XOR gates, with each having one input pin or one bi-directional pin (used as an input pin only) connected to it.

Figure 8-1. XOR Test Tree Chain



8.1 XOR Test Mode Initialization

XOR mode can be entered by driving the XORMODE# pin (ball G1) low. Clocks may be inactive during this test mode. This mode is intended to be asynchronous.

- Drive RSTIN#, XORMODE#, PWRGD High.
- Drive RSTIN# (reset) pin Low and then High again. (This resets the part)
- Then drive the XORMODE# pin Low. (This puts the part into XOR mode)
- Drive all the PADs in a chain to 1, and observe the chain output at the assigned **HI_A[x]** (visibility) pin.
- Drive one of the PADs in the same chain to 0, and observe the chain output toggle.
- Similarly test all XOR chains while cycling through all PAD inputs.

8.1.1 XOR Chains

The following pages contain the XOR Chain information.

Note: To keep the XOR Chain contiguous, the RESERVED signals must have an accessible test point if XOR Testing is to be implemented.

Table 8-1. XOR Chain 0

	Ball Name	Ball #
1	RCVENOUT_A#	AH31
2	MA_A2	AD26
3	MA_A3	AC24
4	MA_A0	AH25
5	MA_A1	AG30
6	CB_A4	AE26
7	CB_A5	AE24
8	DQS_A17	AH29
9	DQS_A8	AH28
10	CB_A6	AG26
11	CB_A7	AF25
12	CB_A0	AF27
13	CB_A1	AF26
14	CB_A2	AG27
15	CB_A3	AE23
16	CMDCLK_A1#	AF22
17	CMDCLK_A1	AE22
18	CMDCLK_A0#	AG24
19	CMDCLK_A0	AF24
20	DQ_A38	AH22
21	DQ_A39	AJ22
22	DQS_A13	AG23
23	DQS_A4	AF21
24	DQ_A37	AJ24
25	DQ_A36	AJ25
26	DQ_A34	AH23
27	DQ_A33	AE20
28	DQ_A32	AE21
29	DQ_A35	AG21
30	MA_A10	AM22
31	CMDCLK_A2#	AJ21
32	CMDCLK_A2	AK21
33	CMDCLK_A3	AF19
34	CMDCLK_A3#	AE19
35	BA_A1	AH20
36	DQ_A44	AF18
37	DQ_A45	AK20
38	DQS_A14	AH19
39	DQS_A5	AG18
40	DQ_A47	AE17
41	DQ_A46	AG17
42	DQ_A41	AJ19
43	DQ_A42	AJ18
44	DQ_A43	AH17
45	DQ_A40	AE18
46	CAS_A#	AN14
47	RAS_A#	AL16
48	BA_A0	AE16
49	WE_A#	AM15
50	DQ_A53	AK14
51	DQ_A52	AK15
52	DQS_A15	AH14
53	DQS_A6	AJ15
54	DQ_A55	AG14
55	DQ_A54	AJ13
56	DQ_A49	AF15
57	DQ_A50	AG15
58	DQ_A51	AE14
59	DQ_A48	AE15
60	MA_A13	AM9
61	CS_A0#	AF13
62	CS_A1#	AJ12
63	DQ_A61	AJ10
64	DQ_A60	AH11
65	DQS_A16	AJ9
66	DQS_A7	AK8
67	DQ_A62	AG11
68	DQ_A63	AE12
69	DQ_A57	AH10
70	DQ_A58	AF12
71	DQ_A59	AE11
72	DQ_A56	AG12
73	CMDCLK_A7#	AJ7
74	CMDCLK_A7	AJ6
75	CS_A3#	AF9
76	CS_A4#/CMDCLK_A6#	AG9
77	CS_A5#/CMDCLK_A6	AG8
78	CS_A2#	AF10
	HI_A0	**AB4**

Table 8-2. XOR Chain 1

	Ball Name	Ball #
1	RCVENOUT_B#	AH32
2	MA_B2	AE28
3	MA_B3	AD27
4	MA_B1	AG29
5	CMDCLK_B3#	AD25
6	CMDCLK_B3	AC25
7	CMDCLK_B2	AF31
8	CMDCLK_B2#	AF30
9	CB_B0	AM30
10	CB_B1	AN30
11	CB_B2	AL29
12	CB_B3	AM28
13	DQS_B8	AK29
14	CB_B4	AJ30
15	CB_B5	AK30
16	CB_B6	AL28
17	CB_B7	AK27
18	DQS_B17	AN29
19	CMDCLK_B0	AN27
20	CMDCLK_B0#	AM27
21	CMDCLK_B1	AJ27
22	CMDCLK_B1#	AJ28
23	DQ_B32	AL26
24	DQ_B33	AM25
25	DQ_B34	AN24
26	DQ_B35	AL23
27	DQS_B4	AM24
28	DQ_B37	AK26
29	DQ_B36	AN26
30	DQ_B39	AK23
31	DQ_B38	AK24
32	DQS_B13	AL25
33	MA_B10	AL22
34	BA_B1	AG20
35	DQ_B40	AN21
36	DQ_B41	AM19
37	DQ_B42	AN18
38	DQ_B43	AK17
39	DQS_B5	AK18
40	DQ_B45	AL20
41	DQ_B44	AN20
42	DQ_B46	AM18
43	DQ_B47	AL17
44	DQS_B14	AL19
45	MA_B0	AN23
46	RAS_B#	AM16
47	BA_B0	AF16
48	WE_B#	AN15
49	DQ_B49	AM13
50	DQ_B48	AL13
51	DQ_B50	AL11
52	DQ_B51	AM10
53	DQS_B6	AM12
54	DQ_B52	AL14
55	DQ_B53	AN12
56	DQ_B54	AN11
57	DQ_B55	AN9
58	DQS_B15	AK12
59	MA_B13	AN8
60	CS_B0#	AH13
61	CS_B1#	AK11
62	CAS_B#	AE13
63	DQ_B56	AM7
64	DQ_B57	AL7
65	DQ_B59	AN3
66	DQ_B58	AM4
67	DQS_B7	AL5
68	DQ_B61	AM6
69	DQ_B60	AL8
70	DQ_B63	AM3
71	DQ_B62	AL4
72	DQS_B16	AN5
73	CMDCLK_B7#	AK6
74	CMDCLK_B7	AK5
75	CS_B3#	AK9
76	CS_B5#/CMDCLK_B6	AH7
77	CS_B4#/CMDCLK_B6#	AH8
78	CS_B2#	AE10
	HI_A1	**AC3**

Table 8-3. XOR Chain 2

	Ball Name	Ball #
	CMDCLK_A5	D31
2	CMDCLK_A5#	D32
3	CMDCLK_A4	K25
4	CMDCLK_A4#	J26
5	DQ_A7	M26
6	DQ_A5	G29
7	DQS_A9	H28
8	DQS_A0	K26
9	DQ_A4	M25
10	DQ_A6	K28
11	DQ_A0	L25
12	DQ_A2	J29
13	DQ_A3	L27
14	DQ_A1	J27
15	CKE_A1	J33
16	CKE_A2	N26
17	CKE_A3	K31
18	CKE_A0	K29
19	DQ_A14	P27
20	DQ_A13	M29
21	DQS_A10	N28
22	DQS_A1	N29
23	DQ_A15	P28
24	DQ_A12	T25
25	DQ_A8	P25
26	DQ_A11	R27
27	DQ_A9	R25
28	DQ_A10	R26
29	MA_A7	T29
30	MA_A9	R30
31	MA_A12	P33
32	MA_A11	R32
33	DQ_A23	W28
34	DQ_A21	U28
35	DQS_A11	V27
36	DQS_A2	V29
37	DQ_A20	V25
38	DQ_A22	W26
39	DQ_A16	V26

	Ball Name	Ball #
40	DQ_A17	U27
41	DQ_A19	W29
42	DQ_A18	W25
43	MA_A8	Y27
44	MA_A5	Y30
45	MA_A4	AA30
46	MA_A6	AA32
47	DQ_A31	AE29
48	DQ_A28	AA26
49	DQS_A12	AB28
50	DQS_A3	AB29
51	DQ_A29	AB26
52	DQ_A30	AC27
53	DQ_A24	AA25
54	DQ_A25	AB25
55	DQ_A26	AC28
56	DQ_A27	AD29
57	N/A	
58	N/A	
59	N/A	
60	N/A	
61	N/A	
62	N/A	
63	N/A	
64	N/A	
65	N/A	
66	N/A	
67	N/A	
68	N/A	
69	N/A	
70	N/A	
71	N/A	
72	N/A	
73	N/A	
74	N/A	
75	N/A	
76	N/A	
77	N/A	
78	N/A	
	HI_A2	**AD3**

Table 8-4. XOR Chain 3

	Ball Name	Ball #		Ball Name	Ball #
1	CMDCLK_B4#	G28	40	DQ_B21	U31
2	CMDCLK_B4	H27	41	DQ_B23	W31
3	CMDCLK_B5#	C33	42	DQS_B11	V33
4	CMDCLK_B5	C32	43	MA_B8	Y28
5	DQ_B0	E31	44	MA_B5	Y31
6	DQ_B1	F32	45	MA_B4	AA29
7	DQ_B2	G32	46	MA_B6	AA33
8	DQ_B3	H33	47	DQ_B24	AC33
9	DQS_B0	G31	48	DQ_B26	AD30
10	DQ_B7	H31	49	DQ_B27	AE32
11	DQ_B4	E33	50	DQ_B25	AC31
12	DQ_B5	F30	51	DQS_B3	AC30
13	DQ_B6	H30	52	DQ_B29	AB32
14	DQS_B9	F33	53	DQ_B28	AB31
15	CKE_B1	J32	54	DQ_B30	AD32
16	CKE_B2	N25	55	DQ_B31	AE31
17	CKE_B3	J30	56	DQS_B12	AD33
18	CKE_B0	L28	57	N/A	
19	DQ_B8	L33	58	N/A	
20	DQ_B9	L31	59	N/A	
21	DQ_B10	P31	60	N/A	
22	DQ_B11	P30	61	N/A	
23	DQS_B1	M30	62	N/A	
24	DQ_B12	K32	63	N/A	
25	DQ_B14	N32	64	N/A	
26	DQ_B13	M33	65	N/A	
27	DQ_B15	N31	66	N/A	
28	DQS_B10	M32	67	N/A	
29	MA_B7	T28	68	N/A	
30	MA_B12	R29	69	N/A	
31	MA_B11	R33	70	N/A	
32	MA_B9	T31	71	N/A	
33	DQ_B18	W32	72	N/A	
34	DQ_B16	U33	73	N/A	
35	DQ_B17	U30	74	N/A	
36	DQ_B19	Y33	75	N/A	
37	DQS_B2	V32	76	N/A	
38	DQ_B20	T32	77	N/A	
39	DQ_B22	V30	78	N/A	
				HI_A3	**AC4**

Table 8-5. XOR Chain 4

	Ball Name	Ball #
1	HI_B15	AL1
2	HI_B16	AL2
3	HI_B18	AK3
4	HI_B0	AK2
5	HI_B2	AH4
6	HI_B1	AH5
7	PSTRBF_B	AJ3
8	HI_B6	AF4
9	HI_B11	AF6
10	PUSTRBF_B	AJ1
11	HI_B14	AH2
12	PUSTRBS_B	AD9
13	HI_B9	AG3
14	HI_B10	AF3
15	PSTRBS_B	AH1
16	HI_B7	AE7
17	HI_B17	AE4
18	HI_B3	AE8
19	HI_B8	AD6
20	HI_B13	AD8
21	HI_B21	AE5
22	HI_B12	AG2
23	HI_B20	AF1
24	HI_B4	AG5
25	HI_B5	AC9
26	HI_A9	AE2
27	PSTRBS_0	AD5
28	PSTRBF_0	AB5
29	HI_A11	AA6
30	HI_A10	AC6
31	HI_A8	AB7
32	N/A	
33	N/A	
34	N/A	
35	N/A	
36	N/A	
37	N/A	
38	N/A	
39	N/A	
40	N/A	
41	N/A	
42	N/A	
43	N/A	
44	N/A	
45	N/A	
46	N/A	
47	N/A	
48	N/A	
49	N/A	
50	N/A	
51	N/A	
52	N/A	
53	N/A	
54	N/A	
55	N/A	
56	N/A	
57	N/A	
58	N/A	
59	N/A	
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61	N/A	
62	N/A	
63	N/A	
64	N/A	
65	N/A	
66	N/A	
67	N/A	
68	N/A	
69	N/A	
70	N/A	
71	N/A	
72	N/A	
73	N/A	
74	N/A	
75	N/A	
76	N/A	
77	N/A	
78	N/A	
	HI_A4	**AC7**

Table 8-6. XOR Chain 5

	Ball Name	Ball #
1	GFRAME# (GFRAME)	Y6
2	GPAR	AA5
3	GTRDY# (GTRDY)	AB2
4	GSTOP# (GSTOP)	AB1
5	GIRDY# (GIRDY)	W7
6	GDEVSEL# (GDEVSEL)	AA2
7	SERR# (SERR)	V9
8	GAD3	Y1
9	GAD0	AA3
10	GAD5	W2
11	GAD2	Y3
12	GAD1	Y4
13	GAD7	W1
14	GAD4	W4
15	GAD9	V5
16	AD_STB0 (AD_STBF0)	V3
17	AD_STB0# (AD_STBS0)	V2
18	GAD11	U6
19	GAD8	W8
20	GC/BE0# (GC#/BE0)	U1
21	GAD6	W5
22	GAD10	V6
23	GAD13	T7
24	GAD14	V8
25	GAD12	U7
26	TESTSIG2	R6
27	TESTSIG1	R5
28	GC/BE1# (GC#/BE1)	U9
29	GAD15	R8
30	GAD17	P9
31	GAD16	R9
32	GC/BE2# (GC#/BE2)	T8
33	GAD18	P7
34	GAD21	T4
35	GAD23	T1
36	GAD25	P1
37	GAD20	P6
38	GAD19	N8
39	GC/BE3# (GC#/BE3)	R2
40	GAD24	N4
41	AD_STB1 (AD_STBF1)	P3
42	AD_STB1# (AD_STBS1)	R3
43	GAD22	N7
44	GAD27	N1
45	DBI_LO	M8
46	GAD31	M6
47	GAD29	M3
48	GAD28	N2
49	GAD26	M5
50	GAD30	M2
51	PIPE# (DBI_HI)	M9
52	SBA6 (SBA6#)	L7
53	SBA4 (SBA4#)	L1
54	SBA7 (SBA7#)	L6
55	SB_STB (SB_STBF)	L3
56	SB_STB# (SB_STBS)	K2
57	SBA5 (SBA5#)	L4
58	SBA2 (SBA2#)	K4
59	WBF# (WBF)	K5
60	SBA0 (SBA0#)	K7
61	SBA1 (SBA1#)	J2
62	SBA3 (SBA3#)	K1
63	RBF# (RBF)	J3
64	ST0	H1
65	ST2	J5
66	ST1	H3
67	GREQ# (GREQ)	J6
68	GGNT# (GGNT)	K8
69	N/A	
70	N/A	
71	N/A	
72	N/A	
73	N/A	
74	N/A	
75	N/A	
76	N/A	
77	N/A	
78	N/A	
	HI_A5	**AA8**

Table 8-7. XOR Chain 6

	Ball Name	Ball #
1	HD59#	C12
2	HD57#	D14
3	HD56#	C14
4	HD48#	F17
5	HD50#	G17
6	HD58#	B13
7	HD60#	B12
8	DINV3#	C15
9	HDSTBN3#	C17
10	HDSTBP3#	E16
11	HD53#	D16
12	HD62#	B15
13	HD63#	A13
14	HD52#	D17
15	HD54#	A16
16	HD55#	B16
17	HD61#	A14
18	HD49#	F18
19	HD51#	A17
20	HD46#	H18
21	HD43#	C18
22	HD45#	E18
23	DINV2#	A19
24	HD40#	B18
25	HD39#	A20
26	HD41#	B19
27	HD38#	D19
28	HDSTBN2#	B21
29	HDSTBP2#	C20
30	HD42#	E19
31	HD47#	G19
32	HD35#	D20
33	HD44#	H19
34	HD33#	B22
35	HD32#	A23
36	HD37#	C21
37	HD34#	C23
38	HD36#	B24
39	HD25#	D23

	Ball Name	Ball #
40	HD31#	G20
41	HD23#	A25
42	HD30#	E22
43	HD28#	D22
44	HD22#	B25
45	HD27#	C24
46	HD26#	F23
47	HD29#	E24
48	HD18#	B27
49	HDSTBN1#	G22
50	HDSTBP1#	H21
51	HD21#	C26
52	HD20#	A26
53	DINV1#	D25
54	HD24#	H22
55	HD16#	A28
56	HD17#	B28
57	HD19#	C27
58	HD5#	A29
59	HD12#	E25
60	HD11#	D26
61	HD14#	G23
62	HD7#	A31
63	HD2#	C29
64	HD8#	B30
65	HD1#	G25
66	HD15#	H24
67	HD6#	D29
68	HDSTBN0#	E27
69	HDSTBP0#	F26
70	HD3#	C30
71	HD10#	D28
72	HD0#	B31
73	HD13#	F27
74	HD9#	E28
75	HD4#	G26
76	DINV0#	H25
77	RESERVED	J20
78	RESERVED	J21
	HI_A6	**AB8**

Table 8-8. XOR Chain 7

	Ball Name	Ball #
1	BINIT#	H4
2	AP0#	F3
3	RSP#	E1
4	AP1#	F2
5	XERR#	D1
6	BREQ0#	F12
7	HA34#	G5
8	HA28#	J8
9	HA22#	H6
10	HA30#	H7
11	HA31#	E3
12	HA25#	J9
13	HA26#	F5
14	HA21#	F6
15	HA35#	E4
16	HADSTB1#	H9
17	HA19#	J11
18	HA29#	G7
19	HA32#	C2
20	HA23#	G8
21	HA27#	D4
22	HA24#	H10
23	HA18#	J12
24	HA33#	C3
25	HA20#	E6
26	HA17#	H12
27	HA16#	D5
28	HA14#	B3
29	HA11#	E7
30	HA9#	F9
31	HA12#	C5
32	HA7#	G11
33	HA8#	D7
34	HA10#	A4
35	HADSTB0#	C6
36	HA6#	E9
37	HA5#	D8
38	HA13#	B4
39	HA4#	F11

	Ball Name	Ball #
40	HA15#	A5
41	HA3#	H15
42	HREQ2#	H13
43	HREQ3#	E10
44	HREQ0#	G10
45	HREQ4#	G14
46	HREQ1#	G13
47	ADS#	A10
48	RS1#	F14
49	RS2#	E13
50	DEP1#	D10
51	DEP0#	C9
52	DEP2#	C8
53	HTRDY#	D11
54	CPURST#	G4
55	BPRI#	F15
56	RS0#	E12
57	DEP3#	B6
58	DEFER#	H16
59	DBSY#	B7
60	HITM#	E15
61	BNR#	B10
62	HIT#	D13
63	HLOCK#	A7
64	DRDY#	A8
65	N/A	
66	N/A	
67	N/A	
68	N/A	
69	N/A	
70	N/A	
71	N/A	
72	N/A	
73	N/A	
74	N/A	
75	N/A	
76	N/A	
77	N/A	
78	N/A	
	HI_A7	**AA9**

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