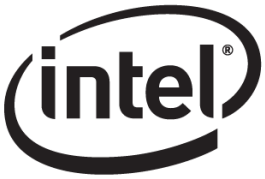

I/O Control Hub 5, 6, 7 and Intel® NM10 Express Chipset EEPROM Map and Programming Information

Application Note (AP-478)

Revision 2.0
October 2010

Revision History

Revision	Revision Date	Description
1.5	Dec. 2005	Initial public release.
2.0	Oct. 2010	Information relating to the Intel® NM10 Express Chipset was added.

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1.0 Introduction and Scope

The scope of this application note describes the EEPROM and its contents for products based upon the Intel® I/O Control Hub 5 (ICH5), I/O Control Hub 6 (ICH6), and I/O Control Hub 7 devices and the Intel® NM10 Express Chipset. These components include an integrated 10/100 Mbps LAN controller.

The EEPROM is used for hardware and software configuration. It is read by software to determine and configure specific design features. For compatibility, Intel does not create separate drivers for the integrated ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset.

Unless otherwise specified, all numbers in this document use the following numbering convention:

- Numbers that do not have a suffix are decimal (base 10).
- Numbers with a suffix of "h" are hexadecimal (base 16).
- Numbers with a suffix of "b" are binary (base 2).

1.1 EEPROM Device and Interface

The serial EEPROM stores configuration data for the controller and is an input and output device. The ICH5, ICH6, and ICH7 support 64-word or 256-word sized EEPROMs. The NM10 Express Chipset supports a 256-word sized EEPROM.

Designs based on the 82562G/GT/ET and 82562GZ/EZ require a 64-word EEPROM. A 256-word EEPROM device is required in systems based on the 82562EP/EM, 82562GX/EX or 82552V.

All accesses, read and write, are preceded by a command instruction to the EEPROM. The command instructions begin with a logical "1b" as a start bit, two opcode bits (read, write, erase, etc.), and six address bits. The end of the address field is indicated by a dummy zero bit from the EEPROM. This indicates that the entire address field has been transferred to the EEPROM. A command is issued by asserting the EEPROM Chip Select signal from the controller and clocking the data out of the EEPROM Data Input signal (which is the EEPROM Data Output signal from the ICH5, ICH6 or ICH7 controller or NM10 Express Chipset perspective) into the EEPROM on its data input pin relative to the EEPROM Shift Clock controller output. The EEPROM Chip Select signal is de-asserted after the EEPROM cycle completes (command, address and data).

The ICH5, ICH6, ICH7 and NM10 Express Chipset automatically read the EEPROM after power-up to retrieve configuration information. The length of an EEPROM read is approximately 12,480 clock cycles (499.2 µs at 100 Mbps LAN connection or 5.0 ms at 10 Mbps LAN connection). Designs using a 256-word EEPROM have an EEPROM read length of approximately 15,296 clock cycles long (611.8 µs at 100 Mbps LAN connection or 6.1 ms at 10 Mbps LAN connection).

1.2 EEPROM Programming Procedure Overview

The EEPROM can be programmed on-board through the ICH5, ICH6, ICH7 and NM10 Express Chipset. This enables the use of a Surface Mount Technology (SMT) EEPROM, which is otherwise difficult to handle with off-line automated programming equipment. The Bill Of Materials (BOM) for an ICH5, ICH6, ICH7 or NM10 Express Chipset based solution requires a blank EEPROM (93C66 for 82562EP/EM or 82562GX/EX systems, and 93C46 for 82562G/GT/ET or 82562GZ/EZ systems). Prior to programming the EEPROM, a data file unique to the Printed Board Assembly (PBA) is required. The data file contains the default EEPROM values for that particular PBA. The EEPROM image contains static and dynamic data. Static data is the basic platform configuration information. Dynamic data holds the product's Ethernet Individual Address (IA) and EEPROM checksum. This file can be created in a simple text editor and follows the format shown in the appendices, which provide an example of an EEPROM map for these designs.

EEPROMs can be programmed prior to board soldering. Some designers might prefer this method over inline programming.

Note: **EEPROM 93C46 Die Revision H** is incompatible with current and future Intel® LAN on Motherboard (LOM) designs. **EEPROM 93C46 Rev L** is recommended.

1.3 EEUPDATE Utility

Intel has created an EEUPDATE utility that meets the two basic requirements for an in-circuit programming utility. First, the utility can be used to update EEPROM images as part of an end-of-line production tool. Secondly, it can be used as a standalone development tool. The tool uses the two basic data files outlined in the following section (static data file and IA address file). To obtain a copy of this program, contact your Intel representative.

The EEUPDATE utility is flexible and can be used to update the entire EEPROM image or update only the IA address of the network controller.

1.3.1 Command Line Parameters

The DOS command format is as follows:

EEUPDATE Parameter_1 Parameter_2

where:

Parameter_1 = filename or /D

Parameter_2 = filename or /A

Parameter 1, in this example case, is file1.eep, which contains the complete EEPROM image in a specific format that is used to update the complete EEPROM. All comments in the .eep file must be preceded by a semicolon (;).

Parameter 1 can also be a switch, /D.

/D = Do not updated the complete EEPROM image.

Parameter 2, in this example case, is file2.dat, which contains a list of IA addresses. The EEUPDATE utility picks up the first unused address from this file and uses it to update the EEPROM. An address is marked as used by following the address with a date stamp. When the utility uses a specific address, it updates that address as used in a log file called eelog.dat. This file should then be used as the .dat file for the next update.

Parameter 2 can also be a switch, /A.

/A = Do not updated the Individual Address (IA).

See Appendix A and B for an example of the raw EEPROM contents.

2.0 ICH5, ICH6, ICH7 and NM10 Express Chipset EEPROM Format and Contents

Table 1 lists the EEPROM map for the ICH5, ICH6, ICH7 and NM10 Express Chipset. Each word listed is described in detail in following sections.

Table 1. ICH5, ICH6, ICH7 and NM10 Express Chipset EEPROM Address Map

Word	HIgh Byte (Bits 15:8)	Low Byte (Bits 7:0)	Used by
00h	Ethernet Individual Address Byte 2	Ethernet Individual Address Byte 1	Hardware
01h	Ethernet Individual Address Byte 4	Ethernet Individual Address Byte 3	Hardware
02h	Ethernet Individual Address Byte 6	Ethernet Individual Address Byte 5	Hardware
03h	Compatibility Byte 1	Compatibility Byte 0	Intel driver
04h	Reserved		
05h	Controller Type (02h for ICH5, ICH6, ICH7 and NM10 Express Chipset)	Connector Type	Intel driver
06h	PHY Device Record		
07h	Reserved		
08h	PWA Number Byte 4	PWA Number Byte 3	Factory
09h	PWA Number Byte 2	PWA Number Byte 1	Factory
0Ah	EEPROM ID		Hardware
0Bh	Subsystem ID		Hardware
0Ch	Subsystem Vendor ID		Hardware
0Dh	ASF Configuration / Reserved	SMB Address Field	ASF driver and hardware
0Eh to 22h	Reserved		
23h	ICH5 = Device ID ICH6 = Device ID ICH7 = Device ID NM10 Express Chipset = Device ID		
24h to 2Fh	Reserved		
30h to 33h	Intel Boot Agent Configuration		Firmware
34h to FAh	Reserved		
FFh	Checksum		Driver

Words 00h through 02h are used by the hardware and are common to all controllers. If the value in word 23h is not 0000h or FFFFh, the ICH5, ICH6, ICH7 and NM10 Express Chipset Device ID uses the information in this word.

Caution: OEMs must ensure that word 40h in the EEPROM image is set to 0044h (not FFFFh). Word 40h contains pointers for the internal micromachine, and an incorrect setting causes the controller to lock up. This condition applies to the 82562EP/EM and 82562GX/EX devices (Basic Alerting).

2.1 Ethernet Individual Address

The Ethernet Individual Address (IA) is a six byte field that must be unique for each adapter card or LOM and unique for each copy of the EEPROM image. The first three bytes are vendor-specific. The last three bytes must be unique for each copy of the EEPROM. OEM versions of the product might be required to have non-Intel IDs in the first three byte positions. The Intel default is listed in Table 2.

Table 2. Ethernet Individual Address (Words 00h - 02h)

		Individual Address Byte					
		Word 00		Word 01		Word 02	
Manufacturer	MAC Address	Byte 2	Byte 1	Byte 4	Byte 3	Byte 6	Byte 5
Intel	00AA00XXYYZZh	AAh	00h	XXh	00h	ZZh	YYh
Intel	00A0C9XXYYZZh	A0h	00h	XXh	C9h	ZZh	YYh
Intel	009027XXYYZZh	90h	00h	XXh	27h	ZZh	YYh

Note: The Ethernet IA is byte swapped, as listed in Table 2.

The IA bytes read from the EEPROM are used by the ICH5, ICH6, ICH7 and NM10 Express Chipset until an IA Setup command is issued by software. The IA defined by the IA Setup command overrides the IA read from the EEPROM.

2.2 Compatibility Fields

The compatibility fields are used by Intel drivers to determine software compatibility. Only one word in the EEPROM image is reserved for compatibility information. New bits within these fields will be defined as the need arises for determining software compatibility between various hardware revisions. These bytes are initialized during manufacturing and should be considered read only by software.

2.2.1 Compatibility Byte 0 (Word 03h)

Table 3. Compatibility Byte 0 (Word 03h)

D7	D6	D5	D4	D3	D2	D1	D0
Auto Sw Enable (0b)	Rsvd (0b)	Rsvd (0b)	SMB	RSVD (0b)	BOB (0b)	MC100 (1b)	MC10 (1b)

Table 4. Compatibility Byte 0 Field Descriptions

Bit	Name	Description
7	AUTO SWITCH ENABLE	**MDI/MDI-X Auto Switching.** Enables the MDI/MDI-X auto-switching feature. • 0b = Disabled (default). • 1b = Enabled.
6:5	Rsvd	**Reserved.** These bits are reserved and should be set to 00b.
4	SMB	**System Management Bus to Motherboard Connection.** This bit indicates whether the Ethernet controller's System Management Bus (SMB) is connected to the motherboard, thereby enabling alerting capability within the ICH5, ICH6, ICH7 or NM10 Express Chipset. Set this bit as follows: 0b = 82562G/GT/ET and 82562GZ/EZ. 1b = 82562EP/EM, 82562GX/EX or 82552V.
3	Rsvd	**Reserved.** this bit is reserved and should be set to 0b.
2	BOB	**Bridge On Board.** This bit enables software to determine whether an adaptor has a PCI bridge without scanning the PCI bus and without relying on using the Subsystem ID. It is necessary since software is not always allowed to scan the PCI bus during configuration and because OEMs are allowed to change the value of the Subsystem ID. 1b = Network Interface Card (NIC) has a PCI bridge. 0b = NIC does not have a PCI bridge. This bit is set to 0b in ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset.
1	MC100	**Multicast Workaround 100 Mbps.** The MC100 bit is discussed in further detail in the 8255x EEPROM Map and Programming Information Application Note (AP-394). This bit is set to 1b in the ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset.
0	MC10	**Multicast Workaround 10 Mbps.** The MC10 bit is discussed in further detail in the 8255x EEPROM Map and Programming Information Application Note (AP-394). This bit is set to 1b in ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset.

2.2.2 Compatibility Byte 1 (Word 03h)

Table 5. Compatibility Byte 1 (Word 03h)

D7	D6	D5	D4	D3	D2	D1	D0
Rsvd (0b)	Rsvd (0b)	Rsvd (0b)	ICH5/ ICH6/ ICH7/ NM10 Express (1b)	LOM (1b)	SRV (0b)	CLI (1b)	OEM

Table 6. Compatibility Byte 1 Field Descriptions

Bit	Name	Description
7:5	Rsvd	**Reserved.** These bits should be set to 000b.
4	ICH5/ICH6/ ICH7/NM10 Express Chipset	**ICH5/ICH6/ICH7/NM10 Express Chipset.** This bit indicates to software that this design uses an ICH5, ICH6 or ICH7 controller or NM10 Express Chipset. 0b = An ICH5, ICH6 or ICH7 controller and NM10 Express Chipset is not on the motherboard. 1b = An ICH5, ICH6 or ICH7 controller and NM10 Express Chipset is located on the motherboard. This bit is set to 1b for ICH5, ICH6, and ICH7 controllers and NM10 Express Chipset.
3	LOM	**ICH5/ICH6/ICH7/NM10 Express Chipset integrated with LAN on Motherboard.** This bit indicates to software that the ICH5, ICH6 or ICH7 controller or NM10 Express Chipset is located on the motherboard. 0b = An ICH5, ICH6 or ICH7 controller or NM10 Express Chipset is not on the motherboard. 1b = An ICH5, ICH6 or ICH7 controller or NM10 Express Chipset is located on the motherboard. This bit is set to 1b for ICH5, ICH6, and ICH7 controllers and NM10 Express Chipset.
2	SRV	**Server.** This bit indicates to software that the card is a server adapter and server extensions are allowed. 0b = Disables Server extensions. 1b = Enables Server extensions. This bit is set to 0b for ICH5, ICH6, and ICH7 controllers and NM10 Express Chipset.
1	CLI	**Client.** This bit indicates to software that the ICH5, ICH6, and ICH7 controllers and NM10 Experss Chipset enable client only features. 0b = Disables Client features. 1b = Enables Client features. This bit is set to 1b for ICH5, ICH6, and ICH7 controllers and NM10 Express Chipset. **NOTE:** If the CLI bit equals 0b, the adapter should be considered a legacy product and the feature set is undefined.
0	OEM	**OEM.** The OEM bit indicates whether the product is identified with a vendor name other than Intel. Software must examine the Subsystem ID and Subsystem Vendor ID fields for more information. 0b = Intel. 1b = Vendor name other than Intel.

2.3 ICH5, ICH6, ICH7 and NM10 Express Chipset Hardware Description Fields

The hardware description fields of the EEPROM describe the component configuration for the product (design). These fields are used by Intel drivers and the controller to determine ICH5, ICH6, ICH7 and NM10 Express Chipset with integrated LAN controller configuration.

2.3.1 Controller Type (Word 05h)

This byte wide field indicates which Intel Fast Ethernet controller (for example, the ICH5, ICH6, ICH7, or NM10 Express Chipset) or compatible Home Phoneline Networking Alliance adapter is installed. It also provides a supplementary method of differentiating between the controllers in addition to the PCI Revision ID field. For the ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset, this byte equals 02h.

Table 7. Controller Type IDs

Controller Description	Controller Type
ICH5 (82559 compatible by default)	2h
ICH6 (82559 compatible by default)	2h
ICH7 (82559 compatible by default)	2h
NM10 Express Chipset (82559 compatible by default)	2h

2.3.2 Connector Types (Word 05h)

This word identifies the connector types used in the design. An RJ-45 connector is used for an Ethernet controller. Its type equals 01h.

Table 8. Connector Types (Word 05h)

D7	D6	D5	D4	D3	D2	D1	D0
Rsvd (0b)	Rsvd (0b)	Rsvd (0b)	RJ-11	MII (0b)	AUI (0b)	BNC (0b)	RJ-45

Table 9. Word 05h Field Descriptions

Bit	Name	Description
7:5	Reserved	**Reserved.** These bits are reserved and should be set to 000b.
4	RJ-11	**RJ-11.** The RJ-11 bit identifies whether an RJ-11 connector is installed. 1b = Supported. 0b = Not supported (82562G/GT/ET, 82562EP/EM, 82562GZ/EZ, 82562GX/EX or 82552V).
3	MII	**MII.** The MII bit indicates whether 10BASE-T and 100BASE-T are supported through an external transceiver. The MII Status Register specifies which 100BASE-T technology is provided (for example, TX or T4). 1b = Supported through an external transceiver. 0b = Not supported through an external transceiver (default).
2	AUI	**AUI.** The AUI bit indicates whether 10BASE-5 technology is supported. 1b = Supported. 0b = Not supported (default).
1	BNC	**BNC.** The BNC bit indicates whether 10BASE-2 technology is supported. 1b = Supported. 0b = Not supported (default).
0	RJ-45	**RJ-45.** The RJ-45 bit identifies whether an RJ-45 connector is installed. The ICH5, ICH6, ICH7 and NM10 Express Chipset support 10BASE-T and 100BASE-T technology. The MII Status Register specifies which 100BASE-T technology is provided (for example, TX or T4). The 82562G/GT/ET, 82562EP/EM, 82562GZ/EZ, 82562GX/EX and 82552V use an RJ-45 connector. 1b = Supported (82562G/GT/ET, 82562EP/EM, 82562GZ/EZ, 82562GX/EX or 82552V). 0 = Not supported.

2.3.3 PHY Device Records (Word 06h)

The PHY device records are used to describe an external PHY. In ICH5, ICH6, ICH7 and NM10 Express Chipset based designs, word 07h is not used. Word 06h contains a value of 4701h for the 82562G/GT/ET, 82562EP/EM, 82562GZ/EZ, 82562GX/EX or 82552V. Word 07h should equal 0000h.

Table 10. PHY Device Records (Word 06h)

D15	D14	D13 - D8	D7 - D0
10 Mbps	VSCR	PHY Device	PHY Address

Table 11. Word 06h Field Descriptions

Bit	Name	Description
15	10 Mbps	**10 Mbps.** This bit designates whether or not the PHY is a 10 Mbps only device. This bit is set to 1b for 82562G/GT/ET, 82562EP/EM, 82562GZ/EZ, 83562GX/EX and 82552V designs if the ADV10 input equals 1b. Otherwise, this bit equals 0b.
14	VSCR	**Vendor Specific Code Requirement.** Designs use this bit to set or report the operating mode through the vendor specific requirements. If this bit is set to 1b, it indicates that the PHY device requires special programming (either to set or report the correct operating mode) through vendor specific registers of the MII Management Interface. Legacy drivers determine if the PHY device is 100 Mbps MII capable, and all status and control is achieved through the standard MII register set defined by the IEEE 802.3u standard. If the VSCR bit equals 0b, the software driver can use its standard configuration code path, even if the PHY Device code (or PHY Identifier found in the MII register) is not recognized. Table 12 lists vendor codes and their associated devices. This value is 1b for 82562G/GT/ET, 82562EP/EM, 82562GZ/EZ, 82562GX/EX and 82552V designs.
13:8	PHY Device	**PHY Device.** This field contains an arbitrarily assigned code that uniquely identifies any device that can be used with the products based on the 82559 Fast Ethernet controller. This value is 7h for 82562G/GT/ET, 82562EP/EM, 82562GZ/EZ, 82562GX/EX and 82552V designs.
7:0	PHY Address	**PHY Address.** This field indicates the PHY address for the given device. The PHY address is relevant only for devices that support the MII Management Interface. The default address for a single PHY solution is 01h. This value is 01h for ICH5, ICH6, and ICH7 controllers and NM10 Express Chipset.

Table 12. PHY Device Codes

PHY Device Code	PHY Device
0h	No PHY device installed
1h	Intel® 82553 (PHY100) A or B Step
2h	Intel® 82553 (PHY100) C Step
3h	Intel® 82503 10 Mbps
4h	National Semiconductor* DP83840
5h	Seeq* 80C240 100BASE-T4
6h	Seeq 80C24 10 Mbps
7h	Intel® 82555 10/100BASE-TX PHY
8h	Microlinear* 10 Mbps
9h	Level One* 10 Mbps
Ah	National Semiconductor DP83840A
Bh	ICS* 1890

2.3.4 Printed Wire Assembly Number (Words 08h - 09h)

The nine digit Printed Wire Assembly (PWA) number is stored in this four byte field. Neither the dash or the first digit of the three digit suffix is stored. The PWA information identifies the revision level of a product. The network driver should not rely on this field to identify the product or its capabilities.

Table 13. PWA Number (Words 08h - 09h)

Product	PWA Number	Byte 1	Byte 2	Byte 3	Byte 4
PILA8465B (TX)	352509-003	35h	25h	09h	03h
PILA8475B (T4)	352433-003	35h	24h	33h	03h
PILA8500 (10)	645477-003	64h	54h	77h	03h
PILA8520 (10)	649439-003	64h	94h	39h	03h
PILA8460	697680-001	69h	76h	80h	01h
PILA8460B	727095-004	72h	70h	95h	04h
PILA8461	704920-001	70h	49h	20h	01h
PILA8470B	735190-001	73h	51h	90h	01h

Note: The suffix field (byte 4) is incremented through the course of hardware Engineering Change Orders (ECOs).

Printed Wire Assembly numbers are used for Intel products only. This value should equal 00h for OEMs.

2.4 ICH5, ICH6, ICH7 and NM10 Express Chipset Product Identification

2.4.1 EEPROM ID (Word 0Ah)

ICH5, ICH6, and ICH7 controllers and NM10 Express Chipset read the EEPROM ID (word 0Ah) to obtain basic power-on configuration information.

Note: The format for this word has evolved substantially from controller to controller.

The Signature bits of this word are used to indicate the validity of this word. If the Signature bits equal 01b, the word is valid and the remaining contents of the EEPROM ID are used to determine configuration information. If the Signature bits do not equal 01b, the EEPROM ID is invalid and the controller uses default values for its configuration.

Word 0Ah is the only section of the EEPROM map that affects the basic functionality of the ICH5, ICH6, ICH7 or NM10 Express Chipset. Although other fields within the EEPROM are loaded into the controller, their impact is limited to loading values such as the IA. Table 14 lists the format of word 0Ah for the ICH5, ICH6, ICH7 or NM10 Express Chipset EEPROM.

Table 14. ICH5, ICH6, ICH7 and NM10 Express Chipset EEPROM (Word 0Ah)

15:14	13	12	11	10:8	7	6	5	4	3:2	1	0
Sig (01b)	ID (0b)	Rsvd (0b)	BD (1b)	Alt Rev ID	PM (1b)	DDPD (0b)	WoL	IA LED	Reserved (00b)	STB Ena (1b)	Rsvd (0b)

Table 15. Word 0Ah Field Descriptions

Bits	Name	Description
15:14	Sig	**Signature.** If this field equals 01b, the remainder of word 0Ah is read to determine the basic functionality of the ICH5, ICH6, ICH7 and NM10 Express Chipset. If the this field does not contain a value of 01b, then the remainder of word 0Ah is ignored and default configuration values are used for the parameters that would have been configured by this word. These bits are set to 01b for ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset.
13	ID	**ID.** The ID bit indicates how the Subsystem ID and Subsystem Vendor ID is used. If the controller detects the presence of an EEPROM (as indicated by a value of 01b in the Signature field), this bit is defined as follows: 1b = The value stored in word 23h (Device ID) is loaded into the Device ID, and the Vendor ID field is loaded from word 0Ch (Vendor ID). 0b = The Device ID and Vendor ID fields in PCI Configuration space remain at their default values. This bit is set to 0b for ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset.
12	Rsvd	**Reserved.** This bit is reserved and should be set to 0b. This bit cannot be reassigned to any other function. This bit is set to 0b for ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset.
11	BD	**Boot Disable.** When this bit is set, it disables the Expansion ROM Base Address Register (PCI Configuration space, offset 30h). This bit is set to 1b for ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset.
10:8	Alt Rev ID	**Alternate Revision ID.** These bits are used as the three least significant bits of the device revision if bits 15:14 equal 01b and the PCI Revision ID is set as described in: Section 2.4.2, "ICH5 Integrated 10/100 Mbps LAN Controller Product Identification", Section 2.4.3, "ICH6 Integrated 10/100 Mbps LAN Controller Product Identification", Section 2.4.4, “ICH7 Integrated 10/100 Mbps LAN Controller Product Identification". Section 2.4.5, “NM10 Express Chipset Integrated 10/100 Mbps LAN Controller Product Identification”. For ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset, these bits should be set to mirror the Revision ID of the silicon. **Note:** In most cases, the Alternate Revision ID is not used. However, these bits should mirror the revision of the silicon in the event this field is unintentionally enabled.
7	PM	**Power Management.** This should always be set to 1b (always enabled) for ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset.

Table 15. Word 0Ah Field Descriptions

Bits	Name	Description
6	DDPD	**Disable Deep Power Down.** When using the Intel® ASF Software Development Kit (SDK), this bit is controlled by the ASF software as the system transitions through power states. This bit should be set to 1b if an IPMI management controller (Total Cost of Ownership [TCO] controller) is being used through the TCO/SMB since it requires receive functionality at all power states. 0b = Deep Power Down enabled in the D3 state while Power Management is disabled. 1b = Deep Power Down disabled in the D3 state while Power Management is disabled. This bit is set to 0b for ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset.
5	WOL	**Wake on LAN.** If the Wake on LAN (WOL) bit is set and Wake on Magic Packet* or Wake on Link Status Change are enabled, the Power Management Enable (PME) bit is ignored with respect to these events. In this case, the Power Management Event signal should be asserted by Magic Packet Wake or Link Status Change. The WOL bit is set to put the ICH5, ICH6, ICH7 and NM10 Express Chipset into Wake on LAN mode. These devices enter WOL mode after the Power-up Reset signal is asserted and they have read the EEPROM. When the ICH5, ICH6, ICH7 and NM10 Express Chipset are in WOL mode, the controllers read three additional words from the EEPROM (words 0h, 1h, and 2h). These words are expected to contain the Individual Address. 0b = WOL mode disabled. 1b = WOL mode enabled. This bit is configured by the OEM.
4	IA LED	**Individual Address LED.** This bit controls the Activity LED (ACTLED) functionality in Wake on LAN (WOL) mode. 0b = In WOL mode, the ACTLED is activated by the transmission and reception of broadcast and Individual Address match packets. 1b = In WOL mode, the ACTLED is activated by the transmission and reception of Individual Address match packets only. This bit is configured by the OEM.
3:2	Rsvd	**Reserved.** These bits are reserved and should be set to 00b. These bits cannot be reassigned to any other function.
1	STB Enable	**Standby Enable.** This bit enables the ICH5, ICH6, ICH7 and NM10 Express Chipset to enter standby mode. When this bit equals 1b, these devices can recognize an idle state and can enter standby mode (some internal clocks are stopped for lower power consumption). They do not require a PCI clock signal in standby mode. If this bit equals 0b, the idle recognition circuit is disabled and the ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset will always remain in an active state. Thus, these devices always request the PCI clock signal using the Clockrun mechanism. This bit is set to 1b for ICH5, ICH6, and ICH7 controllers and the NM10 Express Chipset.
0	Rsvd	**Reserved.** This bit is reserved and should be set to 0b. This bit cannot be reassigned to any other function.

2.4.2 ICH5 Integrated 10/100 Mbps LAN Controller Product Identification

When a valid EEPROM is present, the Device ID is loaded from the EEPROM word 23h after reset if the value of word 23h does not equal 0000h or FFFFh. If a valid EEPROM is not present or the value of word 23h equals 0000h or FFFFh, the Device ID default value is read as 1051h. The ICH5 with integrated LAN provides support for configurable Device ID, Subsystem ID and Subsystem Vendor ID fields.

After hardware reset is de-asserted, the ICH5 automatically reads addresses 0Ah through 0Ch and word 23h of the EEPROM. Word 0Ah is used for controlling various ICH5 functions. Words 0Bh and 0Ch are used for the Subsystem ID and Subsystem Vendor ID values, respectively, and word 23h is the Device ID value. The default values for the Subsystem ID and Subsystem Vendor ID are 00h and 00h, respectively. The ICH5 checks bit numbers 15:13 in the EEPROM word 0Ah and acts according to the table below:

Table 16. ICH5 Controller Identification Values

Bits 15:14 (Word 0Ah)	Bit 13 (Word 0Ah)	Device ID (PCI Space)[a]	Vendor ID (PCI Space)	Revision ID[b]	Subsystem ID	Subsystem Vendor ID
11b, 10b, 00b	Don't care	1051h	8086h	Default	0000h	0000h
01b	0b	Value of word 23h	8086h	Default	Value of Word 0Bh	Value of Word 0Ch
01b	1b	Value of word 23h	Value of word 0Ch	Default plus value of Word 0Ah Bits 10:8	Value of Word 0Bh	Value of Word 0Ch

a. The Device ID is loaded from word 23h only if the value in word 23h is not equal to 0000h or FFFFh. Otherwise, the default is loaded.

b. The Revision ID is subject to change depending upon the silicon stepping.

The table listings imply that if the ICH5 detects the presence of an EEPROM (as indicated by a value of 01b in bits 15 and 14), then bit 13 affects the value loaded in the Vendor ID and Revision ID. If bits 15 and 14 equal 01b and bit 13 equals 1b, the three least significant bits of the Revision ID field are programmed by bits 10:8 of the EEPROM word 0Ah. If EEPROM word 23h is not 0000h or FFFFh, then the ICH5 assumes this value represents the Device ID to be loaded. The word 23h value overwrites the default Device ID in this case.

2.4.2.1 ICH5 Integrated 10/100 Mbps LAN Controller Vendor ID (PCI Space)

The Vendor ID field identifies the vendor of an ICH5-based solution. The Vendor ID values are based upon the vendor's PCI Vendor ID and are controlled by the PCI Special Interest Group (SIG). Intel generates this ID. Intel's PCI vendor ID is 8086.

2.4.2.2 ICH5 Integrated 10/100 Mbps LAN Controller Device ID (PCI Space)

The ICH5 with integrated LAN provides support for a configurable Device ID. This one word (16-bit) field identifies the PCI Device ID for the ICH5 integrated 10/100 Mbps LAN Controller. For OEM products, Intel's Device ID number must be used as listed in Table 17.

2.4.2.3 ICH5 Integrated 10/100 Mbps LAN Controller Subsystem ID (Word 0Bh)

The ICH5 with integrated LAN provides support for a configurable Subsystem ID. This one word (16-bit) field identifies the product number for the vendor. The Subsystem ID field identifies the ICH5 based specific solution implemented by the vendor. For OEM products, the OEM's Subsystem ID number must be used.

2.4.2.4 ICH5 Integrated 10/100 Mbps LAN Controller Subsystem Vendor ID (Word 0Ch)

The ICH5 with integrated LAN provides support for configurable Subsystem Vendor ID. This one word (16-bit) field identifies the OEM vendor. The code used for a particular vendor is the same code assigned as the Vendor ID by the PCI SIG. For OEM products, the OEM's Subsystem Vendor ID number must be used.

Table 17. Product Names/Configurations IDs for ICH5 (Word 0Ch)

Product Name	Product Configuration	Vendor ID	Device ID (Word 23h)
Intel® PRO/100 VE Network Connection	Intel® ICH5 LOM with 82562GT/ET PLC or 82562GZ/EZ PLC	8086h	1050h
Intel® PRO/100 VE Network Connection	Intel® ICH5 with 82562GT/ET Adapter or 82562GZ/EZ Adapter	8086h	1051h
Intel® PRO/100 VM Network Connection	Intel® ICH5 LOM with 82562EM PLC or 82562GX/EX PLC	8086h	1052h
Intel® PRO/100 VM Network Connection	Intel® ICH5 with 82562EM Adapter or 82562GX/EX Adapter	8086h	1053h
Intel® PRO/100 VE Network Connection	Intel® ICH5 LOM or Mobile LOM with 82562GT/ET PLC or 82562GZ/EZ PLC	8086h	1054h
Intel® PRO/100 VM Network Connection	Intel® ICH5 LOM or Mobile LOM with 82562EP/EM or PLC or 82562GX/EX PLC	8086h	1055h

NOTE: The Subsystem ID and Subsystem Vendor ID fields, words 0Bh and 0Ch, respectively, are defined by the OEM. (Refer to the Microsoft* *Specification for Use of PCI IDs with Windows* Operating Systems* for more details.)

2.4.3 ICH6 Integrated 10/100 Mbps LAN Controller Product Identification

When a valid EEPROM is present, the Device ID is loaded from the EEPROM word 23h after reset if the value of word 23h does not equal 0000h or FFFFh. If a valid EEPROM is not present or the value of word 23h equals 0000h or FFFFh, the Device ID default value is read as 1065h. The ICH6 with integrated LAN provides support for configurable Device ID, Subsystem ID and Subsystem Vendor ID fields.

After hardware reset is de-asserted, the ICH6 automatically reads addresses 0Ah through 0Ch and word 23h of the EEPROM. Word 0Ah is used for controlling various ICH6 functions. Words 0Bh and 0Ch are used for the Subsystem ID and Subsystem Vendor ID values, respectively, and word 23h is the Device ID value. The default values for the Subsystem ID and Subsystem Vendor ID are 00h and 00h, respectively. The ICH6 checks bit numbers 15:13 in the EEPROM word 0Ah and acts according to the table below:

Table 18. ICH6 Controller Identification Values

Bits 15:14 (Word 0Ah)	Bit 13 (Word 0Ah)	Device ID[a] (PCI Space)	Vendor ID (PCI Space)	Revision ID[b]	Subsystem ID	Subsystem Vendor ID
11b, 10b, 00b	Don't care	1065h	8086h	Default	0000h	0000h
01b	0b	Value of word 23h	8086h	Default	Value of Word 0Bh	Value of Word 0Ch
01b	1b	Value of word 23h	Value of word 0Ch	Default plus value of Word 0Ah Bits 10:8	Value of Word 0Bh	Value of Word 0Ch

a. The Device ID is loaded from word 23h only if the value in word 23h is not equal to 0000h or FFFFh. Otherwise, the default is loaded.

b. The Revision ID is subject to change depending upon the silicon stepping.

The table listings imply that if the ICH6 detects the presence of an EEPROM (as indicated by a value of 01b in bits 15 and 14), then bit 13 affects the value loaded in the Vendor ID and Revision ID. If bits 15 and 14 equal 01b and bit 13 equals 1b, the three least significant bits of the Revision ID field are programmed by bits 10:8 of the EEPROM word 0Ah. If EEPROM word 23h is not 0000h or FFFFh, then the ICH6 assumes this value represents the Device ID to be loaded. The word 23h value overwrites the default Device ID in this case.

2.4.3.1 ICH6 Integrated 10/100 Mbps LAN Controller Vendor ID (PCI Space)

The Vendor ID field identifies the vendor of an ICH6-based solution. The Vendor ID values are based upon the vendor's PCI Vendor ID and are controlled by the PCI Special Interest Group (SIG). Intel generates this ID. Intel's PCI vendor ID is 8086.

2.4.3.2 ICH6 Integrated 10/100 Mbps LAN Controller Device ID (PCI Space)

The ICH6 with integrated LAN provides support for a configurable Device ID. This one word (16-bit) field identifies the PCI Device ID for the ICH6 integrated 10/100 Mbps LAN Controller. For OEM products, Intel's Device ID number must be used as defined in Table 19.

2.4.3.3 ICH6 Integrated 10/100 Mbps LAN Controller Subsystem ID (Word 0Bh)

The ICH6 with integrated LAN provides support for a configurable Subsystem ID. This one word (16-bit) field identifies the product number for the vendor. The Subsystem ID field identifies the ICH6 based specific solution implemented by the vendor. For OEM products, the OEM's Subsystem ID number must be used.

2.4.3.4 ICH6 Integrated 10/100 Mbps LAN Controller Subsystem Vendor ID (Word 0Ch)

The ICH6 with integrated LAN provides support for configurable Subsystem Vendor ID. This one word (16-bit) field identifies the OEM vendor. The code used for a particular vendor is the same code assigned as the Vendor ID by the PCI SIG. For OEM products, the OEM's Subsystem Vendor ID number must be used.

Table 19. Product Names/Configurations IDs for ICH6 (Word 0Ch)

Product Name	Product Configuration	Vendor ID	Device ID (Word 23h)
Intel® PRO/100 VE Network Connection	Intel® ICH6 LOM with 82562GT/ET PLC or 82562GZ/EZ PLC	8086h	1064h
Intel® PRO/100 VE Network Connection	Intel® ICH6 with 82562GT/ET Adapter or 82562GZ/EZ Adapter	8086h	1065h
Intel® PRO/100 VM Network Connection	Intel® ICH6 LOM with 82562EM PLC or 82562GX/EX PLC	8086h	1066h
Intel® PRO/100 VM Network Connection	Intel® ICH6 with 82562EM Adapter or 82562GX/EX Adapter	8086h	1067h
Intel® PRO/100 VE Network Connection	Intel® ICH6 LOM or Mobile LOM with 82562GT/ET PLC or 82562GZ/EZ PLC	8086h	1068h
Intel® PRO/100 VM Network Connection	Intel® ICH6 LOM or Mobile LOM with 82562EP/EM or PLC or 82562GX/EX PLC	8086h	1069h
Intel® PRO/100 VE Network Connection	Intel® ICH6 LOM with 82562G PLC	8086h	106Ah
Intel® PRO/100 VE Network Connection	Intel® ICH6 Mobile with 82562G PLC	8086h	106Bh

NOTE: The Subsystem ID and Subsystem Vendor ID fields, words 0Bh and 0Ch, respectively, are defined by the OEM. (Refer to the Microsoft* *Specification for Use of PCI IDs with Windows* Operating Systems* for more details.)

2.4.4 ICH7 Integrated 10/100 Mbps LAN Controller Product Identification

When a valid EEPROM is present, the Device ID is loaded from the EEPROM word 23h after reset if the value of word 23h does not equal 0000h or FFFFh. If a valid EEPROM is not present or the value of word 23h equals 0000h or FFFFh, the Device ID default value is read as 1091h. The ICH7 with integrated LAN provides support for configurable Device ID, Subsystem ID and Subsystem Vendor ID fields.

After hardware reset is de-asserted, the ICH7 automatically reads addresses 0Ah through 0Ch and word 23h of the EEPROM. Word 0Ah is used for controlling various ICH6 functions. Words 0Bh and 0Ch are used for the Subsystem ID and Subsystem Vendor ID values, respectively, and word 23h is the Device ID value. The default values for the Subsystem ID and Subsystem Vendor ID are 00h and 00h, respectively. The ICH7 checks bit numbers 15:13 in the EEPROM word 0Ah and acts according to the table below:

Table 20. ICH7 Controller Identification Values

Bits 15:14 (Word 0Ah)	Bit 13 (Word 0Ah)	Device ID[a] (PCI Space)	Vendor ID (PCI Space)	Revision ID[b]	Subsystem ID	Subsystem Vendor ID
11b, 10b, 00b	Don't care	1091h	8086h	Default	0000h	0000h
01b	0b	Value of word 23h	8086h	Default	Value of Word 0Bh	Value of Word 0Ch
01b	1b	Value of word 23h	Value of word 0Ch	Default plus value of Word 0Ah Bits 10:8	Value of Word 0Bh	Value of Word 0Ch

a. The Device ID is loaded from word 23h only if the value in word 23h is not equal to 0000h or FFFFh. Otherwise, the default is loaded.

b. The Revision ID is subject to change depending upon the silicon stepping.

The table listings imply that if the ICH7 detects the presence of an EEPROM (as indicated by a value of 01b in bits 15 and 14), then bit 13 affects the value loaded in the Vendor ID and Revision ID. If bits 15 and 14 equal 01b and bit 13 equals 1b, the three least significant bits of the Revision ID field are programmed by bits 10:8 of the EEPROM word 0Ah. If EEPROM word 23h is not 0000h or FFFFh, then the ICH6 assumes this value represents the Device ID to be loaded. The word 23h value overwrites the default Device ID in this case.

2.4.4.1 ICH7 Integrated 10/100 Mbps LAN Controller Vendor ID (PCI Space)

The Vendor ID field identifies the vendor of an ICH7-based solution. The Vendor ID values are based upon the vendor's PCI Vendor ID and are controlled by the PCI Special Interest Group (SIG). Intel generates this ID. Intel's PCI vendor ID is 8086.

2.4.4.2 ICH7 Integrated 10/100 Mbps LAN Controller Device ID (PCI Space)

The ICH7 with integrated LAN provides support for a configurable Device ID. This one word (16-bit) field identifies the PCI Device ID for the ICH7 integrated 10/100 Mbps LAN Controller. For OEM products, Intel's Device ID number must be used as defined in Table 21.

2.4.4.3 ICH7 Integrated 10/100 Mbps LAN Controller Subsystem ID (Word 0Bh)

The ICH7 with integrated LAN provides support for a configurable Subsystem ID. This one word (16-bit) field identifies the product number for the vendor. The Subsystem ID field identifies the ICH7 based specific solution implemented by the vendor. For OEM products, the OEM's Subsystem ID number must be used.

2.4.4.4 ICH7 Integrated 10/100 Mbps LAN Controller Subsystem Vendor ID (Word 0Ch)

The ICH7 with integrated LAN provides support for configurable Subsystem Vendor ID. This one word (16-bit) field identifies the OEM vendor. The code used for a particular vendor is the same code assigned as the Vendor ID by the PCI SIG. For OEM products, the OEM's Subsystem Vendor ID number must be used.

Table 21. Product Names/Configurations IDs for ICH7 (Word 0Ch)

Product Name	Product Configuration	Vendor ID	Device ID (Word 23h)
Intel® PRO/100 VE Network Connection	Intel® ICH7 LOM with 82562GT/ET PLC or 82562GZ/EZ PLC	8086h	27DCh
Intel® PRO/100 VM Network Connection	Intel® ICH7 LOM with 82562EM PLC or 82562GX/EX PLC	8086h	1091h
Intel® PRO/100 VE Network Connection	Intel® ICH7 LOM or Mobile LOM with 82562GT/ET PLC or 82562GZ/EZ PLC	8086h	1092h
Intel® PRO/100 VM Network Connection	Intel® ICH7 LOM or Mobile with 82562EP/EM PLC or 82562GX/EX PLC	8086h	1093h
Intel® PRO/100 VE Network Connection	Intel® ICH7 LOM with 82562G PLC	8086h	1094h
Intel® PRO/100 VE Network Connection	Intel® ICH7 Mobile with 82562G PLC	8086h	1095h

NOTE: The Subsystem ID and Subsystem Vendor ID fields, words 0Bh and 0Ch, respectively, are defined by the OEM. (Refer to the Microsoft* *Specification for Use of PCI IDs with Windows* Operating Systems* for more details.)

2.4.5 NM10 Express Chipset Integrated 10/100 Mbps LAN Controller Product Identification

When a valid EEPROM is present, the Device ID is loaded from the EEPROM word 23h after reset if the value of word 23h does not equal 0000h or FFFFh. If a valid EEPROM is not present or the value of word 23h equals 0000h or FFFFh, the Device ID default value is read as 10FEh. The NM10 Express Chipset with integrated LAN provides support for configurable Device ID, Subsystem ID and Subsystem Vendor ID fields.

After hardware reset is de-asserted, the NM10 Express Chipset automatically reads addresses 0Ah through 0Ch and word 23h of the EEPROM. Word 0Ah is used for controlling various ICH6 functions. Words 0Bh and 0Ch are used for the Subsystem ID and Subsystem Vendor ID values, respectively, and word 23h is the Device ID value. The default values for the Subsystem ID and Subsystem Vendor ID are 00h and 00h, respectively. The NM10 Express Chipset checks bit numbers 15:13 in the EEPROM word 0Ah and acts according to the following table.

Table 22. NM10 Express Chipset Identification Values

Bits 15:14 (Word 0Ah)	Bit 13 (Word 0Ah)	Device ID[a] (PCI Space)	Vendor ID (PCI Space)	Revision ID[b]	Subsystem ID	Subsystem Vendor ID
11b, 10b, 00b	Don't care	10FEh	8086h	Default	0000h	0000h
01b	0b	Value of word 23h	8086h	Default	Value of Word 0Bh	Value of Word 0Ch
01b	1b	Value of word 23h	Value of word 0Ch	Default plus value of Word 0Ah Bits 10:8	Value of Word 0Bh	Value of Word 0Ch

a. The Device ID is loaded from word 23h only if the value in word 23h is not equal to 0000h or FFFFh. Otherwise, the default is loaded.

b. The Revision ID is subject to change depending upon the silicon stepping.

The table listings imply that if the NM10 Express Chipset detects the presence of an EEPROM (as indicated by a value of 01b in bits 15 and 14), then bit 13 affects the value loaded in the Vendor ID and Revision ID. If bits 15 and 14 equal 01b and bit 13 equals 1b, the three least significant bits of the Revision ID field are programmed by bits 10:8 of the EEPROM word 0Ah. If EEPROM word 23h is not 0000h or FFFFh, then the ICH6 assumes this value represents the Device ID to be loaded. The word 23h value overwrites the default Device ID in this case.

2.4.5.1 NM10 Express Chipset Integrated 10/100 Mbps LAN Controller Vendor ID (PCI Space)

The Vendor ID field identifies the vendor of an NM10 Express Chipset-based solution. The Vendor ID values are based upon the vendor's PCI Vendor ID and are controlled by the PCI Special Interest Group (SIG). Intel generates this ID. Intel's PCI vendor ID is 8086.

2.4.5.2 NM10 Express Chipset Integrated 10/100 Mbps LAN Controller Device ID (PCI Space)

The NM10 Express Chipset with integrated LAN provides support for a configurable Device ID. This one word (16-bit) field identifies the PCI Device ID for the NM10 Express Chipset integrated 10/100 Mbps LAN Controller. For OEM products, Intel's Device ID number must be used as defined in Table 23.

2.4.5.3 NM10 Express Chipset Integrated 10/100 Mbps LAN Controller Subsystem ID (Word 0Bh)

The NM10 Express Chipset with integrated LAN provides support for a configurable Subsystem ID. This one word (16-bit) field identifies the product number for the vendor. The Subsystem ID field identifies the NM10 Express Chipset based specific solution implemented by the vendor. For OEM products, the OEM's Subsystem ID number must be used.

2.4.5.4 NM10 Express Chipset Integrated 10/100 Mbps LAN Controller Subsystem Vendor ID (Word 0Ch)

The NM10 Express Chipset with integrated LAN provides support for configurable Subsystem Vendor ID. This one word (16-bit) field identifies the OEM vendor. The code used for a particular vendor is the same code assigned as the Vendor ID by the PCI SIG. For OEM products, the OEM's Subsystem Vendor ID number must be used.

Table 23. Product Names/Configurations IDs for NM10 Express Chipset (Word 0Ch)

Product Name	Product Configuration	Vendor ID	Device ID (Word 23h)
Intel® 82552V 10/100 Network Connection	Intel® NM10 Express Chipset LOM with 82552V	8086h	10FEh

NOTE: The Subsystem ID and Subsystem Vendor ID fields, words 0Bh and 0Ch, respectively, are defined by the OEM. (Refer to the Microsoft* *Specification for Use of PCI IDs with Windows* Operating Systems* for more details.)

2.5 Integrated ASF Information

The ICH5, ICH6, ICH7 and NM10 Express Chipset include an integrated Alert Sending Device (ASD) to support ASF, Version 1.0.

2.5.1 SMB Address (Word 0Dh)

In PCI systems word 0Dh contains the ICH5, ICH6, ICH7 and NM10 Express Chipset SMB address.

Table 24. SMB Address (Word 0Dh)

Bits	Field	Description
15	ASF Enabled	**ASF Enabled.** This bit specifies whether ASF is enabled: 1b = ASF is enabled. 0b = ASF is NOT enabled.
14	Rsvd	**Reserved.** This bit is reserved for the ICH5, ICH6, ICH7 and NM10 Express Chipset. Set this bit to 0b.
11:8	Rsvd	**Reserved.** These bits are reserved and should be set to 0.
7:0	SMB Address	**SMB Address.** In a PCI system, this 8-bit field holds the ICH5, ICH6, ICH7 or NM10 Express Chipset address on the SMB address bus. However, bit seven is ignored. As a result, the address programmed into the EEPROM must be shifted right one bit. For example, address C8h is programmed as address 64h in bits 7:0.

NOTE: When using Intel ASF software these fields should be 007Fh at the factory. The SMB Address in this field are configured by the ASF software when it initializes.

2.5.1.1 Word 40h

This field must be configured to 0044h for proper operation. OEMs must ensure that word 40h in the EEPROM image is set to 0044h (not FFFFh). Word 40h contains pointers for the internal micromachine. An incorrect setting causes the controller to lock up. This condition applies to the 82562EP/EM and 82562GX/EX devices (Basic Alerting).

2.6 Boot Agent Configuration Information

2.6.1 Boot Agent Main Setup Options (Word 30h)

The boot agent software configuration is controlled by the EEPROM with the main setup options stored in word 30h. These options are those that can be changed by using the Control-S setup menu or by using the IBA Intel Boot Agent utility.

Note: These settings only apply to Boot Agent software.

Table 25. Boot Agent Main Setup Options

Bit	Name	Description
15	PPB	**PXE Presence.** Setting this bit to 0b indicates that the image in the Flash contains a PXE image. 1b = No PXE image is contained. 0b = EEPROM word 32h (PXE version) is valid. The default for this bit is 0b in order to be backwards compatible with existing systems already in the field. If this bit is set to 0b when EPB is set to 1b, it indicates that both images are present in the Flash.
14	EPB	**EFI Presence.** Setting this bit to 1b Indicates that the image in the Flash contains an EFI image. 1b = EEPROM word 33h (EFI version) is valid. 0b = No EFI image is contained. The default for this bit is 0b in order to be backwards compatible with existing systems already in the field. If this bit is set to 1b when PPB is set to 0b, it indicates that both images (PXE and EFI) are present in the Flash.
13	Rsvd	**Reserved.** This bit is reserved and should be set to 0b.
12	FDP	**Force Full Duplex[a].** This bit indicates the duplex mode. 1b = Full duplex. 0b = Half duplex. **NOTE:** This bit is a don't care unless bits the FSP field (bits 11:10) are set.
11:10	FSP	**Force Speed[a].** These bits determine speed. 00b = Speed is determined through auto-Negotiation. 01b = 10 Mbps 10b = 100 Mbps 11b = Invalid value. **NOTE:** If these bits are not set, bit 12 is a don't care bit.
9	LWS	**Legacy OS Wakeup Support (for 82559-based adapters only).** If this bit is set to 1b, the agent enables PME in the adapter's PCI configuration space during initialization. This allows remote wakeup under legacy operating systems that don't normally support it. 1b = Enabled. 0b = Disabled (default). **NOTE:** Enabling this bit makes the network controller technically non-compliant with the ACPI specification.
8	DSM	**Display Setup Message.** If this bit is set to 1b, the "Press Control-S" message appears after the title message. The default for this bit is 1b.
7:6	PT	**Prompt Time.** These bits control how long the "Press Control-S" setup prompt message appears if it is enabled by DIM. 00b = 2 seconds (default). 01b = 3 seconds. 10b = 5 seconds. 11b = 0 seconds. **NOTE:** The Control-S message does not appear if 0 seconds prompt time is selected.

Table 25. Boot Agent Main Setup Options

Bit	Name	Description
5	LBS	Local Boot Selection (OBSOLETE). In previous versions of the agent, this bit enables or disables local boot if the DBS bit selects it. The default for this bit is 1b, enable local booting. The boot agent no longer uses this bit at runtime.
4:3	DBS	**Default Boot Selection.** These bits select the default boot device. These bits are only used if the agent detects that the BIOS does not support boot order selection or if the MODE field of word 31h is set to MODE_LEGACY. 00b = Network boot, then local boot. 01b = Local boot, then network boot. 10b = Network boot only. 11b = Local boot only.
2	BBS	BIOS Boot Specification (OBSOLETE). In previous versions of the agent, this bit enables or disables use of the BBS to determine boot order. If set to 1, the BIOS boot order is used, and the DBS bits are ignored. The boot agent at runtime no longer uses this bit. The runtime checks for BBS/PnP and the setting in the MODE field of word 31h are used instead.
1:0	PS	**Protocol Select.** These bits select the boot protocol. 00b = PXE (default). 01b = RPL protocol. 10b = Undefined. 11b = Undefined.

a. This setting only applies to the Boot Agent software.

2.6.2 Boot Agent Configuration Customization Options (Word 31h)

Word 31h contains settings that can be programmed by an OEM or network administrator to customize the operation of the software. These settings cannot be changed from within the Control-S setup menu or the Intel Boot Agent (IBA) utility. The lower byte contains settings typically configured by a network administrator using the Intel Boot Agent utility. These settings control which setup menu options are changeable. The upper byte is generally settings used by an OEM to control the operation of the agent in a LOM environment, although there is nothing in the agent to prevent their use on a NIC implementation.

Table 26. Boot Agent Configuration Customization Options (Word 31h)

Bit	Name	Description
15:14	SIG	**Signature.** These bits must be set to 01b to indicate that this word has been programmed by the agent or other configuration software.
13:11	Rsvd	**Reserved.** This field is reserved and these bits should be set to 0b.
10:8	MODE	**Mode.** This field selects the agent's boot order setup mode. It changes the agent's default behavior in order to make it compatible with systems that do not completely support the BBS and PnP Expansion ROM standards. Valid values and their meanings are: 000b = Normal behavior. The agent attempts to detect BBS and PnP Expansion ROM support as it normally does. 001b = Force Legacy mode. The agent does not attempt to detect BBS or PnP Expansion ROM supports in the BIOS and assumes the BIOS is not compliant. The BIOS boot order can be changed in the Setup Menu. 010b = Force BBS mode. The agent assumes the BIOS is BBS-compliant, even though it may not be detected as such by the agent's detection code. The BIOS boot order CANNOT be changed in the Setup Menu. 011b = Force PnP Int18 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 18h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order CANNOT be changed in the Setup Menu. 100b = Force PnP Int19 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 19h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order CANNOT be changed in the Setup Menu. 101b = Reserved. If specified, treated as value 000b. 110b = Reserved. If specified, treated as value 000b. 111b = Reserved. If specified, treated as value 000b.
7:6	Rsvd	**Reserved.** This field is reserved and these bits should be set to 0b.
5	DFU	**Disable Flash Update.** 1b = No updates to the Flash image using PROSet are allowed. 0b = Flash image updates using PROSet are allowed (default).
4	DLWS	**Disable Legacy Wakeup Support.** 1b = No updates to the Legacy OS Wakeup support menu option are allowed. 0b = Updates to the Legacy OS Wakeup support menu option are allowed (default).

Table 26. Boot Agent Configuration Customization Options (Word 31h)

Bit	Name	Description
3	DBS	**Disable Boot Selection.** 1b = No changes to the boot order menu option are allowed. 0b = Boot order menu option changes are allowed (default).
2	DPS	**Disable Protocol Select.** 1b = No changes to the boot protocol are allowed. 0b = Changes to the boot protocol are allowed (default).
1	DTM	**Disable Title Message.** 1b = The title message displaying the version of the boot agent is suppressed. The Control-S message is also suppressed. This is for OEMs who do not wish the boot agent to display any messages at system boot. 0b = The title message that displays the version of the boot agent and the Control-S message is allowed (default).
0	DSM	**Disable Setup Menu.** 1b = The setup menu cannot be invoked by pressing Control-S. This is not allowed. In this case, the EEPROM can only be changed through an external program. 0b = The setup menu can be invoked by pressing Control-S (default).

2.6.3 Boot Agent Configuration Customization Options (Word 32h)

Word 32h is used to store the version of the boot agent that is stored in the Flash image. When the boot agent loads, it can check this value to determine if any initial (or first time) configuration needs to be performed. The agent then updates this word with its version. Some diagnostic tools to report the version of the Boot Agent in the Flash also read this word. This word is only valid if the PPB is set to 0b. Otherwise, the contents may be undefined.

Table 27. Boot Agent Configuration Customization Options (Word 32h)

Bit	Name	Description
15:12	MAJOR	PXE boot agent major version. The default for these bits is 0b.
11:8	MINOR	PXE boot agent minor version. The default for these bits is 0b.
7:0	BUILD	PXE boot agent build number. The default for these bits is 0b.

2.6.4 IBA Capabilities (Word 33h)

Word 33h is used to enumerate the boot technologies that have been programmed into the Flash. It is updated by IBA configuration tools and is not updated or read by IBA.

Table 28. IBA Capabilities

Bit	Name	Description
15:14	SIG	Signature. These bits must be set to 01b to indicate that this word has been programmed by the agent or other configuration software.
13:5	Rsvd	Reserved. This field is reserved and these bits should be set to 0b.
4	SAN	SAN capability is present in Flash. 0b = The SAN capability is not present (default). 1b = The SAN capability is present.
3	EFI	EFI UNDI capability is present in Flash. 0b = The RPL code is not present (default). 1b = The RPL code is present.
2	RPL	RPL capability is present in Flash. 1b = The RPL code is present (default). 0b = The RPL code is not present.
1	UNDI	PXE/UNDI capability is present in Flash. 1b = The PXE base code is present (default). 0b = The PXE base code is not present.
0	BC	PXE base code is present in Flash. 0b = The PXE base code is present (default). 1b = The PXE base code is not present.

2.7 Checksum

The Checksum word is calculated by adding all of the EEPROM words (00h through FFh, based on a 256-register EEPROM), including the Checksum word itself. The sum should equal BABAh. The initial value before the values are added together should be 0000h, and the carry bit should be ignored after each addition. This checksum can be located at 3Fh or FFh depending on the size of the EEPROM.

Note: This page left intentionally blank.

Appendix A ICH5 EEPROM Contents

This appendix contains a sample of raw EEPROM contents for the ICH5. All values for these images are hexadecimal.

Table 29. ICH5 EEPROM Contents

Word	Description
00:02h	Ethernet Individual Address
03h	Compatibility Bytes
05h	Controller and Connector Type
06h	PHY Device Record
08:09h	PWA Bytes
0Ah	EEPROM ID
0Bh	Subsystem ID
0Ch	Subsystem Vendor ID
0Dh	SMB Address Field
23h	ICH5 Device ID
3Fh	Checksum for 64-word EEPROM
FFh	Checksum for 256-word EEPROM

A.1 82562GT/ET EEPROM Image with ICH5

Note: "XXXX" denotes the Individual Address, "YYYY" denotes the checksum, and "ZZZZ" is the Subsystem ID field and "WWWW" is the Subvendor ID field.

```
XXXX XXXX XXXX 1A03 0000 0201 4701 0000

0000 0000 49A2 ZZZZ WWWW 007F 0000 0000

0000 0000 0000 0000 0000 0000 0000 0000

0000 0000 0000 0000 0000 0000 0000 0000

0000 0000 0000 1050 0000 0000 0000 0000

0000 0000 0000 0000 0000 0000 0000 0000

002C 0000 0000 0000 0000 0000 0000 0000

0000 0000 0000 4030 0000 0000 0000 YYYY
```

A.2 82562EM EEPROM Image with ICH5

Note: "XXXX" denotes the Individual Address, "YYYY" denotes the checksum, and "ZZZZ" is the Subsystem ID field and "WWWW" is the Subvendor ID field.

```
XXXX XXXX XXXX 1A13 0000 0201 4701 0000
0000 0000 49A2 ZZZZ WWWW 8064 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 1052 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
002C 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 4030 0000 0000 0000 0000
0044 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
```

```
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 YYYY
```

A.3 82562EP EEPROM Image with ICH5

Note: "XXXX" denotes the Individual Address, "YYYY" denotes the checksum, and "ZZZZ" is the Subsystem ID field and "WWWW" is the Subvendor ID field.

```
XXXX XXXX XXXX 1A03 0000 0210 4C01 0000
0000 0000 49A2 ZZZZ WWWW 8064 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 1054 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
002C 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 4030 0000 0000 0000 0000
0044 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
```

```
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 YYYY
```

A.4 82562GZ/EZ EEPROM Image with ICH5

Note: "XXXX" denotes the Individual Address, "YYYY" denotes the checksum, and "ZZZZ" is the Subsystem ID field and "WWWW" is the Subvendor ID field.

```
XXXX XXXX XXXX 1A03 0000 0201 4701 0000
0000 0000 49A2 ZZZZ WWWW 8064 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 1050 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
002C 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 4030 0000 0000 0000 YYYY
```

A.5 82562GX/EX EEPROM Image with ICH5

Note: "XXXX" denotes the Individual Address, "YYYY" denotes the checksum, and "ZZZZ" is the Subsystem ID field and "WWWW" is the Subvendor ID field.

```
XXXX XXXX XXXX 1A03 0000 0210 4C01 0000
0000 0000 49A2 ZZZZ WWWW 007F 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 1052 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
```

```
002C 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 4030 0000 0000 0000 0000
0044 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 YYYY
```

Note: This page intentionally left blank.

Appendix B ICH6 and ICH7 EEPROM Contents

This appendix contains a sample of raw EEPROM contents for the ICH6 and ICH7. All values for these images are hexadecimal.

Table 30. ICH6 and ICH7 EEPROM Contents

Word	Description
00:02h	Ethernet Individual Address
03h	Compatibility Bytes
05h	Controller and Connector Type
06h	PHY Device Record
08:09h	PWA Bytes
0Ah	EEPROM ID
0Bh	Subsystem ID
0Ch	Subsystem Vendor ID
0Dh	SMB Address Field
23h	ICH6 Device ID
3Fh	Checksum for 64-word EEPROM
FFh	Checksum for 256-word EEPROM

B.1 82562EZ/ET and 82562EX/EP/EM EEPROM Starter Image with ICH6 and ICH7

Note: "YYYY" denotes the Device ID (see Table 19 and Table 21 for details).

```
0000 0000 0000 1A13 0000 0201 4701 0000

0000 0000 69B2 0001 8086 007F FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF YYYY FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

0000 0000 0000 FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF 0000 FFFF FFFF FFFF 0000
```

B.2 82562GX/EX EEPROM Image with ICH6 and ICH7 (With Manageability)

Note: "YYYY" denotes the Device ID (see Table 19 and Table 21 for details).

```
0700 00E9 6805 1313 0000 1013 4701 0000
0000 0000 69B2 1091 8086 007F FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF YYYY FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
0000 0000 0000 FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF 0000 FFFF FFFF FFFF FFFF
0088 8803 0200 0088 8801 0400 FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
0488 0404 0488 0202 0488 0101 FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
6F07 1804 FF10 0003 6F01 1803 FF10 0000
6F05 1800 FF10 0000 FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```

```
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```

B.3 82562GT/ET EEPROM Image with ICH6 and ICH7 (Without Manageability)

Note: "XXXX" denotes the Individual Address. "YYYY" denotes the Device ID (see Table 19 and Table 21 for details).

```
FFFF FFFF FFFF 1313 0000 1035 4701 0000

0000 0000 49B2 27DC 8086 007F FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF YYYY FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

0000 0000 0000 FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF 0000 FFFF FFFF FFFF XXXX
```

B.4 82562GX/EX EEPROM Image with ICH6 and ICH7 (Without Manageability)

Note: "XXXX" denotes the Individual Address. "YYYY" denotes the Device ID (see Table 19 and Table 21 for details).

```
FFFF FFFF FFFF 1313 0000 1053 4701 0000

0000 0000 49B2 1091 8086 007F FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF YYYY FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

0000 0000 0000 FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF 0000 FFFF FFFF FFFF XXXX
```

B.5 82562G/ET EEPROM Image with ICH6 and ICH7 (Without Manageability)

Note: "XXXX" denotes the Individual Address. "YYYY" denotes the Device ID (see Table 19 and Table 21 for details).

```
FFFF FFFF FFFF 1313 0000 1011 4701 0000

0000 0000 49B2 1094 8086 007F FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF YYYY FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

0000 0000 0000 FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF 0000 FFFF FFFF FFFF XXXX
```

B.6 82552V EEPROM Image with NM10 Express Chipset

Note: "XXXX" denotes the Individual Address, "YYYY" denotes the checksum, and "ZZZZ" is the Subsystem ID field and "WWWW" is the Subvendor ID field.

```
XXXX XXXX XXXX 1B13 0000 1021 4701 0000

0000 0000 49B2 0000 8086 007F FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF 10FE FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

0100 4000 4202 4003 FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```