Intel® E7500 Chipset MCH Intel®x4 Single Device Data Correction (x4 SDDC) Implementation and Validation

Application Note (AP-726)

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Revision History

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1. Overview

The Intel® E7500 Chipset MCHs support Intel® x4 Single Device Data Correction (x4 SDDC). x4 SDDC provides S4EC-D4ED (Single x4 Error Correction-Double x4 Error Detection). This document covers the Intel® E7500 MCH specific implementation and validation.

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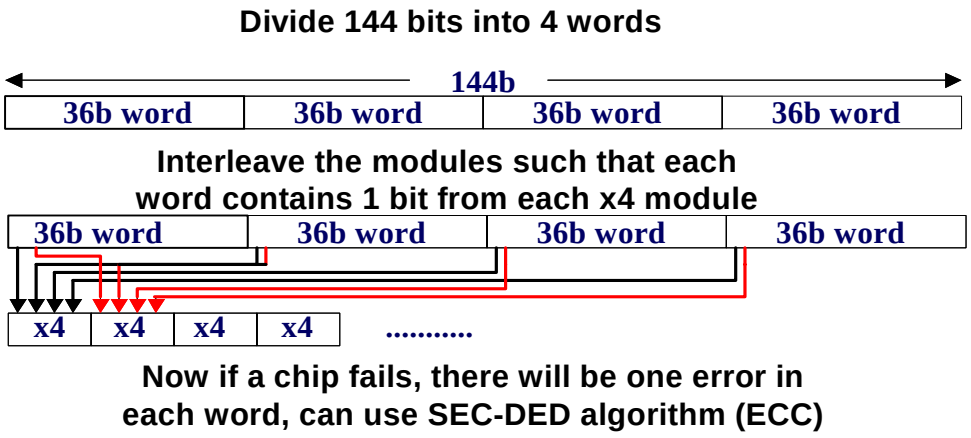
2. Intel® Single Device Data Correction (SDDC) Algorithm

The x4 SDDC is an ECC algorithm designed to recover from a single DRAM chip failure of the data signals. x4 SDDC can be configured to correct errors in x4 chips or to correct in x8 chips. Data or data pin errors in the same chip are correctable. Double errors across two chips are detectable. The SxEC-DxED algorithm is similar to SEC-DED (x = number of bits, 4 or 8). Below is a x4 SDDC example of how bits are organized into words that will contain at most a single bit error in the case of a single device failure.

Figure 1. Example of x4 Interleaved Approach



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3. Intel® E7500 Chipset MCH x4 Intel® SDDC Technology Implementation

The Intel® E7500 Chipset MCH use the x4 SDDC implementation that allows the memory system to detect and correct 1 to 4-bit internal data and data pin failures within one DDR memory device and detect up to 8-bit internal data and data pin failures within two DDR memory devices. This implementation is designed to recover from faults that are contained within a single DDR memory device that do not impact other DDR memory devices in the memory system. This implementation cannot tolerate the failure of control signals or the failure to properly complete the JEDEC Mode Register Set (MRS) initialization of the DDR memory device.

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4. Testing Intel® x4 SDDC Corrections on the Intel® E7500 Chipset MCH

Two sets of tests can safely validate the operation of the Intel® E7500 Chipset MCH x4 SDDC logic, an Open Circuit Test and a Short to Ground Test. These two tests can be executed in the following sequence using two "sacrificial" DIMMs built using 66-pin TSOP x4 DDR memory devices. Once done with these tests, the "sacrificial" DIMMs represent two worst-case scenarios (all-open and all-short-to-ground) and they can be used to validate the x4 SDDC operation in additional systems.

A. Open Circuit Test:

1. Select any memory device on the DIMM to be used for the test
2. Open circuit DQ0 pin 5 of the selected memory device by lifting it from the PCB pad
3. Ensure the system boots and runs with the modified DIMM
4. Open circuit DQ1 pin 11 of the selected memory device by lifting it from the PCB pad
5. Ensure the system boots and runs with the modified DIMM
6. Open circuit DQ2 pin 56 of the selected memory device by lifting it from the PCB pad
7. Ensure the system boots and runs with the modified DIMM
8. Open circuit DQ3 pin 62 of the selected memory device by lifting it from the PCB pad
9. Ensure the system boots and runs with the modified DIMM

B. Short Circuit to Ground Test:

1. Select any memory device on the DIMM to be used for the test
2. Short circuit DQ0 pin 5 of the selected memory device by connecting it ground
3. Ensure the system boots and runs with the modified DIMM
4. Short circuit DQ1 pin 11 of the selected memory device by connecting it ground
5. Ensure the system boots and runs with the modified DIMM
6. Short circuit DQ2 pin 56 of the selected memory device by connecting it ground
7. Ensure the system boots and runs with the modified DIMM
8. Short circuit DQ3 pin 62 of the selected memory device by connecting it ground
9. Ensure the system boots and runs with the modified DIMM