



82551QM/ER/IT EEPROM Map and Programming Information

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Contents

1.0	Introduction and Scope	1
1.1	Component Identification Via Programming Interface.....	1
1.2	EEPROM Device and Interface.....	2
1.3	EEPROM Programming Procedure Overview	2
2.0	82551 EEPROM Format and Contents.....	3
2.1	82551QM EEPROM Address Map.....	3
2.2	82551ER/IT EEPROM Address Map	4
2.3	Ethernet Individual Address (Words 00h:02h)	5
2.4	Compatibility Field (Word 03h).....	6
2.5	Hardware Description Fields	7
2.5.1	Reserved Word (04h)	7
2.5.2	Controller Type (Word 05h, High Byte).....	7
2.5.3	Connector Types (Word 05h, Low Byte).....	7
2.5.4	PHY Device Records (Words 06h, 07h)	8
2.5.5	Printed Wire Assembly Number (Words 08h, 09h).....	8
2.6	Product Identification.....	8
2.6.1	EEPROM ID (Word 0Ah)	8
2.6.2	Product Identification (Words 0Bh, 0Ch)	12
2.6.3	82551QM AoL Configuration (Word 0Dh).....	13
2.6.4	EEPROM Security Integrity (Words 0Eh, 0Fh)	14
2.6.5	82551ER/IT Reserved Words (10h:22h)	14
2.6.6	82551QM (Words 10h:14h)	15
2.6.7	82551QM AoL 2 SMBus Polling Descriptors (Words 15h:1Ch).....	15
2.6.8	81552QM AoL 2 RESET Descriptor (Words 1Dh, 1Eh)	15
2.6.9	82551QM AoL 2 Registers CRC (Word 1Fh, Bits 7:0)	16
2.6.10	82551QM Reserved (Words 20h:22h).....	16
2.6.11	82551IT/ER Reserved (Words 23h:2Fh)	16
2.6.12	82551QM PCI Device ID (Word 23h)	16
2.6.13	82551QM Reserved (Words 24h:2Fh).....	16
2.6.14	82551QM Boot Agent Main Setup Options (Word 30h).....	16
2.6.15	82551QM Boot Agent Configuration Customization Options (Word 31h).....	18
2.6.16	82551QM Boot Agent Configuration Customization Options (Word 32h).....	19
2.6.17	82551QM IBA Capabilities (Word 33h).....	20
2.6.18	Reserved (Words 34h:3Eh)	20
2.6.19	Checksum Word Calculation (Word 3Fh)	20
2.6.20	82551ER/IT Reserved (Words 40h:FEh).....	20
2.6.21	81551QM AoL Heartbeat Packet (Words 40h:F5h).....	20
2.6.22	82551QM Heartbeat Packet Structure within the EEPROM (Word F6h:FAh)	21
2.6.23	82551QM Modem Configuration (Words FBh:FEh).....	22
2.6.24	Checksum Word Calculation (Word FFh)	22



A	EEPROM Contents	23
A.1	82551QM Ethernet Controller EEPROM Image	23
A.2	82551QM EEPROM Image with Basic AoL.....	23
A.3	82551QM EEPROM Image with Advanced AoL	25
A.4	82551QM LOM EEPROM Image with Basic AoL.....	26
A.5	82551QM LOM EEPROM Image with Advanced AoL.....	27
A.6	82551ER/IT EEPROM Image.....	29

Revision History

Revision	Revision Date	Description
1.3	August 2009	Updated sections 1.0, 1.4, and 1.5.
1.2	November 2008	Updated sections 2.6.14 through 2.6.17.
1.1	March 2008	Added new Intel logo. Updated sections 2.1, 2.2, and A.1 through A.6. Updated Table 13 through 16.
1.0	October 2004	Initial release White Cover Confidential (WCC)



1.0 Introduction and Scope

This application note describes the 82551QM/ER/IT EEPROM and its contents. The EEPROM is used for hardware and software configuration and is read by software to determine specific design features.

Note: The 82551QM Fast Ethernet PCI controller supports bi-directional ASF or the Total Cost of Ownership (TCO) interface that enables a connection with alerting and management controllers such as the Intelligent Platform Management Interface (IPMI) solutions and Baseboard Management Controllers (BMCs). 82551ER/IT Fast Ethernet PCI controllers DO NOT support ASF or TCO.

Unless otherwise specified, all numbers in this document use the following numbering convention:

- Numbers with a suffix of “b” are binary (base 2).
- Numbers without a suffix are decimal (base 10).
- Numbers with a suffix of “h” are hexadecimal (base 16).

1.1 Component Identification Via Programming Interface

82551QM/ER/IT controller stepping is identified by the following register contents.

Table 1. Component Identification

Stepping	Vendor ID	Device ID	Revision Number
82551QM - A1	8086h	1229h (deskside/server) 1059h (mobile)	
82551ER - A0	8086h	1209h	
82551IT - A0	8086h	1209h	

Note: These devices also provide identification data through the Test Access Port (TAP).



1.2 EEPROM Device and Interface

The serial EEPROM is a 3.3 volt 9346 or 9366 Microwire* device that stores configuration data for the 82551QM/ER/IT controller. The controller supports 64-word or 256-word sized EEPROMs.

In 82551QM Alert on LAN* (AoL) enabled systems, the 256-word (16 bits per register) EEPROM device is required. In PCI designs that do not use AoL functionality, the 82551QM/ER/IT controller only requires an EEPROM that contains 64 registers of 16 bits per register. The 82551QM/ER/IT controller auto-detects the EEPROM size via a dummy zero mechanism following reset.

All read and write accesses are preceded by a command instruction to the EEPROM. The command instructions begin with a logical one (1) as a start bit, two opcode bits (read, write, erase, etc.), and six address bits. The address field is six bits for a 64-register EEPROM. A dummy zero bit from the EEPROM indicates the end of the address field. This indicates that the entire address field has been transferred to the EEPROM. A command is issued by asserting the EEPROM Chip Select (EECS) signal from the controller and clocking the data out of the EEPROM Data Input (EEDI) pin into the EEPROM on its data input pin relative to the EEPROM Shift Clock (EESK) controller output. The EECS signal is de-asserted after the EEPROM cycle completes (command, address and data).

In designs employing the 64-register EEPROM, the EEPROM read is approximately 6,000 clock cycles long (180 microseconds at 33 MHz). The system is required to provide a valid clock on the Clock (CLK) pin for this time period after de-asserting the Reset pin (RST#), even if the Isolate pin (ISOLATE#) is asserted (the CLK input is not isolated until the EEPROM accesses are complete).

The controller reads several words from the EEPROM after a PCI reset. The number of words read depends on the configuration of the device.

1.3 EEPROM Programming Procedure Overview

A device based on the 82551QM/ER/IT controller EEPROM can be programmed in-line at a Final Acceptance Test (FAT) station. This allows the use of a surface mount technology (SMT) EEPROM, which is otherwise difficult to handle with off-line automated programming equipment. The Bill of Materials (BOM) for an 82551 controller-based solution requires a blank EEPROM; type 93C66 for TCO enabled systems (82551QM only) or a type 93C46). The image programmed into the EEPROM is specified by two controlled documents:

1. 82551QM/ER/IT EEPROM Map and Programming Information Application Note (*this document*).
2. A program file that is unique for each Printed Board Assembly (PBA) and contains the default EEPROM values for that particular PBA.

Note: This unique program file can be created using a simple text editor that follows the example format shown in Appendix A, "EEPROM Contents".

EEPROMs may be pre-programmed prior to their being soldered onto a board. Some LAN on Motherboard (LOM) designers may prefer this method over in-line programming.

The EEPROM image consists of two types of data: static data, which is fully described by this document, and dynamic (or serialized) data, which varies for each unit programmed. The dynamic data consists of the product's Ethernet Individual Address (IA) and the EEPROM checksum.



2.0 82551 EEPROM Format and Contents

Section 2.1 and Section 2.2 list the EEPROM address maps for the 82551QM and 82551ER/IT Fast Ethernet PCI controllers. Each word listed is described in the sections that follow the EEPROM address maps.

2.1 82551QM EEPROM Address Map

Table 2 lists the EEPROM address map for the 82551QM Fast Ethernet PCI controller.

Table 2. 82551QM EEPROM Address Map

Word	High Byte (Bits 15:8)	Low Byte (Bits 7:0)
00h	Ethernet Individual Address Byte 2	Ethernet Individual Address Byte 1
01h	Ethernet Individual Address Byte 4	Ethernet Individual Address Byte 3
02h	Ethernet Individual Address Byte 6	Ethernet Individual Address Byte 5
03h	Compatibility Byte 1	Compatibility Byte 0
04h	Reserved	
05h	Controller Type	Connectors
06h	Primary PHY Record, high byte	Primary PHY Record, low byte
07h	Secondary PHY Record, high byte	Secondary PHY Record, low byte
08h	PWA Byte 1	PWA Byte 2
09h	PWA Byte 3	PWA Byte 4
0Ah	EEPROM_ID, high byte	EEPROM_ID, low byte
0Bh	Subsystem_ID, high byte	Subsystem_ID, low byte
0Ch	Subsystem_Vendor, high byte	Subsystem_Vendor, low byte
0Dh	Configuration and Heartbeat Pointer	SMBus Address/CIS Pointer
0Eh:0Fh	Reserved	
10:22h	Controlled by Alert on LAN (AoL) Software	
23h	Device ID, high byte	Device ID, low byte
24h:2Fh	Reserved	
30h:33h	Intel Boot Agent Configuration	
34h:3Eh	Reserved	
3Fh	64-word EEPROM Checksum, high byte	64-word EEPROM Checksum, low byte
40h:F7h	Controlled by ASF Software	
F8h	Reserved	AoL Time Stamp Offset
F9h	Reserved	AoL Sequence Offset
FAh	Reserved	AoL Event Data Offset
FBh	Modem Vendor ID, high byte	Modem Vendor ID, low byte
FCh	Modem Device ID, high byte	Modem Device ID, low byte

**Table 2. 82551QM EEPROM Address Map (Continued)**

Word	High Byte (Bits 15:8)	Low Byte (Bits 7:0)
FDh	Modem Programming Interface	Modem Revision ID
FEh	Modem Power Dissipation	Modem Power Consumption
FFh	256-word EEPROM Checksum, high byte	256-word EEPROM Checksum, low byte

2.2 82551ER/IT EEPROM Address Map

Table 3 lists the EEPROM address map for the 82551ER/IT Fast Ethernet PCI controller.

Table 3. 82551ER/IT EEPROM Address Map

Word	High Byte (Bits 15:8)	Low Byte (Bits 7:0)
00h	Ethernet Individual Address Byte 2	Ethernet Individual Address Byte 1
01h	Ethernet Individual Address Byte 4	Ethernet Individual Address Byte 3
02h	Ethernet Individual Address Byte 6	Ethernet Individual Address Byte 5
03h	Compatibility Byte 1	Compatibility Byte 0
04h	Reserved	
05h	Controller Type	Connectors
06h	Primary PHY Record, high byte	Primary PHY Record, low byte
07h	Secondary PHY Record, high byte	Secondary PHY Record, low byte
08h	PWA Byte 1	PWA Byte 2
09h	PWA Byte 3	PWA Byte 4
0Ah	EEPROM_ID, high byte	EEPROM_ID, low byte
0Bh	Subsystem_ID, high byte	Subsystem_ID, low byte
0Ch	Subsystem_Vendor, high byte	Subsystem_Vendor, low byte
0Dh	Reserved (set to 0000h)	
0Eh:3Eh	Reserved	
3Fh	64-word EEPROM Checksum, high byte	64-word EEPROM Checksum, low byte
40h:FEh	Reserved	
FFh	256-word EEPROM Checksum, high byte	256-word EEPROM Checksum, low byte



2.3 Ethernet Individual Address (Words 00h:02h)

Ethernet Individual Address (IA) is a 6-byte field that must be unique for each NIC or LOM system. The first three bytes are vendor specific and the last three bytes must be unique for each copy of the EEPROM. Although the Intel default value is shown in [Table 4](#), it is anticipated that OEM versions of the product may be required to have non-Intel ID's.

Individual Address (IA) bytes read from the EEPROM are used by the controller until an IA Setup command is issued by software. The IA defined by the IA Setup command overrides the IA read from the EEPROM.

Note: The Ethernet Individual Address is byte swapped.

Table 4. Ethernet Individual Address

		Individual Address Byte / Value					
		Word 00h		Word 01h		Word 02h	
Manufacturer	MAC Address	Byte 1	Byte 0	Byte 1	Byte 0	Byte 1	Byte 0
Intel	00AA00xxyyzz	AA	00	xx	00	zz	yy
Intel	00A0C9xxyyzz	A0	00	xx	C9	zz	yy
Intel	009027xxyyzz	90	00	xx	27	zz	yy
Intel	0002B3xxyyzz	02	00	xx	B3	zz	yy



2.4 Compatibility Field (Word 03h)

Intel reserves one word in the EEPROM image for compatibility purposes. Bits within this field may be defined, if needed, to resolve software compatibility issues with various hardware revisions. These bits are initialized during manufacturing and should be treated as read-only by software.

Table 5. Compatibility Field

Bit	Name	Description
15:12	Reserved	Reserved for future use. Set these bits to 0b.
11	LOM	LAN on Motherboard This bit indicates that the 82551QM/ER/IT controller is embedded on the motherboard and permits features unique to LOM implementations. 0 = No LOM (default) 1 = LOM
10	SRV	Server Bit This bit indicates to the software that the 82551QM/ER/IT is a server NIC and that server extensions are allowed. 0 = Disables server extensions (default). 1 = Enables server extensions
9	CLI	Client Bit This bit indicates that the 82551QM/ER/IT controller is a client NIC and that client-only NIC features are permitted. 0 = Server NIC features 1 = Client NIC features (default)
8	OEM	OEM Bit This bit allows software to examine the Subsystem_Vendor and Subsystem_ID fields for OEM information. 0 = Intel product (default) 1 = OEM product
7	AUTO SWITCH ENABLE	MDI/MDI-X Auto Switching Enables the MDI/MDI-X auto-switching feature. 0 = Disabled (default) 1 = Enabled
6:5	Reserved	Reserved for future use. Set these bits to 0b.
4	SMB	System Management Bus (SMBus) to Motherboard (82551QM only) This bit indicates if the 82551QM controller's SMBus alert signal is connected to the motherboard for alerting with the ICH2 or ICH3. Set this bit as follows: 0 = SMBus not connected (default). 1 = SMBus connected. Note: For the 82551ER/IT, always set this bit to 0b.
3	AOL2	AoL 2 ASIC Present This bit indicates whether or not an external AoL 2 ASIC or ASF Controller (82551QM only) is present and connected to the system's main SMBus. This allows for future AoL 2 implementations to be used. 0 = AoL 2 ASIC is not present (default). 1 = AoL 2 ASIC is present. Note: The 82551ER/IT controller does not support bi-directional ASF.

**Table 5. Compatibility Field**

Bit	Name	Description
2	BOB	PCI Bridge On Board This bit allows software to determine if a NIC or LOM system has a PCI bridge without scanning the PCI bus or relying on the Subsystem ID. It is required when PCI bus scans are not allowed (such as configuration) and for OEM Subsystem ID. 0 = NIC/LOM does not have a PCI bridge (default). 1 = NIC/LOM has a PCI bridge.
1	MC10	Multicast Workaround 10 Mb/s 0 = Bypass 10 multicast workaround. 1 = Do not bypass 10 multicast workaround (default).
0	MC100	Multicast Workaround 100 Mb/s 0 = Bypass 100 multicast workaround 1 = Do not bypass 100 multicast workaround (default).

2.5 Hardware Description Fields

The hardware description fields of the EEPROM detail the component configuration for the product (design). Intel supplied drivers and the controller use these fields to determine the NIC or LOM system configuration.

2.5.1 Reserved Word (04h)

This word is reserved and should be set to zero (0). However, it may also be left unprogrammed (FFFFh).

2.5.2 Controller Type (Word 05h, High Byte)

This byte wide field indicates which Intel Fast Ethernet controller (82550, 82551, 82557, 82558, or 82559) is installed and provides an additional means of differentiating the controllers alternative to the PCI Revision ID field.

Table 6. Controller Type

Controller Description	Controller Type
82550	02h
82551	02h
82557	01h
82558 (82557 compatible by default)	02h
82559 (82557 compatible by default)	02h

2.5.3 Connector Types (Word 05h, Low Byte)

This byte identifies the connector types installed on the product (for the RJ-45, set this byte to 01h).



2.5.4 PHY Device Records (Words 06h, 07h)

The PHY device records are used to describe an external PHY. These words are used with the 82557 controller. Since the 82551 controller has an internal PHY, these words have limited relevance. In 82551QM/ER/IT controller-based designs, word 06h contains a value of 4701h, and word 07h is not used. These fields cannot be used for any other purpose.

2.5.5 Printed Wire Assembly Number (Words 08h, 09h)

This four-byte field holds the nine-digit Printed Wire Assembly (PWA) number and allows identification of the exact revision level of a product¹. A network driver should not rely on this field to identify the product or its capabilities.

Note: Customers can use these words for non-standard manufacturing use.

2.6 Product Identification

2.6.1 EEPROM ID (Word 0Ah)

The 82551QM/ER/IT controller reads this register to obtain basic power-on configuration information. Note that the format for this word has undergone substantial change with each controller release (Refer to [Table 7](#)).

Word 0Ah is the only section of the EEPROM map that affects the basic functionality of the 82551QM/ER/IT controller. Although other fields within the EEPROM affect the controller, their impact is limited to the loading of values (such as the IA address).

Note: The Signature Bits (15:14) are used to indicate the word's validity. If the Signature Bits are set to 1b, then the word is valid and the remaining contents of the word are used to determine controller configuration. If the Signature Bits are set to 0b, then the remainder of this word is ignored and the 82551QM/ER/IT controller uses default values for its configuration.

1. Neither the dash nor the first digit of the three-digit suffix is stored.



Table 7. EEPROM ID (Word 0Ah)

Bit	Field Name	Description
15:14	SIG	Signature Bits The default configuration values are: • Modem is disabled (82551QM only). • Revision ID is 1b (default) • Standby mode is enabled. • Wake on LAN (WoL) is enabled (82551QM only). • Deep power down is enabled (refer to the bit 6 description). • Boot ROM is disabled, and boot expansion ROM base address register is enabled. • The Subsystem ID and System Vendor ID are set to 0b. • The SMBus Address Pointer and Heartbeat Packet Pointer are set to 0b (82551QM only).
13	ID	Subsystem ID and Subsystem Vendor ID Usage This bit indicates how the Subsystem ID and the Subsystem Vendor ID within the PCI configuration space are loaded. If the controller detects the presence of a valid EEPROM (as indicated by a value of 1b in bits 15 and 14), then: • If ID bit equals 0b (default), then the PCI Device ID is loaded with the contents of word 23h, and the PCI Vendor ID is loaded with the contents of 8086h. • If ID bit equals 1b, then the PCI Device ID is loaded with the contents of word 23h, and the PCI Vendor ID is loaded with the value of word 0Ch.
12	UD	UNDI Disable This bit is used to disable or enable the integrated UNDI ROM support. 0 = Enable UNDI ROM support. 1 = Disable UNDI ROM support (default). Note: For the 82551ER/IT, always set this bit to 1b.
11	BD	Boot Disable If this bit equals 1b (default), the Expansion ROM Base Address Register (PCI Configuration space, offset 30h) is disabled and an expansion ROM window should not be requested. If this bit equals 0b, the Expansion ROM Base Address Register (PCI Configuration space, offset 30h) is enabled and an expansion ROM window should be requested. For the 82551QM, this bit should be set to 1b.
10:8	Alt Rev ID	Alternate Revision ID If this bit field equals 111b (default), then this ID is set as described in Section 2.6.2. The default value depends on the silicon revision. This field is the three least-significant bits of the 82551QM/ER/IT controller's Revision ID field in the Ethernet PCI configuration space. Note that the Revision ID field in the EEPROM is active only if the ID field (bit 13) is also set.
7	XTALOFF	Crystal Off on Force TCO Power-down Enable (82551QM only) If this bit is set to 1b, the 82551QM is capable of shutting down the crystal in the force TCO power-down state for lower power consumption. 0 = Crystal off on force TCO power-down disabled. 1 = Crystal off on force TCO power-down enabled (default). Note: This bit is reserved for the 82551ER/IT. Always set this bit to 1b.



Table 7. EEPROM ID (Word 0Ah) (Continued)

Bit	Field Name	Description
6	DDPD	Disable Deep Power Down This bit must be set to 1b if a TCO controller is used through the SMBus to permit receive functionality in all power states (82551QM only). 0 = Deep Power Down is enabled (default) in D3 state while power management is disabled. 1 = Deep Power Down is disabled in D3 state while power management is disabled. When the Intel AoL Software Development Kit (SDK) is used, this bit is controlled by the AoL software when the system transitions through the power states. Note: This bit should be set to 1b if a management controller (such as TCO) is being used through the SMBus since it requires receive functionality at all power states (82551QM only).
5	WOL	WoL (WoL) Mode (82551QM only) If WoL equals 1b, the 82551QM controller is capable of waking the system by asserting the Power Management Event signal (PME#) on receipt of a wake-up packet. If the 82551QM controller is in the D3 power state (not initialized) and PME# is asserted, then the 82551QM controller also asserts the Card Status Change signal (CSTCHG) for a minimum of 50 ms to provide a WoL signal to a WoL cable. WoL mode is only valid until the 82551QM controller receives a configuration or memory/IO cycle. If enabled, the 82551 controller enters WoL mode following an alternate reset. 0b = WoL mode not enabled. 1b = WoL mode enabled (default). Note: This bit is reserved for the 82551ER and 82551IT. Set this bit to 1b.
4	LEDMODE	LED Mode (82551QM only) This bit configures the functionality of the Speed and Link LED. The Activity LED functionality during the WoL mode is fixed (non-configurable) and is activated by transmission and reception of broadcast (JSL) or Individual Address match packets. For legacy mode operation: LEDMODE = 0b (default) Link LED Lit, link is valid. Not lit, link is invalid. Speed LED Lit, speed is 100 Mb/s. Not lit, speed is 10 Mb/s. For optional LED mode operation: LEDMODE = 1b Link LED Lit, link is valid at 10 Mb/s. Not lit, link is invalid. Speed LED Lit, link is valid at 100 Mb/s. Not lit, link is invalid. Note: This bit is reserved for the 82551ER and 82551IT. Set this bit to 0b.



Table 7. EEPROM ID (Word 0Ah) (Continued)

Bit	Field Name	Description
3	Reserved	Reserved for future use. Set this bit to 0b.
2	WMR	Wide Modem Reset Control (82551QM only) If WMR equals 1b, the 82551QM controller issues a reset to the modem whenever the PCI Reset is active or the modem is at the D0_u state. If WMR equals 0b (default), the 82551QM controller issues a reset to the modem through an extended PCI reset. In both cases, there is an additional source for the modem reset through the modem system control registers. Note: This bit is reserved for the 82551ER and 82551IT. Set this bit to 0b.
1	STB Ena	Standby Enable If this bit equals 1b (default), then the 82551 controller can recognize an idle state and enter standby mode. Note that some internal clocks are stopped for power saving purposes. If this bit equals 0b, then the idle recognition circuit is disabled and the 82551 controller remains in an active state. Note: The 82551 controller does not require a PCI clock signal in standby mode and always requests a PCI clock using the Clockrun mechanism.
0	MD	Modem (82551QM only) If the MD bit equals 0b (default), then the design is a single function LAN. If the MD bit equals 1b, a modem is attached to the 82551QM controller's local parallel port. Notes: • In a PCI system, this bit must be set to 0b. • When MD is enabled, Flash is not supported. As a result, Boot Disable (BD) should be active (disabled) when MD is enabled.



At power up, the 82551QM/ER/IT controller can map either the on-chip ROM or the external Flash as a BIOS extension. This is controlled through the UD (82551QM only) and BD bits in the EEPROM. Table 8 lists the possible configurations for the Modem (81551QM only), Boot ROM, and Flash.

Table 8. Modem Boot ROM and Flash Configuration

Boot Disable	UNDI Disable	Modem Enable	Expansion Enable	Local Port Interface	Boot ROM Mapping
1	x ^a	0	x	Flash	None
1	x	1	0	Modem	None
0	1	0	x	Flash	Flash
0	1	1	0	Modem	Flash
0	1	1	1	Flash	Flash
0	0	0	x	Flash	UNDI
0	0	1	0	Modem	UNDI
0	0	1	1	Flash	UNDI

a. An "x" = "don't care" state.

2.6.2 Product Identification (Words 0Bh, 0Ch)

The Product Identification fields provide optional "branding" space in which to identify an OEM vendor and product.

After a hardware reset is de-asserted, the 82551 controller automatically reads EEPROM words 0Ah through 0Ch (word 0Ah was described in Section 2.6.1).

The Subsystem ID field (0Bh) identifies the 82551 controller-based specific solutions implemented by the vendor and indicated in the Subsystem Vendor ID field.

The Subsystem Vendor ID field (0Ch) identifies the vendor of a 82551 controller-based solution. Its values are based upon the vendor's PCI Vendor ID, which is controlled by the PCI Special Interest Group (PCI-SIG) in accordance with PCI Specification, Revision 2.1.

Note: The Subsystem ID and Subsystem Vendor ID fields are implemented if they contain a value other than 0000h or FFFFh. Both fields are set to 0000h by default.



Note: Based on the contents of EEPROM word 0Ah, bits 15:13, the 82551QM/ER/IT controller's behavior at reset is described as follows.:

Table 9. Reset Behavior

Bits 15, 14 of Word 0Ah	Bit 13 of Word 0Ah	PCI Space Device ID	PCI Space Vendor ID	Revision ID ^a	Subsystem ID	Subsystem Vendor ID
11, 10, 00	Don't care	1229h/1059h (QM) 1209h (ER/IT)	8086h	Default	0000h	0000h
01	0	Word 23h	8086h	Default	Word 0Bh	Word 0Ch
01	1	Word 23h	Word 0Ch	• Bits 7:3 = Default Bits 7:3 • Bits 2:0 = Bits 10:8 of Word 0Ah	Word 0Bh	Word 0Ch

a. The Revision ID is subject to change according to the silicon stepping.

Table 9 indicates that if the controller detects the presence of a valid EEPROM (bits 15 and 14 = 1b and bit 13 is set to 1b, the values stored in EEPROM, words 23h (PCI Device ID) and 0Ch (Subsystem Vendor ID) are loaded into the Device ID and Vendor ID fields, respectively, in the PCI Configuration space. If bit 13 is set to 0b (cleared), then the Device ID is loaded from EEPROM word 23h, and the Vendor ID field in PCI Configuration space remains at the default value.

Between de-asserting reset and completing an automatic EEPROM read, the 82551QM/ER/IT controller will not respond to any PCI configuration cycles. If the 82551QM/ER/IT controller is accessed during this time, the device will not respond and additional PCI configuration retries will need to occur until the device is ready.

2.6.2.1 Subsystem ID (Word 0Bh)

This one-word (16-bit) field identifies the vendor product number. Intel generates this number for products that it creates. For OEM products, the number must be supplied and controlled by the OEM to avoid duplication. Refer to the Microsoft* *Specification for Use of PCI IDs with Windows* Operating Systems* for more details.

2.6.2.2 Subsystem Vendor ID (Word 0Ch)

This one-word (16-bit) field identifies the OEM vendor. The code used for a particular vendor is the same Vendor ID code as assigned by the PCI SIG. Refer to the Microsoft* *Specification for Use of PCI IDs with Windows* Operating Systems* for more details.

2.6.3 82551QM AoL Configuration (Word 0Dh)

This field is used to enable or disable Advanced AoL functionality. It should be set to 4464h to enable alerting or 007Fh to disable alerting. In systems using Basic AoL functionality, the AoL software configures this field to enable or disable alerting. A description of each field, SMB Address/CIS Pointer and Heartbeat Pointer (refer to Table 10).

Note: This word is reserved for the 82551ER/IT controller and must be set to 0000h.



In PCI systems, word 0Dh contains the System Management Bus (SMB) address where the 82551QM resides. In 82551QM CardBus systems, this field acts as the address pointer to the Card Information Structure (CIS), located in the EEPROM.

Table 10. 82551QM SMB Address, CIS Pointer & HB Packet Pointers

Bits	Field	Description
15	Reserved	Reserved for future use. Set this bit to 0b.
14	GCL Enable	GCL Enable This bit enables the 82551QM controller to perform several advanced manageability functions of the AoL 2 device. If this bit equals 1b, advanced manageability features are enabled. If this bit equals 0b (default), the 82551QM controller uses an external alert on LAN ASIC through the SMBus to perform management functions.
13:12	Reserved	Reserved for future use. Set these bits to 0b.
11:8	HB Pointer	This field contains the location of the heartbeat packet within the EEPROM. The pointers are expressed in a granularity of 16 words. If AoL is not used, these bits should be set to 0b (default). The contents of word 0Dh in the EEPROM image should equal x0xxh, where the value of "x" does not matter. For basic alert functionality these bits should initially be set to 0b (EEPROM word 0Dh contents equal x0xxh) since the AoL software configures this field. For advanced alert functionality using the 82551QM controller, these bits should be set to 0100b (in other words, EEPROM word 0Dh contents equal x4xxh).
7:0	SMBus Add/CIS Pointers	This is a multiplexed field. In a PCI system, this 8-bit field is the 82551QM controller's address on the SMBus. However, bit 7 is ignored. As a result, the address programmed into the EEPROM must be shifted right one bit. For example, address FEh is programmed as address 7Fh in bits 7:0. In a CardBus system, this field provides two four-bit pointers pointing to CIS information within the EEPROM. The pointers are expressed in a granularity of 16 words. A 0b value is used as a null pointer. The Ethernet CIS pointer resides in bits 3:0 and the modem CIS pointer resides in bits 7:4. For example, a value of 0180h equates to the LAN CIS being located in the EEPROM at address 01h and the modem CIS being located at address 80h.

Note: The IA read from the EEPROM is used by the 82551QM controller until an IA Setup command is issued by software. The IA defined by the IA Setup command overrides the IA read from the EEPROM.

2.6.4 EEPROM Security Integrity (Words 0Eh, 0Fh)

These words are reserved and should be set to zeros. However, they may also be left unprogrammed (FFFFh).

2.6.5 82551ER/IT Reserved Words (10h:22h)

These words are reserved and should be set to zeros (0). However, they may also be left unprogrammed (FFFFh).



2.6.6 82551QM (Words 10h:14h)

Note: The bits in these fields are configured by the AoL software using data extracted from the aolan.ini file. They do not need to be set by the OEM.

2.6.7 82551QM AoL 2 SMBus Polling Descriptors (Words 15h:1Ch)

Note: The bits in these fields are configured by the AoL software using data extracted from the aolan.ini file. They do not need to be set by the OEM.

The 82551QM controller polls up to four SMBus devices every five seconds. The EEPROM configuration in words 15h:1Ch specifies the SMBus address and register of the polled device, a mask to apply to the data read, and an event code to send in an alert packet if the masked data is non-zero. The format of a polled device descriptor is listed in [Table 11](#).

Table 11. 81551QM Polling Descriptor

Byte Number	
7:1	0
SMB Address ^a	Reserved
SMB Register ^b	
SMB Data Mask ^c	
SMB Event Code ^d	

- a. The SMB address of the external device
- b. The command (or register pointer) that the 82551QM controller should write before reading data.
- c. The mask to compare against the read data. This is a positive mask which does a logical AND against the read data.
- d. Code to be used in the alert packet when the read data poll reveals an alert to report.

2.6.8 81552QM AoL 2 RESET Descriptor (Words 1Dh, 1Eh)

Note: The bits in this field are configured by the AoL software using data extracted from aolan.ini file. They do not need to be set by the OEM.

Table 12. 82551QM AoL 2 RESET Descriptor

Bits	Field	Description/Function
15	PDPOL	This bit indicates the power-down polarity.
14:12	Reserved	Reserved for future use.
11:8	POWER DN BIT#	This field contains the encoded bit in the register that should be accessed for the power-down operation.
7	PUPOL	This bit indicates the power-up polarity.
6:4	POWER UP BIT#	This field contains the encoded bit in the register that should be accessed for the power-up operation.
3	RPOL	This bit is the reset polarity.
2:0	RESET BIT#	This field contains the encoded bit in the register that should be accessed for the reset operation.



2.6.9 82551QM AoL 2 Registers CRC (Word 1Fh, Bits 7:0)

Bits 7:0 of word 1Fh contain an 8-bit CRC for words 10h:1Eh (high-byte/low-byte). The CRC algorithm is documented in the SMBus 2.0 specification for the PEC byte. Bits 15:8 of word 1Fh are reserved.

2.6.10 82551QM Reserved (Words 20h:22h)

These words are reserved and should be set to zeros. However, they may also be left unprogrammed (FFFFh).

2.6.11 82551IT/ER Reserved (Words 23h:2Fh)

These words are reserved and should be set to zeros. However, they may also be left unprogrammed (FFFFh).

2.6.12 82551QM PCI Device ID (Word 23h)

This word was added to the EEPROM auto-read after reset to allow the EEPROM programmer to be able to change the device ID. If the EEPROM is missing or invalid, then the device ID defaults to 1229h/1059h.

2.6.13 82551QM Reserved (Words 24h:2Fh)

These words are reserved and should be set to zeros. However, they may also be left unprogrammed (FFFFh).

2.6.14 82551QM Boot Agent Main Setup Options (Word 30h)

The boot agent software configuration is controlled by the EEPROM with the main setup options stored in word 30h. These options are those that can be changed by using the Control-S setup menu or by using IBAUtil.EXE (Intel Boot Agent utility). Note that these settings only apply to Boot Agent software.

Table 13. 82551QM Boot Agent Main Setup Options

Bit	Name	Description
15:13	Reserved	Reserved for future use. This bit must be set to 0b.
12:10	FSD	Bits 12:10 control forcing speed and duplex during driver operation. Valid values are: 000b = Auto-negotiate. 001b = 10 Mb/s half duplex. 010b = 100 Mb/s half duplex. 011b = Not valid (treated as 000b). 100b = 10 Mb/s full duplex. 101b = 100 Mb/s full duplex. 111b = Reserved.
9	Reserved	Reserved Set this bit to 0b.



Table 13. 82551QM Boot Agent Main Setup Options

Bit	Name	Description
8	DSM	Display Setup Message. If this bit is set to 1b, the "Press Control-S" message appears after the title message. The default for this bit is 1b.
7:6	PT	Prompt Time. These bits control how long the "Press Control-S" setup prompt message appears, if enabled by DIM. 00b = 2 seconds (default). 01b = 3 seconds. 10b = 5 seconds. 11b = 0 seconds. Note that the Ctrl-S message does not appear if 0 seconds prompt time is selected.
5	Reserved	Reserved
4:3	DBS	Default Boot Selection. These bits select which device is the default boot device. These bits are only used if the agent detects that the BIOS does not support boot order selection or if the MODE field of word 31h is set to MODE_LEGACY. 00b = Network boot, then local boot. 01b = Local boot, then network boot. 10b = Network boot only. 11b = Local boot only.
2	Reserved	Reserved
1:0	PS	Protocol Select. These bits select the boot protocol. 00b = PXE (default value). 01b = Reserved. Other values are undefined.



2.6.15 82551QM Boot Agent Configuration Customization Options (Word 31h)

Word 31h contains settings that can be programmed by an OEM or network administrator to customize the operation of the software. These settings cannot be changed from within the Control-S setup menu or the IBA Intel Boot Agent utility. The lower byte contains settings that would typically be configured by a network administrator using the Intel Boot Agent utility; these settings generally control which setup menu options are changeable. The upper byte are generally settings that would be used by an OEM to control the operation of the agent in a LOM environment, although there is nothing in the agent to prevent their use on a NIC implementation.

Table 14. 82551QM Boot Agent Configuration Customization Options (Word 31h)

Bit	Name	Description
15:14	SIG	Signature. These bits must be set to 01b to indicate that this word has been programmed by the agent or other configuration software.
13:11	Reserved	Reserved for future use. Set these bits to 0b.
10:8	MODE	Selects the agent's boot order setup mode. This field changes the agent's default behavior in order to make it compatible with systems that do not completely support the BBS and PnP Expansion ROM standards. Valid values and their meanings are: 000b - Normal behavior. The agent attempts to detect BBS and PnP Expansion ROM support as it normally does. 001b - Force Legacy mode. The agent does not attempt to detect BBS or PnP Expansion ROM supports in the BIOS and assumes the BIOS is not compliant. The BIOS boot order can be changed in the Setup Menu. 010b - Force BBS mode. The agent assumes the BIOS is BBS-compliant, even though it may not be detected as such by the agent's detection code. The BIOS boot order CANNOT be changed in the Setup Menu. 011b - Force PnP Int18 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 18h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order CANNOT be changed in the Setup Menu. 100b - Force PnP Int19 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 19h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order CANNOT be changed in the Setup Menu. 101b - Reserved for future use. If specified, treated as value 000b. 110b - Reserved for future use. If specified, treated as value 000b. 111b - Reserved for future use. If specified, treated as value 000b.
7:6	Reserved	Reserved for future use. Set these bits to 0b.
5	DFU	Disable Flash Update. If set to 1b, no updates to the Flash image using PROSet is allowed. The default for this bit is 0b; allow Flash image updates using PROSet.
4	DLWS	Disable Legacy Wakeup Support. If set to 1b, no changes to the Legacy OS Wakeup Support menu option is allowed. The default for this bit is 0b; allow Legacy OS Wakeup Support menu option changes.

**Table 14. 82551QM Boot Agent Configuration Customization Options (Word 31h)**

Bit	Name	Description
3	DBS	Disable Boot Selection. If set to 1b, no changes to the boot order menu option is allowed. The default for this bit is 0b; allow boot order menu option changes.
2	DPS	Disable Protocol Select. If set to 1b, no changes to the boot protocol is allowed. The default for this bit is 0b; allow changes to the boot protocol.
1	DTM	Disable Title Message. If set to 1b, the title message displaying the version of the boot agent is suppressed; the Control-S message is also suppressed. This is for OEMs who do not wish the boot agent to display any messages at system boot. The default for this bit is 0b; allow the title message that displays the version of the boot agent and the Control-S message.
0	DSM	Disable Setup Menu. If set to 1b, no invoking the setup menu by pressing Control-S is allowed. In this case, the EEPROM can only be changed via an external program. The default for this bit is 0b; allow invoking the setup menu by pressing Control-S.

2.6.16 82551QM Boot Agent Configuration Customization Options (Word 32h)

Word 32h is used to store the version of the boot agent that is stored in the Flash image. When the Boot Agent loads, it can check this value to determine if any first-time configuration needs to be performed. The agent then updates this word with its version. Some diagnostic tools that report the version of the Boot Agent in the Flash also read this word. This word is only valid if the Boot Agent is present and enabled. Otherwise the contents may be undefined.

Table 15. 82551QM Boot Agent Configuration Customization Options (Word 32h)

Bit	Name	Description
15:12	MAJOR	PXE boot agent major version. The default for these bits is 0b.
11:8	MINOR	PXE boot agent minor version. The default for these bits is 0b.
7:0	BUILD	PXE boot agent build number. The default for these bits is 0b.



2.6.17 82551QM IBA Capabilities (Word 33h)

Word 33h is used to enumerate the boot technologies that have been programmed into the Flash. It is updated by IBA configuration tools and is not updated or read by IBA.

Table 16. 82551QM IBA Capabilities

Bit	Name	Description
15:14	SIG	Signature. These bits must be set to 01b to indicate that this word has been programmed by the agent or other configuration software.
13:5	Reserved	Reserved for future use. All bits must be set to 0b.
4	SAN	SAN capability is present in Flash. 0b = The SAN capability is not present (default). 1b = The SAN capability is present.
3	EFI	EFI UNDI capability is present in Flash. 0b = The EFI code is not present (default). 1b = The EFI code is present.
2	Reserved	Reserved
1	UNDI	PXE/UNDI capability is present in Flash. 1b = The PXE base code is present (default). 0b = The PXE base code is not present.
0	BC	PXE base code is present in Flash. 0b = The PXE base code is present (default). 1b = The PXE base code is not present.

2.6.18 Reserved (Words 34h:3Eh)

These words are reserved and should be set to zeros. However, they may also be left unprogrammed (FFFFh).

2.6.19 Checksum Word Calculation (Word 3Fh)

The 64-word Checksum (3Fh) should be calculated such that after adding all the words (00h-3Fh), including the Checksum word itself, the sum should be BABAh. The initial value in the 16-bit summing register should be 0000h and the carry bit should be ignored after each addition. This checksum can be located at 3Fh or FFh depending on the size of the EEPROM.

2.6.20 82551ER/IT Reserved (Words 40h:FEh)

These words are reserved and should be set to zeros. However, they may also be left unprogrammed (FFFFh).

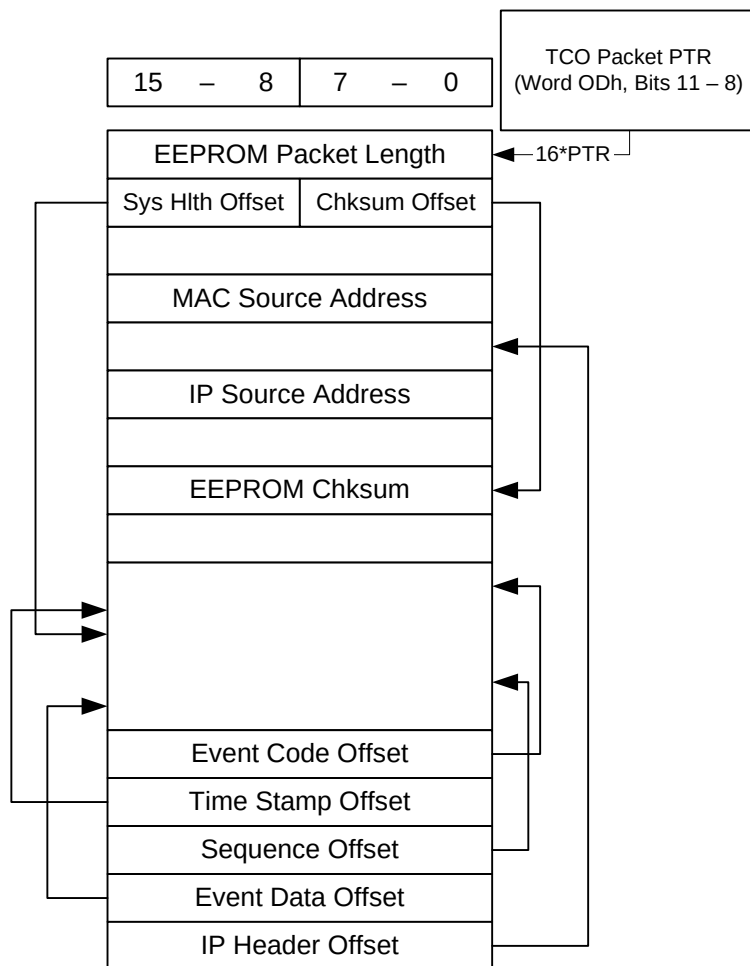
2.6.21 81551QM AoL Heartbeat Packet (Words 40h:F5h)

Word 40h is the first field of the AoL heartbeat packet and configures the Ethernet controller to generate the heartbeat packet. This field must be configured to 0044h for proper operation if AoL is enabled. Setting this field to FFFFh or 0000h causes undesirable results.

2.6.22 82551QM Heartbeat Packet Structure within the EEPROM (Word F6h:FAh)

When the 82551QM controller is connected directly to a side-band SMBus port in the PCI chipset for TCO functionality, the EEPROM may contain a heartbeat packet. The EEPROM packet format is matched, but not limited to, a UDP packet type. The offset of the system health indication and the offset of the UDP checksum are both aligned on even bytes. If a value of FFh is used in the checksum word, a checksum calculation is not calculated by the 82551QM controller. The FFh value can be used for packet formats other than the UDP packet.

Figure 1. 82551QM Transmit Management Package



Note: In words F6h:FAh, bits 15:8 are reserved and not used by the heartbeat packet.



2.6.23 82551QM Modem Configuration (Words FBh:FEh)

Words FBh:FEh contain the modem parameter information that will be loaded into the PCI Function 1 Configuration registers. This information follows the same format as utilized by the LAN (function 0). Note that CardBus combination NICs require a 256-word EEPROM.

Table 17. 82551QM Modem Configuration

Word	Hi Byte (Bits 15:8)	Lo Byte (Bits 7:0)
FBh	Modem Vendor ID	
FCh	Modem Device ID	
FDh	Modem Program Interface = 02h	Modem Revision Number = 00h
FEh	Modem Power Dissipation (D0h:D3h)	Modem Power Consumption (D0h:D3h)

2.6.24 Checksum Word Calculation (Word FFh)

The 256-word Checksum (3Fh) should be calculated such that after adding all the words (00h-FFh), including the Checksum word itself, the sum should be BABAh. The initial value in the 16-bit summing register should be 0000h and the carry bit should be ignored after each addition. This checksum can be located at 3Fh or FFh depending on the size of the EEPROM.



Appendix A: EEPROM Contents

This section contains an example of raw EEPROM contents. All values for these images are hexadecimal.

A.1 82551QM Ethernet Controller EEPROM Image

The following EEPROM image is for the 82551QM Fast Ethernet controller with Alert on LAN (AoL) capability disabled.

Note: “XXXX” denotes the Individual Address and “YYYY” denotes the Checksum. “WWW” is used for words Bh and Ch and is defined by the OEM (refer to [Section 2.6.2.1](#) and [Section 2.6.2.2](#)).

```
XXXX XXXX XXXX 0203 0000 0201 4701 0000
A276 9501 5022 WWW WWW 007F 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 1229 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 YYYY
```

A.2 82551QM EEPROM Image with Basic AoL

The following EEPROM image is for the 82551QM Fast Ethernet controller with basic AoL capability enabled.

Note: “XXXX” denotes the Individual Address and “YYYY” denotes the Checksum. “WWW” is used for words Bh and Ch and is defined by the OEM (refer to [Section 2.6.2.1](#) and [Section 2.6.2.2](#)).

```
XXXX XXXX XXXX 0B13 0000 0201 4701 0000
A320 4002 5022 WWW WWW 007F FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF 1229 FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```



```
;  
0044 FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
;  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
;  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF  
FFFF FFFF FFFF FFFF FFFF FFFF FFFF YYY
```



A.3 82551QM EEPROM Image with Advanced AoL

The following EEPROM image is for the 82551QM Fast Ethernet controller with advanced AoL capability enabled.

Note: “XXXX” denotes the Individual address and “YYYY” denotes the checksum. “WWWW” is used for words Bh and Ch and is defined by the OEM (refer to [Section 2.6.2.1](#) and [Section 2.6.2.2](#)).

```
XXXX XXXX XXXX 0B13 0000 0201 4701 0000
A320 4002 5022 WWWW WWWW 447F FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF 1229 FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
;
0044 FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
;
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
;
```



```
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF YYYY
```

A.4 82551QM LOM EEPROM Image with Basic AoL

The following EEPROM image is for the 82551QM LOM Fast Ethernet controller with basic AoL capability enabled.

Note: “XXXX” denotes the Individual Address and “YYYY” denotes the Checksum. “WWWW” is used for words Bh and Ch and is defined by the OEM (refer to [Section 2.6.2.1](#) and [Section 2.6.2.2](#)).

```
XXXX XXXX XXXX 0B13 0000 0201 4701 0000
A320 4002 5022 WWWW WWWW 007F FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF 1229 FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
;
0044 FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
;

```

[illegible]

A.5 82551QM LOM EEPROM Image with Advanced AoL

The following EEPROM image is for the 82551QM LOM Fast Ethernet controller with advanced AoL capability enabled.

Note: “XXXX” denotes the Individual address and “YYYY” denotes the checksum. “WWWW” is used for words Bh and Ch and is defined by the OEM (refer to [Section 2.6.2.1](#) and [Section 2.6.2.2](#)).

```

XXXX XXXX XXXX 0B13 0000 0201 4701 0000
A320 4002 5022 WWWW WWWW 447F FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF 1229 FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
002C 4000 3005 FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

```



```
0044 FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```

;

```
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```

;

```
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF YYY
```




A.6 82551ER/IT EEPROM Image

```
0200 00B3 0000 0203 FFFF 0201 4701 FFFF
A795 7401 5FA2 0070 8086 007F FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF 1209 FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```