C COMPILER FOR THE MICRO ARCHITECTURE CODE

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WHAT IS MICRO ARCHITECTURE CODE ?

- Intel CISC CPUs mandate a dual-layer design:
  - External architectural appearance is CISC
  - internal mechanisms employ RISC
- The Internal RISC instructions are called micro-instructions or micro-operations
- Programming of Microcode is done using a low-level microassembly language.

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- Hybrid calling support : C <-> Microcode
- Aggressive optimization of size and performance
- Support debugging for aggressively optimized
- Constant changes in micro arch registers should not lead to compiler upgrade
- Micro arch HW contains large set of restrictions on the usage of registers and instruction groups

BASIC EXAMPLE OF C TO MICROCODE

```
void TEST()
{
 uint32_t x = 1;
 uint64_t y = 0;

  y = x + 6;
  EAX = y;
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global TEST():
{
    # uint32_t x = 1;
    R0 := umove32(0x1);

    # uint64_t y = 0;
    R1 := umove64(0x0);

    # y = x + 6;
    R1 := uadd64(R0, 0x6);

    # EAX = y;
    EAX := umove64(R1);
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SUPPORTING MICRO-ARCH REGISTERS

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typedef union {
    uint32_t raw32;
    struct {
        uint32_t        x:1;            // reg[0:0]
        uint32_t        field_1:7;      // reg[7:1]
        uint32_t        y:1;            // reg[8:8]
        uint32_t        field_2:22;     // reg[30:9]
        uint32_t        z:1;            // reg[31:31]
    };
} uArchReg_t;

extern uArchReg_t uArchReg;
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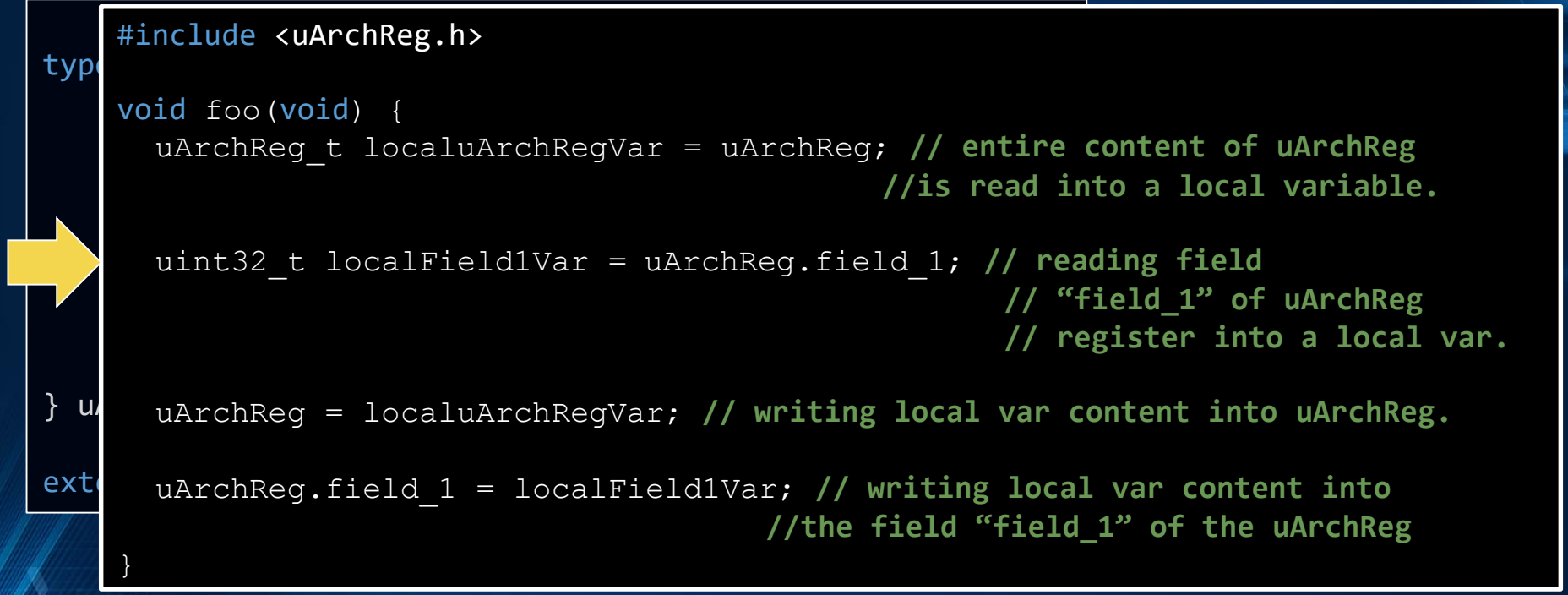

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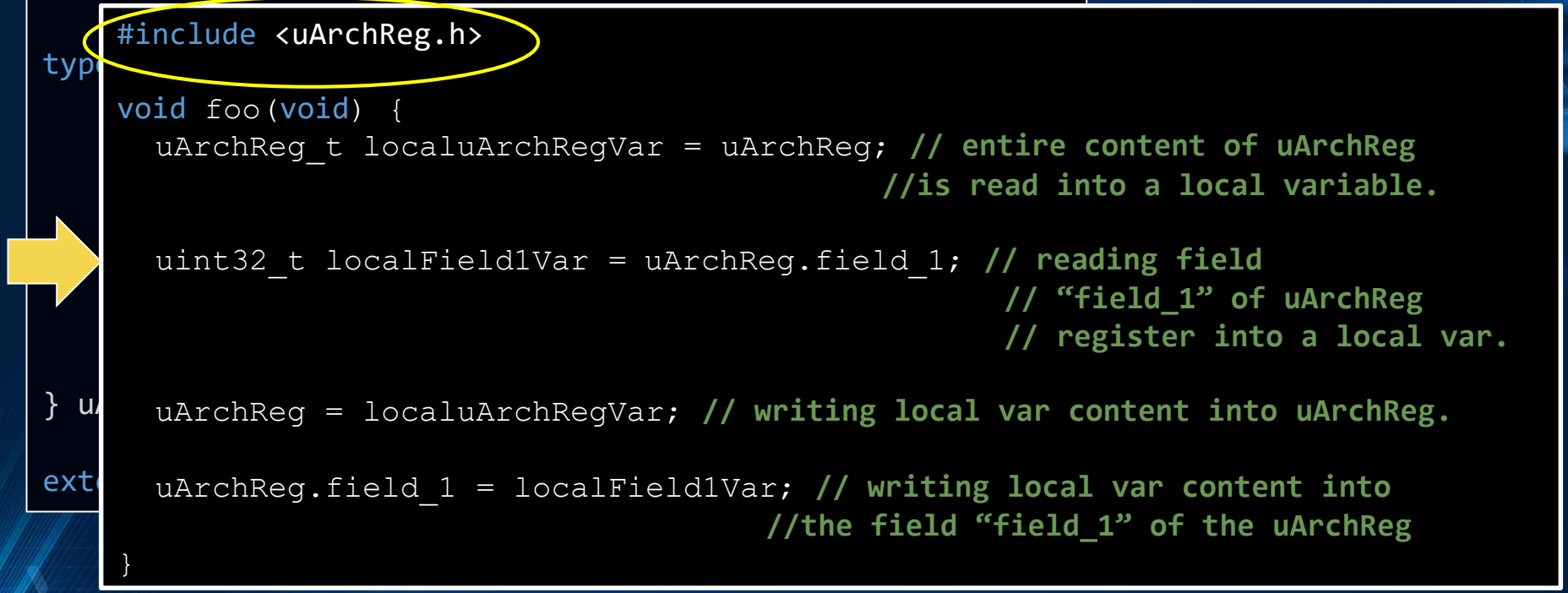

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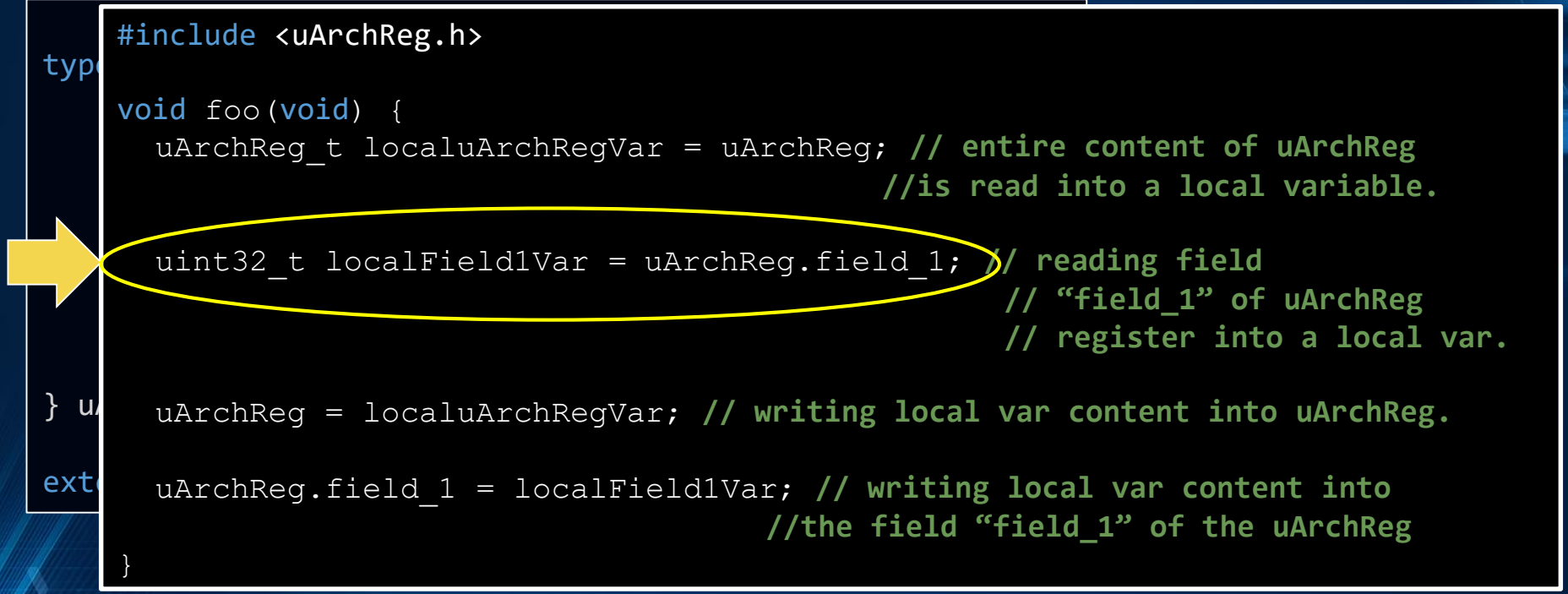

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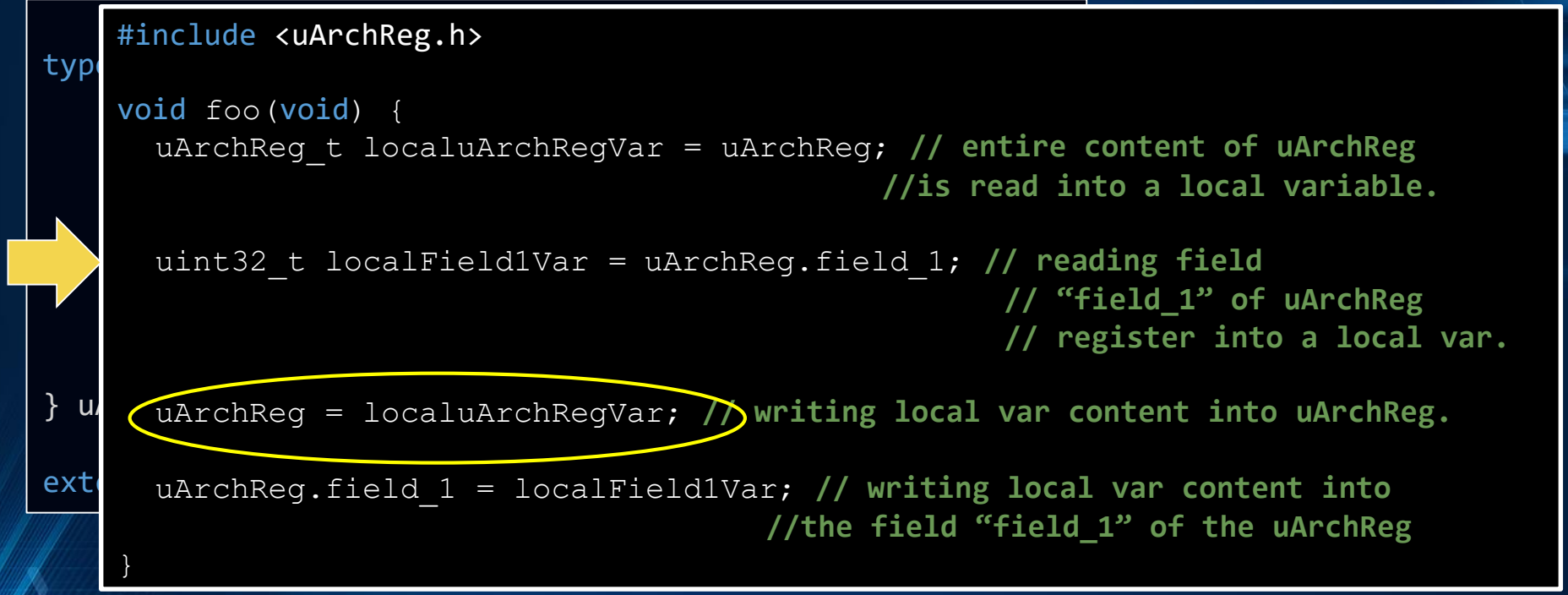

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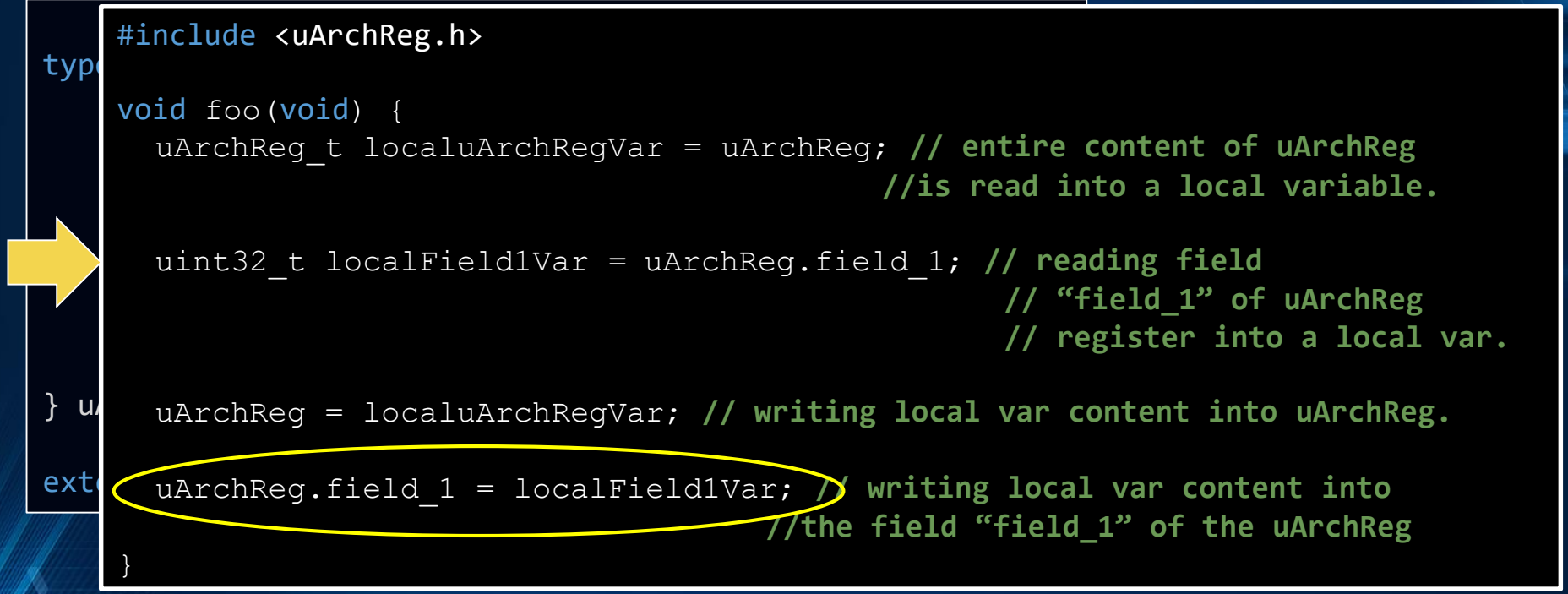

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TYPICAL OPTIMIZATION ON SINGLE BIT FIELDS

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if (uArchReg.x & uArchReg.y & uArchReg.z){
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(uArchReg >> x_pose) & 0x1
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(uArchReg >> y_pose) & 0x1
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(uArchReg >> z_pose) & 0x1
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if ((uArchReg & (1 << x_pose | 1 << y_pose | 1 << z_pose))
        == (1 << x_pose) | 1 << y_pose  | 1 << z_pose))  {
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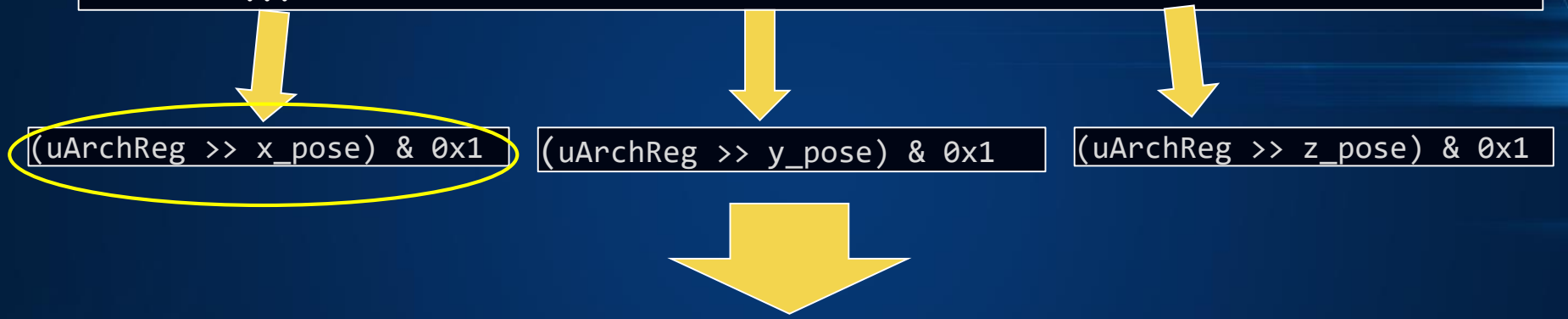


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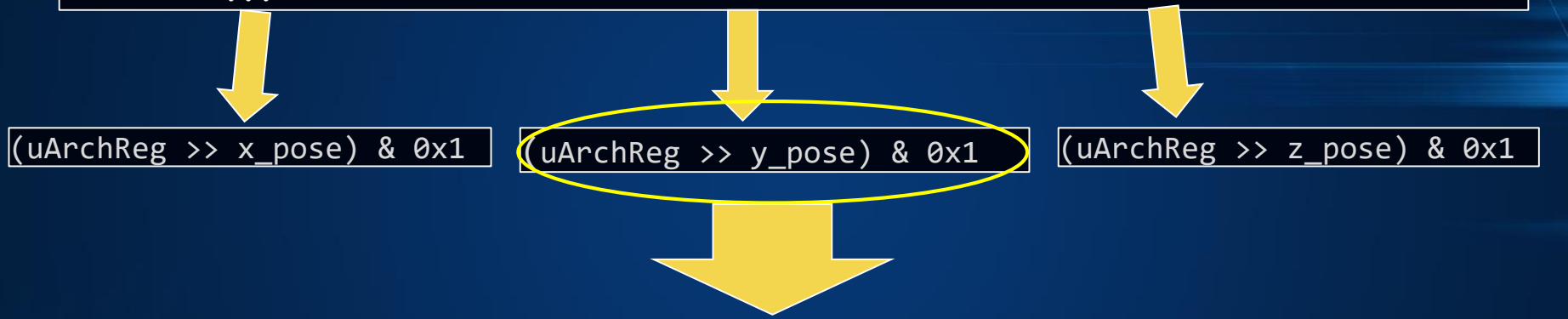


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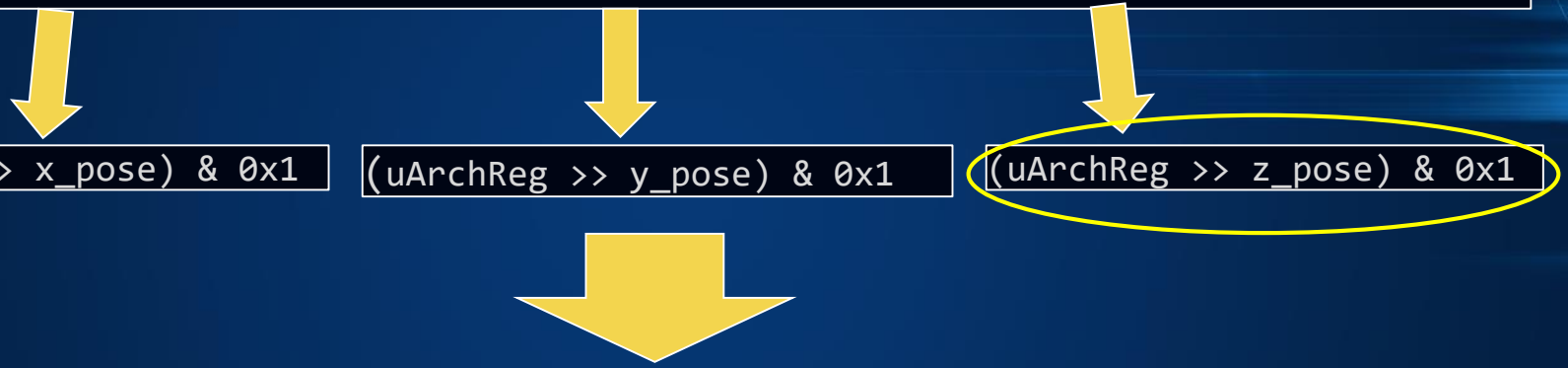


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```
if ((uArchReg & (1 << x_pose | 1 << y_pose | 1 << z_pose)) != 0)    {
                        ...
```

THANK YOU