September 2017 Newsletter

Highlights

2017 IXPUG Annual Meeting at TACC, September 26-28, 2017 in Austin, Texas: Register now to meet with experts from around the world to learn more about code modernization on Intel® Xeon Phi™ processors.

Intel® HPC Developer Conference November 11-12, 2017 in Denver, Colorado: Come gain hands-on experience with Intel platforms and network with peers and HPC industry experts. Register now.

RSVP to the Intel® PCC members only meeting during SC17: Join us at Venice Ristorante Downtown on November 14, 2017 from 6:00PM-9:30PM MST. This event is invite-only. If you have not received an email please contact IPCC.Program.Office@intel.com.

New Intel® PCCs

Welcome our newest Intel® PCC members:

- The Molecular Sciences Software Institute
- National Energy Research Scientific Computing Center
- New York University
- University of California, Berkeley
- University of California, Davis
- University of Liverpool
- University of Oxford
- Shanghai Jiao Tong University
- Tsinghua University - School of Life Sciences

Case Studies

National Energy Research Scientific Computing Center launches a new Big Data Center on Cori with five Intel® PCCs: University of California-Berkeley, University of California-Davis, New York University, Oxford University and the University of Liverpool.

SURFsara achieved Deep Learning training in less than 40 minutes with best accuracy on ImageNet-1K with scale-out KNL by using large global batch sizes, modified batch normalization, aggressive learning rate schedules, warm-up strategies, and wide network topology architectures.

University of Tennessee reorganized elements in matrices in **LAPACK**, a Linear Algebra Package, into contiguous arrays, using block interleaved memory format and optimizing the use of cache which gave them a 40x times faster for POSV on KNL.

Training Opportunities

These upcoming parallel programming workshops offer developers training with hands-on experience:

Date	Location	Event
Sept 6, 2017	Espoo, Finland	Intro to C Programming
Sept 7, 2017	Seoul, South Korea	HPC Code Modernization Workshop
Sept 9-13, 2017	Portland, USA	Parallel Architectures and Compilation Techniques
Sept 13, 2017	Virtual	Boost Application Performance using Intel® Parallel Studio XE
Sept 18-29, 2017	Virtual	Colfax: HOW Series Webinar
Sept 20, 2017	Virtual	Increase Performance for Workloads on Intel® Xeon® Processors
Sept 19-21, 2017	Virtual	Introducing Intel's Thread Building Blocks
Sept 26, 2017	Seoul, South Korea	Intel Software Developers Conference
Sept 27, 2017	Virtual	Better Threaded Performance with Intel® VTune™ Amplifier + OpenMP*
Sept 29, 2017	Tokyo, Japan	Intel Software Developers Conference
Oct 2-3, 2017	Espoo, Finland	Geocomputing Using CSC Resources
Oct 3, 2017	London, UK	Intel Software Developers Conference
Oct 4, 2017	Virtual	Memory Profiling: Find and Fix Common Performance Bottlenecks
Oct 11, 2017	Virtual	Is Python* Almost as Fast as Native Code? Believe It!
Oct 18, 2017	Virtual	Speed Up Small-Matrix Multiplication with Intel® Math Kernel Library
Oct 25, 2017	Virtual	Accelerating Lossless Data Compression Code for Cloud
Nov 3, 2017	Virtual	Parallel Programming Standards Update: MPI*, OpenMP* and Intel® TBB
Nov 8, 2017	Virtual	Better, Faster and More Scalable: The March To Exascale
Jan 28-31, 2018	Tokyo, Japan	IXPUG Workshop at HPC Asia

Access to Intel® Xeon Phi™ Processor

Optimize your applications for multi-node by testing on the following clusters:

Texas Advanced Computing Center (TACC) Stampede Cluster:

- Click **HERE** and create a new account (**do not click on PI-eligible**) and follow the email instructions.
- Register your account by emailing **ipcc.program.office@intel.com** with your username.

More News...

Check out these latest HPC news stories:

- Scalable Processors Accelerate Creation and Innovation in Next-Generation Workstations
- A Look Ahead (and Back) to the Intel HPC Developer Conference
- New Intel® Xeon® Scalable Processor Scalable Family Improves HPC Performance
- Boosting Performance and Efficiency of HPC Workloads

- **Texas Advanced Supercomputing Center Taps Latest HPC Tech**