January 2017 Newsletter

Artificial Intelligence on Intel® Architecture

See how Intel's commitment to Artificial Intelligence (AI) on Intel® Architecture will drive unprecedented developments in medicine, scientific discovery and education.

- **Intel Unveils Strategy for State-of-the-Art Artificial Intelligence**
- **AI and Machine Learning in the Spotlight at the Intel HPC Developer Conference**
- **Intel® PCCs Kai Li Keynote: Going Where Neuroscience and Computer Science Have not Gone Before**

Remote Intel® Xeon Phi™ Processor Cluster Access

We encourage you to optimize your application for multi-node by testing on the following clusters:

Texas Advanced Computing Center (TACC) Stampede Cluster:

- Click **HERE** and create a new account (**do not click on PI-eligible**) and follow the email instructions.
- Register account by emailing **ipcc.program.office@intel.com** with username.

Zuse Institute Berlin's (ZIB) Cluster:

- Request account by following the instructions on the application document, located **HERE**.

Intel® Application Development Cluster (Endeavor):

- Request account by completing the form located **HERE**.

Publication Opportunities

We encourage you to share best practices and results with the broader community by participating in the publishing opportunities below.

IXPUG Working Groups listed below are a platform for you to share your challenges, successes, and experiences in code modernization:

User Group	Description
General Optimization and Tuning Working Group	Share general results and techniques, troubleshooting optimization issues, and facilitating collaboration between community members and Intel® engineers.
Vectorization Working Group	Identifying frequent patterns and challenges encountered in using compiler-assisted (auto-) vectorization to generate feedback for compilers and language standards (e.g. OpenMP).
Message Passing Interface (MPI) Working Group	Share knowledge of methods for using MPI generally and of Intel®-oriented exploitation of MPI (e.g. Intel's® HPC fabric products, Intel® MPI Library and profilers).

International Supercomputing Conference 2017 board is accepting proposals. The event will be held in Frankfurt, Germany from June 18-22, 2017. Check out the important info below:

Submission Deadlines	Opportunities
Wednesday, February 15, 2017	Workshops, Tutorials, BoF Sessions, PhD Forum
Friday, March 3, 2017	Research Posters, Project Posters

Free Training Opportunities

Participate in the workshops listed below! Sharpen your theoretical and experiential skills with these training opportunities for developers.

Date	Location	Event
Jan 16-27, 2017	Virtual	Colfax Hands-On Webinar Series
Jan 18-19, 2017	Berlin, Germany	Intel® Code Modernization Workshop Berlin

*NEW: Case Studies

Sao Paulo State University (UNESP): GeantV is a next-generation simulation software describing the passage of particles through matter. Their approach is portable performance, and as a bonus, it comes with the insulation of the core application and algorithms from the technology layer.

University of Texas at Austin: BLAS interface for matrix operations in defining a simple, low-level interface for tensor contraction and other operations, while providing a high-performance implementation using the BLIS framework.

More News...

Find out more about HPC in the articles below:

- Quick Analysis of Vectorization Using the Intel® Advisor 2017 Tool (Article) (Video)
- Exploring MPI for Python* on Intel® Xeon Phi™ Processor
- Thread Parallelism in Cython*