

# Intel® Stress Bitstreams and Encoder (Intel® SBE) 2016 - SHVC Scalable Main Profile

Version 2.2      Apr 1st 2016

## Package Description

This stream set is intended to validate a decoder for **SHVC Scalable Main Profile** compliance. It covers features of these profiles bit stream format and makes it easy to verify that the decoder's compliance to standard. The package contains:

- SHVC compressed bitstreams
  - Package includes
    - files of 30 frames at 128x72 EL, 256x128 BL resolution
    - files of 20 frames at 128x72 EL, 432x240 BL resolution
    - files of 20 frames at 256x128 EL, 432x240 BL resolution
    - files of 30 frames at 640x288 BL, 400x288 EL resolution
- MD5 check sums for decoding results of each encoded file
- all\_bitstreams.md5 — file with check sums for all encoded files
- number of bytes read from reconstructed buffer while decoding evaluated by simple memory model and number of bytes read per source sample
- Table with detailed description of each bitstream: enabled coding tools and possible values.

The decoding result is assumed correct if it binary-matches to the result of the reference decoder. This can be verified with the md5-files included within the package. All the streams are SHVC compliant - this package doesn't contain any invalid streams for error-resilience testing. Also this package is not intended for decoder-performance testing since a lot of bitstream features have distributions not typical for "real-world" video: many long motion vectors pointing out of frame, areas with random noise, highly variable QP values, etc.

The stream package consists of several buckets. Some buckets validate the features presumably related to intra and inter prediction correspondingly, and other buckets contains streams covering other SHVC format features not directly related to intra or inter prediction.

There are some types of streams like *Syntax*, *Stress*, *Special*, etc. *Syntax* streams are designed to test a certain subset of features, for example, all the intra-prediction. *Stress* streams include all the features covered by the bucket, so they are useful for smoke testing: if a decoder passes the *Stress* stream, it is likely to pass all the *Syntax* streams from the bucket. *Special* streams designed to using special SHVC technologies like POC reset's.

## File name pattern

All files are named corresponding to the following pattern: (Purpose)\_HEVC\_(level)\_(resolution)\_(frame rate)\_(id)\_(bucket/name)\_(encoder\_version)\_(layers).hevc

- (purpose) is "Syntax", "Stress";
- (resolution) is pair of frame width and height joint with "x"
- (frame rate) is number of frames per second followed by "fps"
- (id): either an index of stream in the bucket;
- (bucket/name): "INTRA", "INTER" or "SYNTAX"/ special feature name, e.g. "poc\_reset";
- (encoder\_version): version of encoder used for stream generation. Package may contain streams of different encoder versions;

- (layers): number of layers.

For example,

Syntax\_SHVC\_Main\_256x128\_30fps\_607\_shvc\_syntax\_poc\_reset\_all\_2.2\_s3\_432x240\_0.hevc is the 7th stream from SYNTAX bucket for POC reset testing, two layers.

Pair of (id) and (bucket/name) is a short description of the content of the stream.

### Video content

Each bitstream is encoded from a synthetic video sequence. Encoded sequences **may have strong visual artifacts** because of randomly selected syntax. Bitstreams contain frame sequences with bit depth 8 both in luma and chroma.

## Stream Description

Stream name	Description	Resolution, number of frames
<i>INTRA</i> bucket		
001_shvc_intra_base	Intra prediction, two layers and without cross layer prediction.	128×72 EL, 256x128 BL, 30 frames; 432×240 BL, 256x128 EL, 20 frames;
002_shvc_intra_adaptive_res	Intra prediction, two layers and without cross layer prediction. Adaptive resolution enable.	
003_shvc_intra_ref_layer_aux	Intra prediction, two layers and without cross layer prediction. AUX enable.	
004_shvc_intra_intra_layer3	Intra prediction, three layers and without cross layer prediction.	
005_shvc_intra_layer4	Intra prediction, four layers and without cross layer prediction.	
006_shvc_intra_intra_layer5	Intra prediction, five layers and without cross layer prediction.	
007_shvc_intra_intra_layer6	Intra prediction, six layers and without cross layer prediction.	
008_shvc_intra_intra_layer7	Intra prediction, seven layers and without cross layer prediction.	
009_shvc_intra_intra_layer8	Intra prediction, eight layers and without cross layer prediction.	
<i>INTER</i> bucket		
101_shvc_intra_ref_layer	Intra prediction, two layers and cross layer reference enable.	128×72 EL, 256x128 BL, 30 frames; 432×240 BL, 256x128 EL, 20 frames;
102_shvc_intra_ref_layer3	Intra prediction, three layers and cross layer reference enable.	
103_shvc_inter_inter_ref_layer4	Intra prediction, four layers and cross layer reference enable.	
104_shvc_intra_inter_ref_layer5	Intra prediction, five layers and cross layer reference enable.	
105_shvc_intra_inter_ref_layer6	Intra prediction, six layers and cross layer reference enable.	
106_shvc_intra_inter_ref_layer7	Intra prediction, seven layers and cross layer reference enable.	

107_shvc_intra_inter_ref_layer8	Intra prediction, eight layers and cross layer reference enable.	
201_shvc_inter_ref_layer1	Inter prediction, two layers and cross layer reference enable.	
202_shvc_inter_ref_layer3	Inter prediction, three layers and cross layer reference enable.	
203_shvc_inter_inter_ref_layer4	Inter prediction, four layers and cross layer reference enable.	
204_shvc_inter_inter_ref_layer5	Inter prediction, five layers and cross layer reference enable.	
205_shvc_inter_inter_ref_layer6	Inter prediction, six layers and cross layer reference enable.	
206_shvc_inter_inter_ref_layer7	Inter prediction, seven layers and cross layer reference enable.	
207_shvc_inter_inter_ref_layer8	Inter prediction, eight layers and cross layer reference enable.	128x72 EL, 256x128 BL, 30 frames; 432x240 BL, 256x128 EL, 20 frames;
301_shvc_bframes_ref_layer	B frames enable, two layers.	
302_shvc_bframes_ref_layer3	B frames enable, three layers.	
303_shvc_bframes_ref_layer4	B frames enable, four layers.	
304_shvc_bframes_ref_layer5	B frames enable, five layers.	
305_shvc_bframes_ref_layer6	B frames enable, six layers.	
306_shvc_bframes_ref_layer7	B frames enable, seven layers.	
307_shvc_bframes_ref_layer8	B frames enable, eight layers.	
309_shvc_bpred_ref_layer	B-pyramid, two layers	
EXTRA bucket		
401_shvc_extra_bf_layer3	B frames and several references. Three layers.	128x72 EL, 256x128 BL, 30 frames; 432x240 BL, 256x128 EL, 20 frames;
402_shvc_extra_bf_layer3	B frames and several cross layers references. Three layers. Some syntax values enable.	
403_shvc_extra_bf_layer4	B frames and several cross layers references. Four layers.	
404_shvc_extra_bf_ref_layer4	B frames and several cross layers references. Four layers. Some syntax values enable.	
STRESS bucket		
501_shvc_stress_ref_layer8	B frames and several cross layers references. Eight layers.	128x72 EL, 256x128 BL, 30 frames; 432x240 BL, 256x128 EL, 20 frames;
503_shvc_stress_ref_layer8	B frames and several cross layers references. Eight layers. Enabled all of the above.	
Special bucket		
601_shvc_syntax_ng_offsets	Negative offsets in resampling.	128x72 EL, 256x128 BL, 30 frames; 432x240 BL, 256x128 EL, 20 frames;
602_shvc_syntax_cl_bla	Cross layer BLA flag enabled.	

603_shvc_syntax_discard	Discardable flag enabled	
604_shvc_syntax_phase	Phase randomization.	
605_shvc_syntax_poc_reset_1	POC reset of type 1.	
606_shvc_syntax_poc_reset_2	POC reset of type 2.	
607_shvc_syntax_poc_reset_all	All types of POC reset are enabled.	
608_shvc_syntax_ref_reg	BL window randomization.	
609_shvc_syntax_scaled_ref	EL window randomization.	
610_shvc_syntax_SP_S	SPS SHVC syntax randomization.	

## Legal Information

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

This document contains information on products, services and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest forecast, schedule, specifications and roadmaps.

The products and services described may contain defects or errors known as errata which may cause deviations from published specifications. Current characterized errata are available on request.

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or by visiting [www.intel.com/design/literature.htm](http://www.intel.com/design/literature.htm).

Intel, the Intel logo, Intel Core are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.