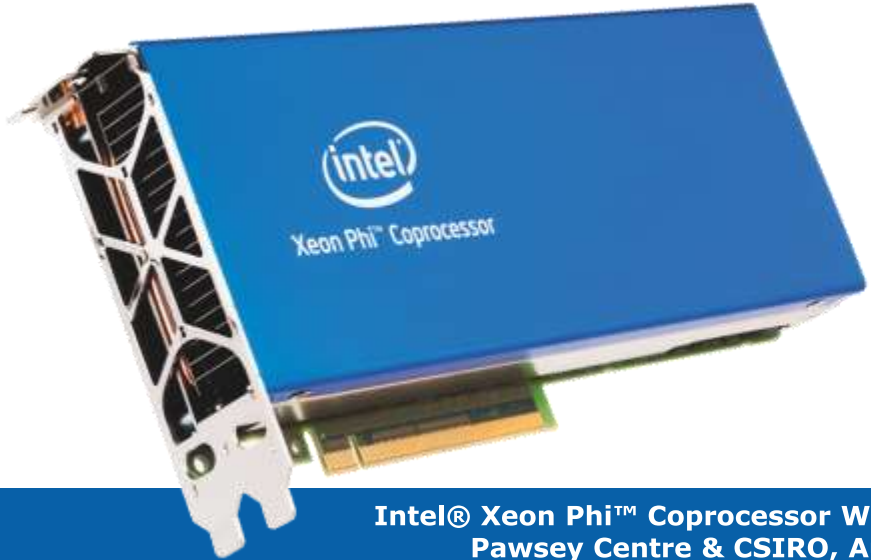
Intel® Xeon Phi™ Coprocessor Architecture Overview



Intel® Xeon Phi™ Coprocessor Workshop
Pawsey Centre & CSIRO, Aug 2013

Optimization Notice

Intel Software

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Architecture Topics

- Intel® Many Integrated Core (MIC) Architecture
- Intel® Xeon Phi™ Coprocessor Overview
- Core and Vector Processing Unit
- Setting Expectations
- Performance
- Summary

Module Outline

- **Intel® Many Integrated Core (MIC) Architecture**
- Intel® Xeon Phi™ Coprocessor Overview
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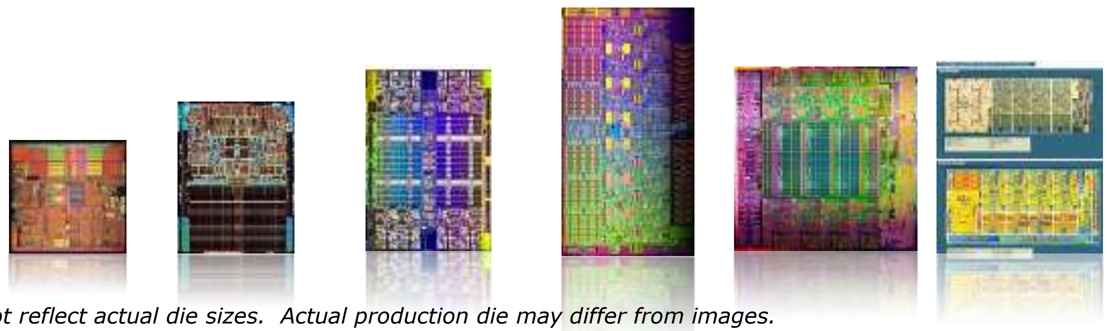
Intel Architecture Multicore and Manycore
More cores. Wider vectors. Coprocessors.

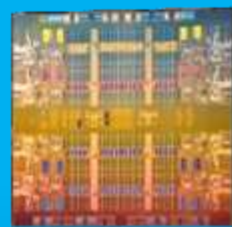


Images do not reflect actual die sizes. Actual production die may differ from images.

	Intel® Xeon® processor 64-bit	Intel® Xeon® processor 5100 series	Intel® Xeon® processor 5500 series	Intel® Xeon® processor 5600 series	Intel® Xeon® processor E5 Product Family	Intel® Xeon® processor code name Ivy Bridge	Intel® Xeon® processor code name Haswell	Intel® Xeon Phi™ Coprocessor
Core(s)	1	2	4	6	8	10	To be determined	61
Threads	2	2	8	12	16	20		244

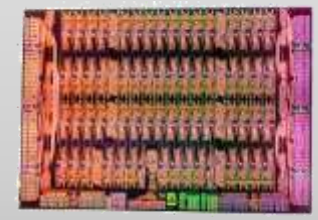
Intel® Xeon Phi™ coprocessor extends established CPU architecture and programming concepts to highly parallel applications

Intel® Multicore Architecture



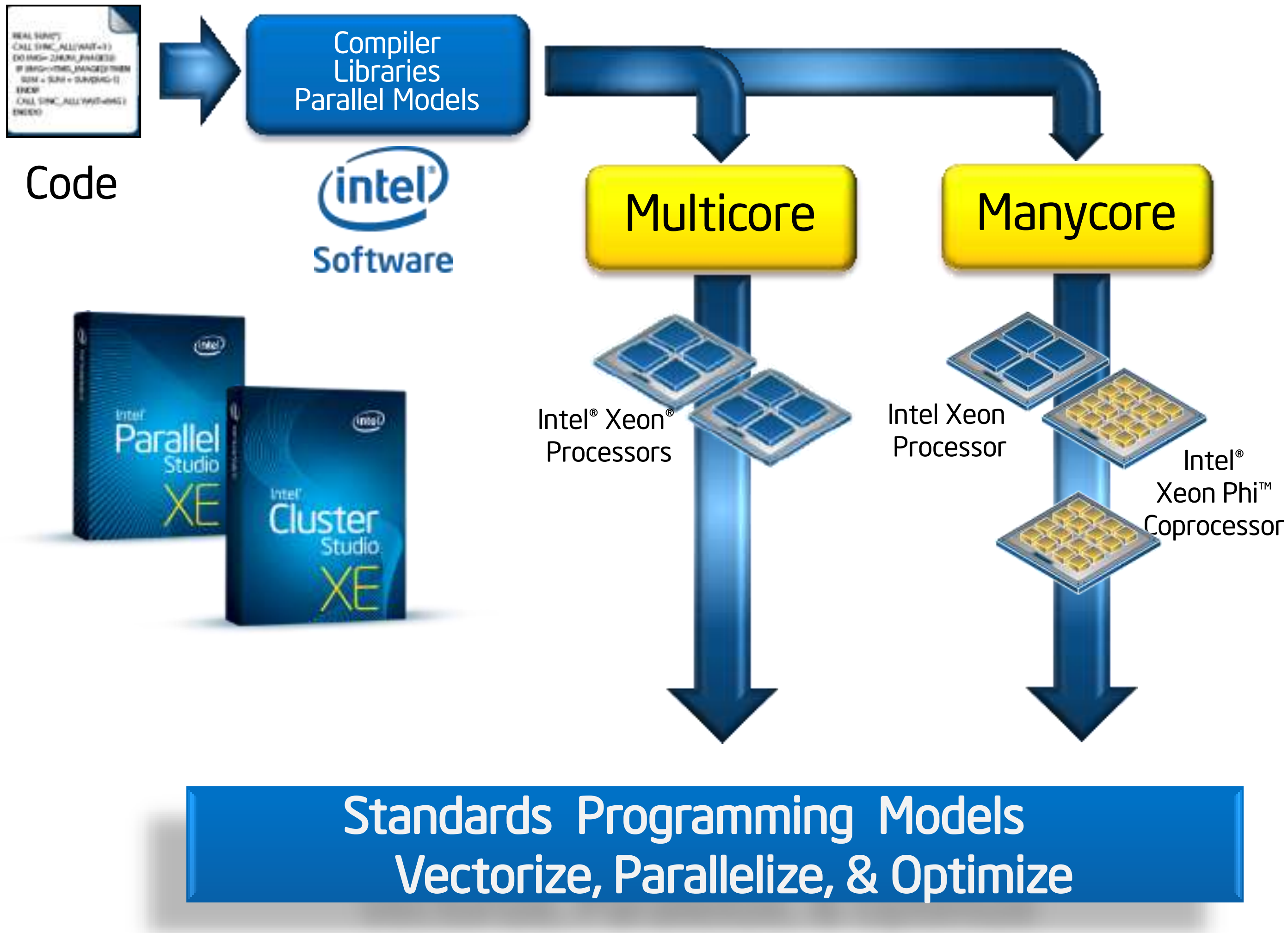
- Foundation of HPC Performance
- Suited for full scope of workloads
- Industry leading performance and performance/watt for serial & parallel workloads
- Focus on fast single core/thread performance with "moderate" number of cores

Intel® Many Integrated Core Architecture



- Performance and performance/watt optimized for highly parallelized compute workloads
- Common software tools with Intel® Xeon® architecture enabling efficient application readiness and performance tuning
- Intel® Architecture extension to Manycore
- Many cores/threads with wide SIMD

Consistent Tools & Programming Models



Module Outline

- Intel® Many Integrated Core (MIC) Architecture
- **Intel® Xeon Phi™ Coprocessor Overview**
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Introducing Intel® Xeon Phi™ Coprocessors

Highly-parallel Processing for Unparalleled Discovery

Groundbreaking differences

Up to 61 Intel® Architecture cores/1.1 GHz/ 244 threads

Up to 8 GB memory with up to 352 GB/s bandwidth

512-bit SIMD instructions

Linux* operating system, IP addressable

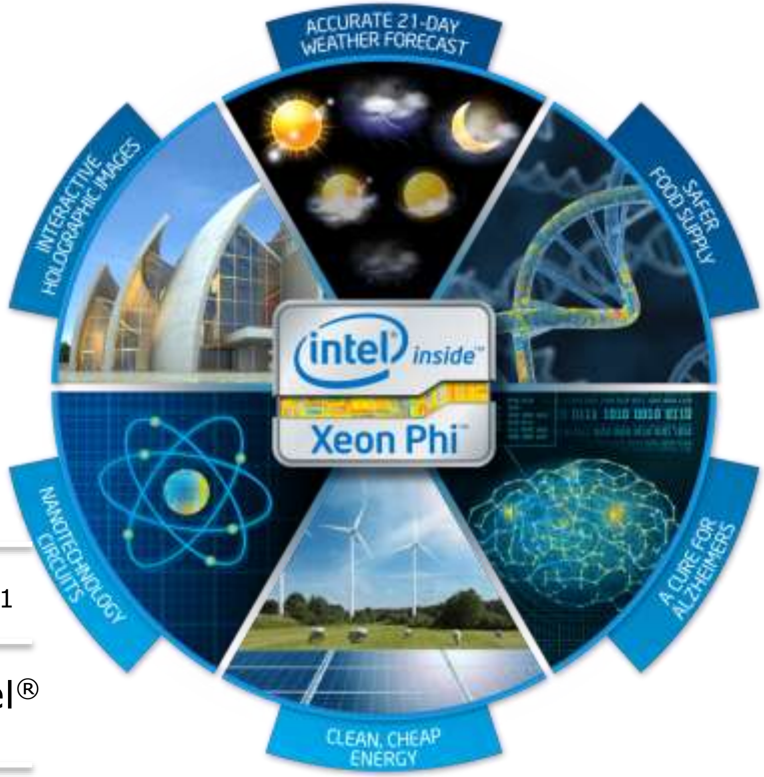
Standard programming languages and tools

Leading to Groundbreaking results

Over 1 TeraFlop/s double precision peak performance[1]

Up to 2.2x higher memory bandwidth than on an Intel® Xeon® processor E5 family-based server[2]

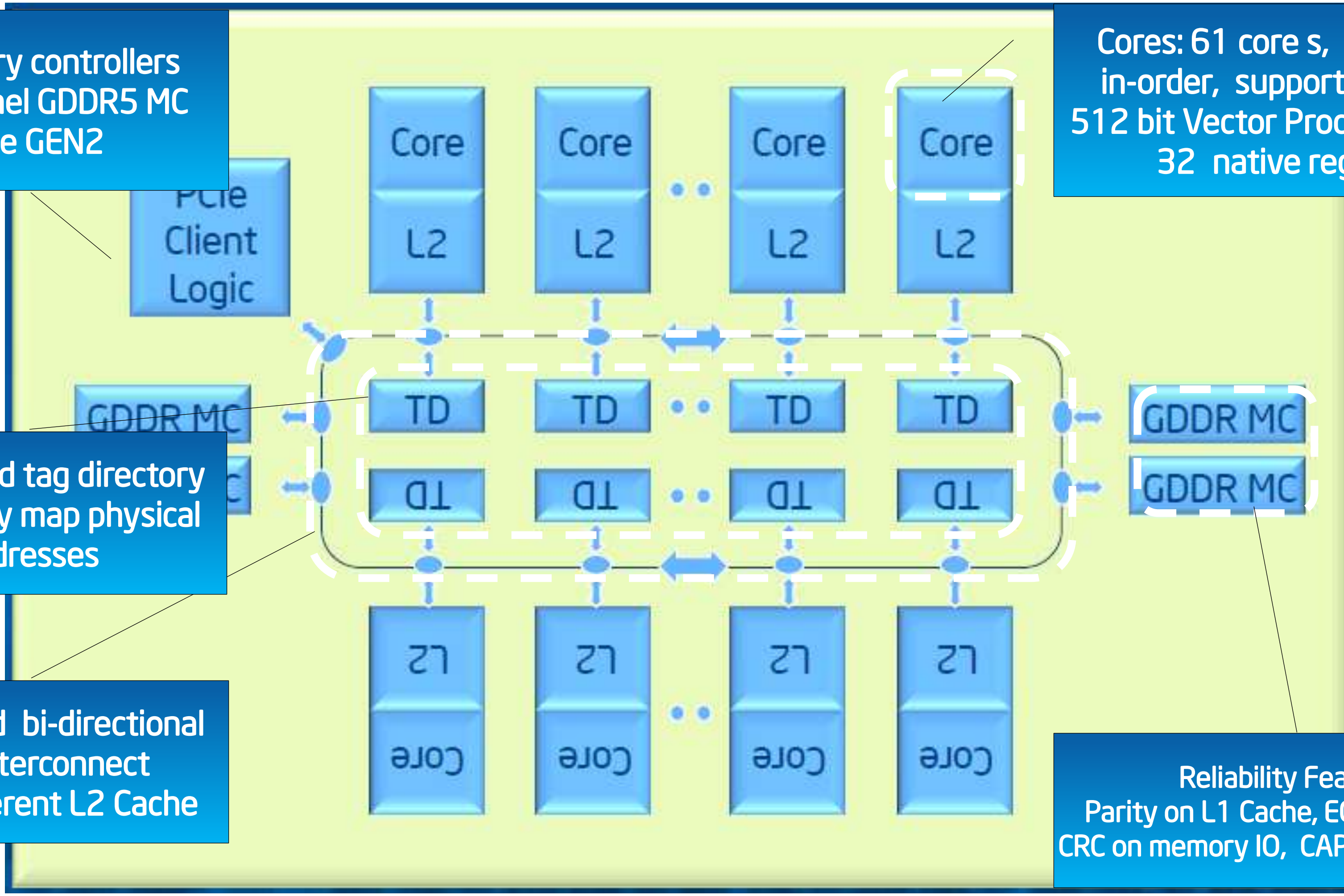
Up to 4x more performance per watt than with an Intel Xeon processor E5 family-based server[3]



Intel® Xeon Phi™ Architecture Overview

8 memory controllers
16-channel GDDR5 MC
PCIe GEN2

Cores: 61 core s, at 1.1 GHz
in-order, support 4 threads
512 bit Vector Processing Unit
32 native registers

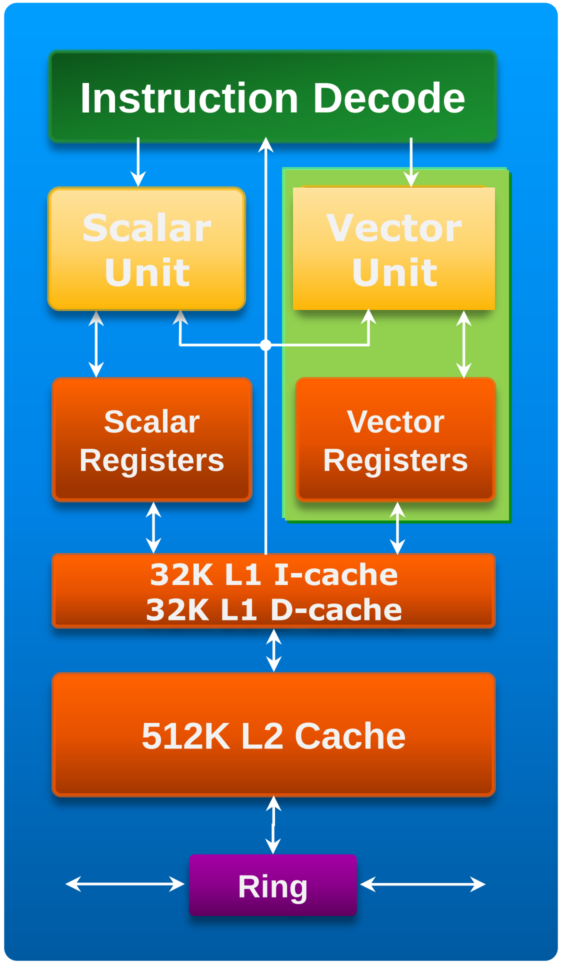


Distributed tag directory to uniquely map physical addresses

High-speed bi-directional ring interconnect
Fully coherent L2 Cache

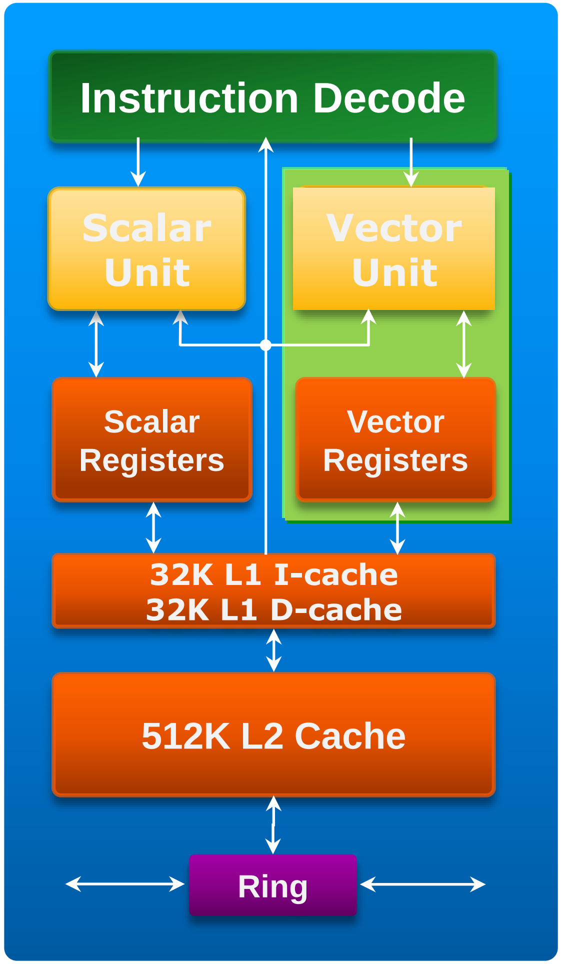
Reliability Features
Parity on L1 Cache, ECC on memory
CRC on memory IO, CAP on memory IO

Core Architecture Overview



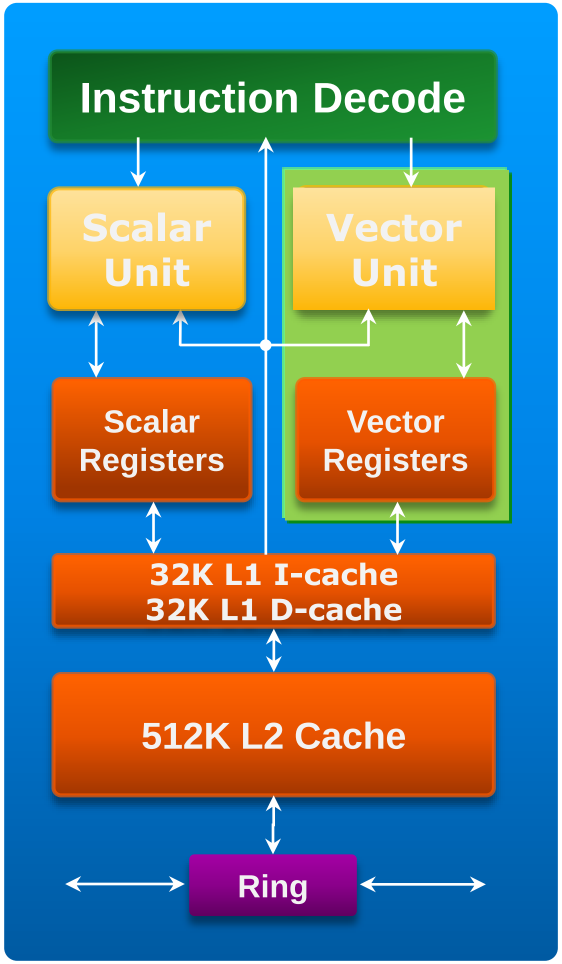
- 60+ in-order, low-power Intel® Architecture cores in a ring interconnect
- Two pipelines
  - Scalar Unit based on Pentium® processors
  - Dual issue with scalar instructions
  - Pipelined one-per-clock scalar throughput
- SIMD Vector Processing Engine
- 4 hardware threads per core
  - 4 clock latency, hidden by round-robin scheduling of threads
  - Cannot issue back-to-back inst in same thread
- Coherent 512 KB L2 Cache per core

Core Architecture Overview



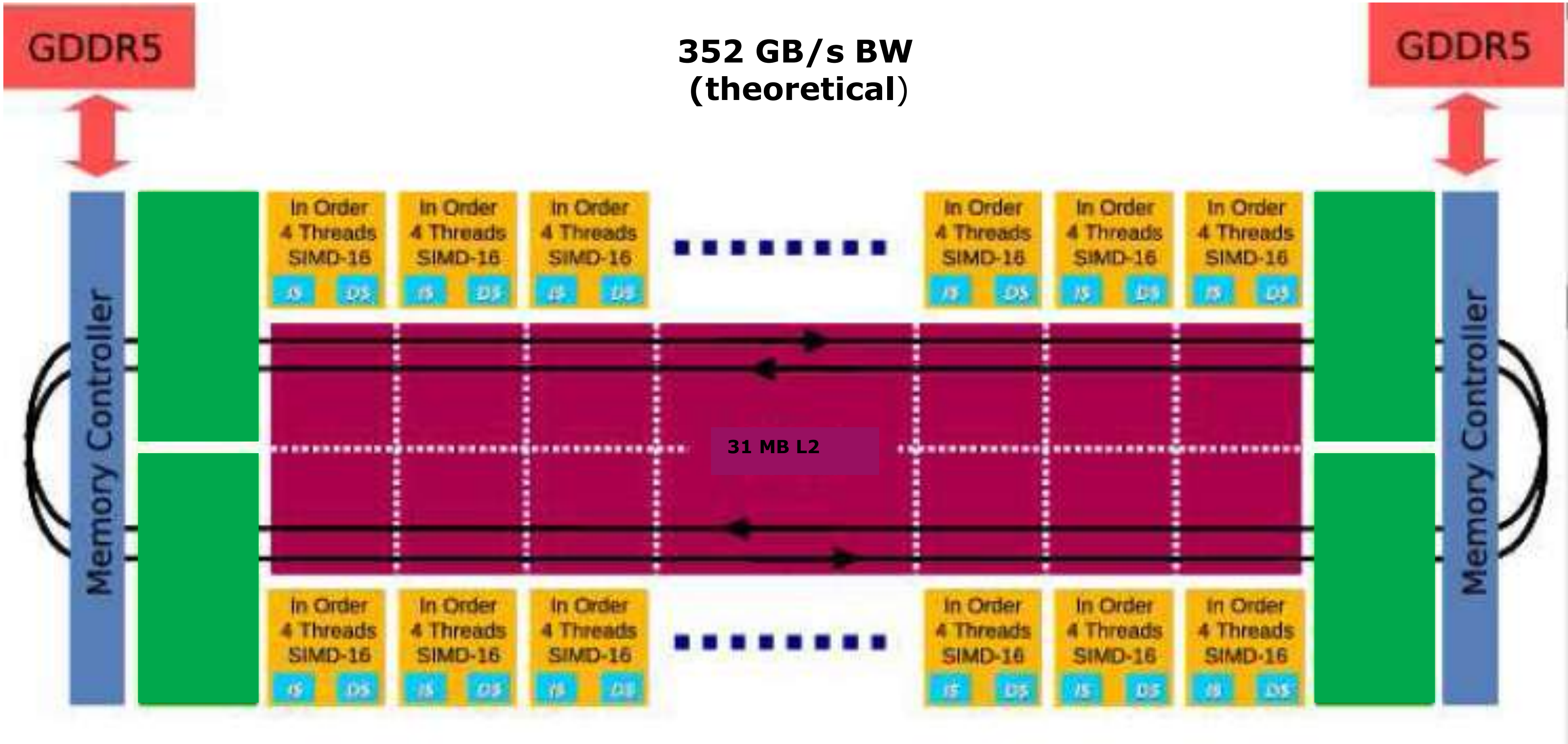
- 2 issue (1 scalar/1 vector)
- 2 cycle decoder: no back-to-back cycle issue from the same context (thread)
- Most vec instructions have 4 clock latency
- At least two HW contexts (thread/proc) to fully utilize the core

Core Architecture Overview

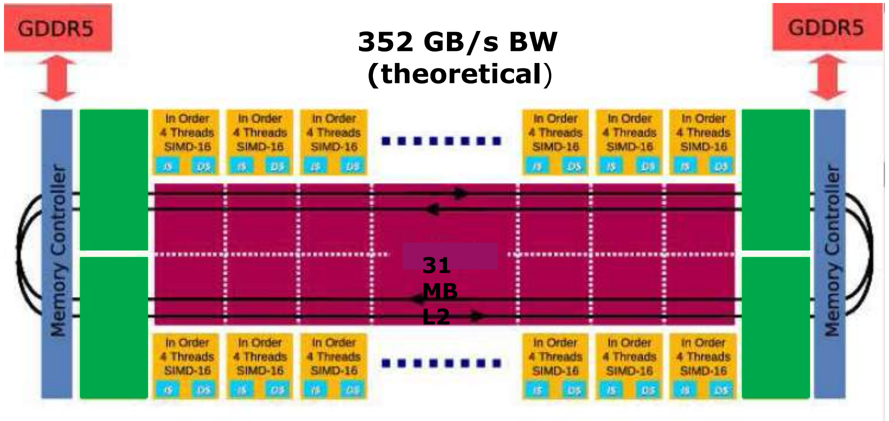


- Performance Monitoring Unit
  - 4 event select register
  - 4 performance counters
  - Shared among the 4 HW threads
  - Programmable via model specific registers (MSR) using RDMSR/WRMSR

Knights Corner Architecture Overview – Cache

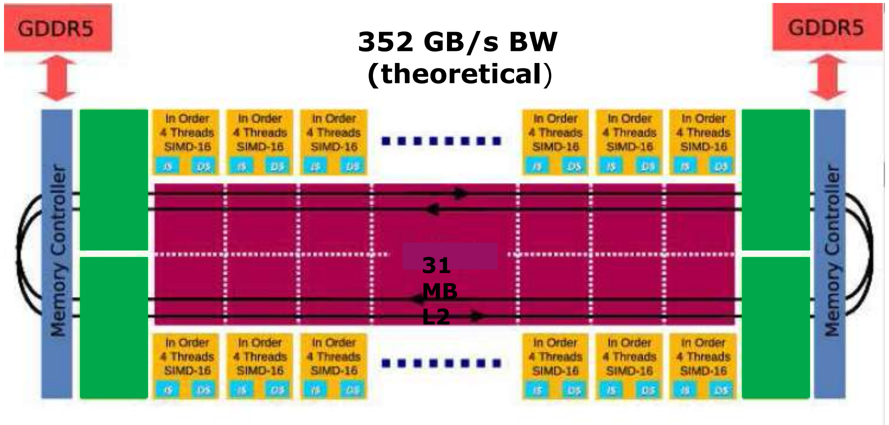


Knights Corner Architecture Overview – Cache



- L1 cache
  - 32K I-cache per core
  - 32K D-cache per core
  - 8 way associative
  - 64B cache line
  - 3 cycle access
  - Up to 8 outstanding requests
  - Fully coherent (MESI)
- L2 cache
  - 512K Unified per core
  - 8 way assoc
  - Inclusive
  - 31M total across 62 cores
  - 11 cycle best access
  - Up to 32 outstanding requests
  - Streaming HW prefetcher
  - Fully coherent

Knights Corner Architecture Overview – Cache



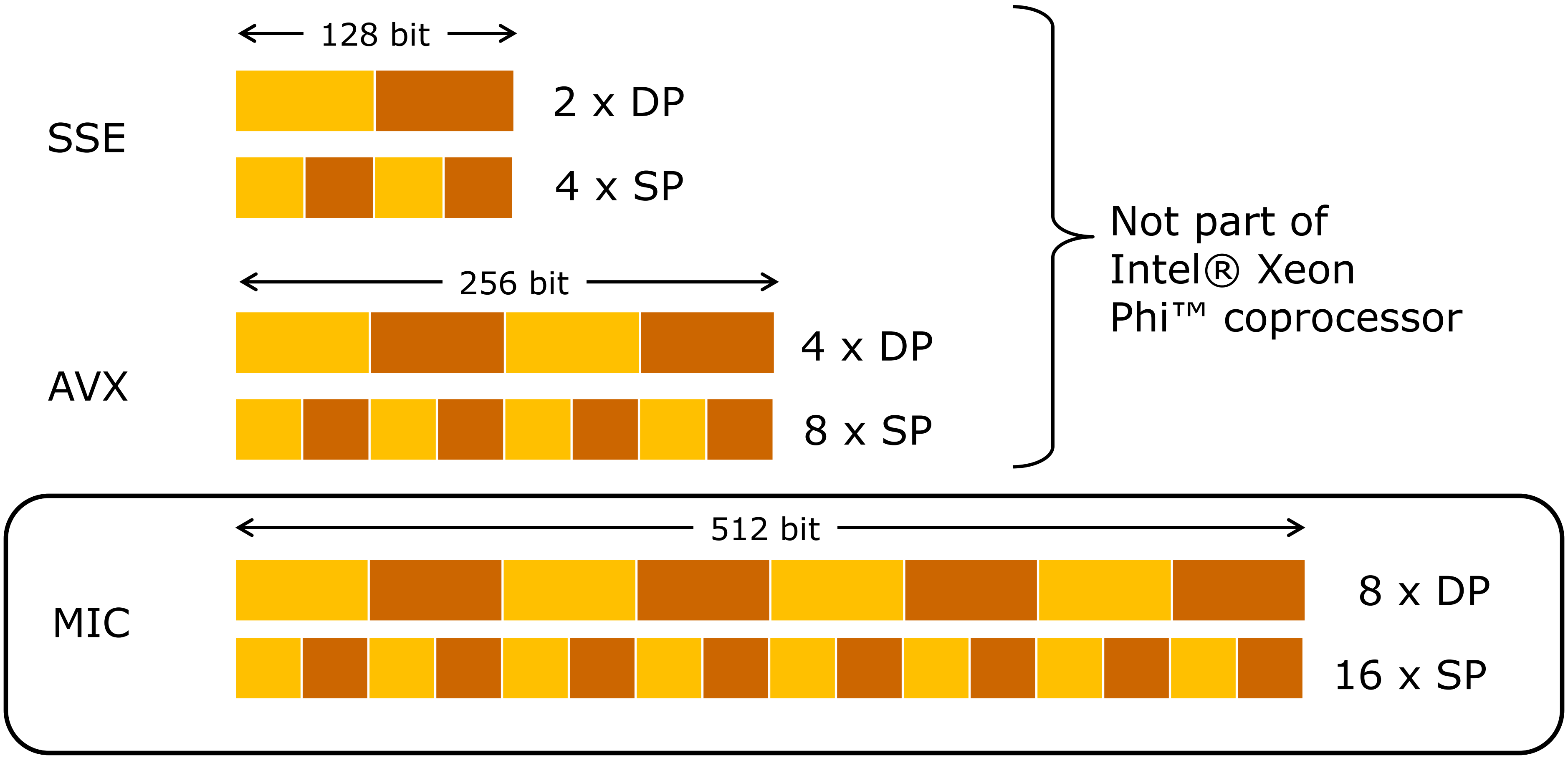
- Alignment
  - Based upon number of elements, element size, and vector load and store instruction
  - 64B alignment for 4B (float) data elements for a 16 to 16 vector load

- Memory
  - 8GB GDDR5
  - 8 Memory controllers, 16 GDDR5 channels, up to 5.5 GT/s
  - 300 ns access
  - Aggregate 352 GB/s peak memory bandwidth
  - ECC
- PCI Express*
  - Gen2 (Client) x16 per direction

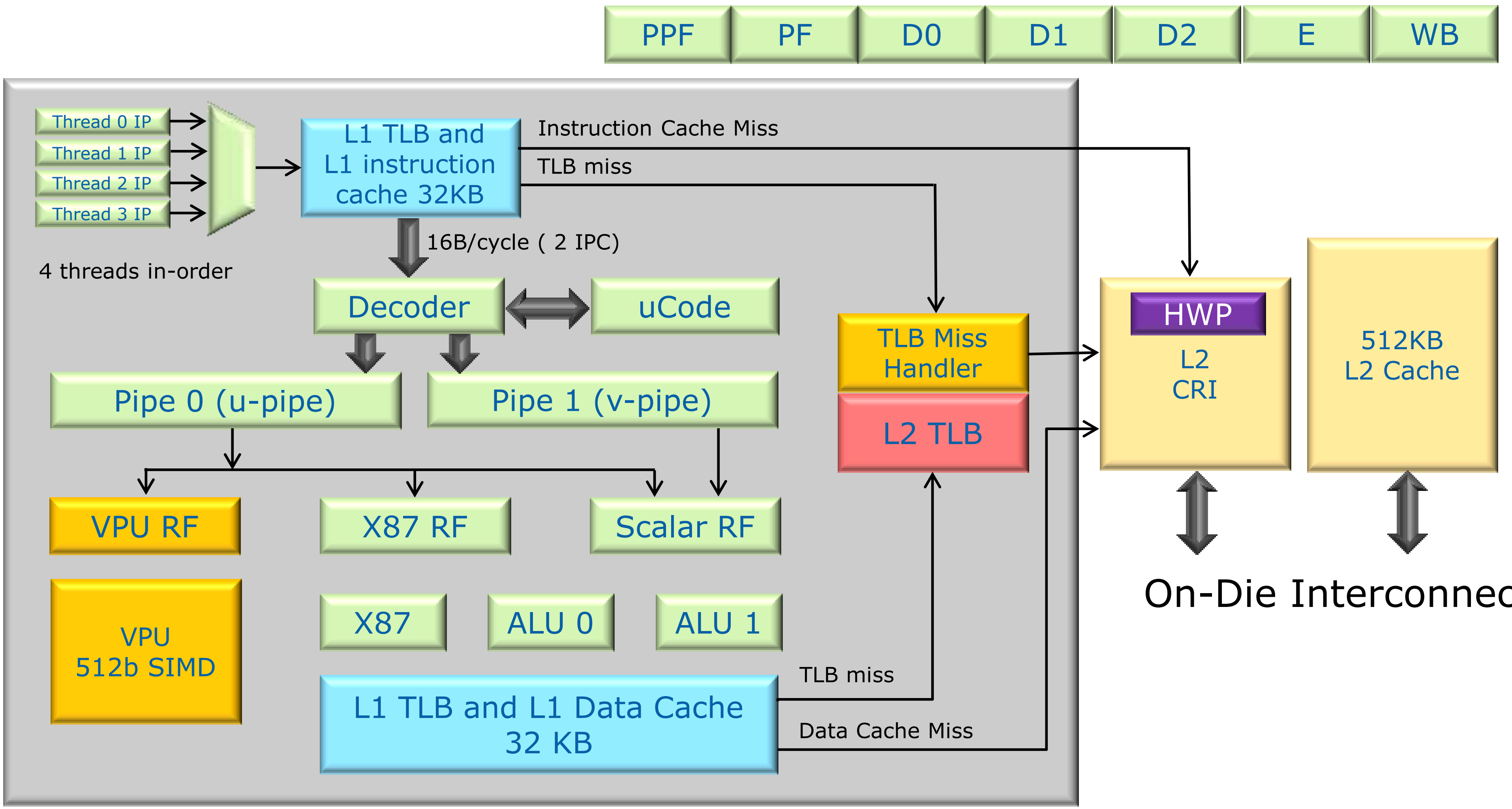
Module Outline

- Intel® Many Integrated Core (MIC) Architecture
- Intel® Xeon Phi™ Coprocessor Overview
- **Core and Vector Processing Unit**
- Setting Expectations
- Performance
- Summary

Knights Corner Architecture Overview
Vector Processing Unit and ISA



Vector Processing Unit Extends the Scalar IA Core



Vector Processing Unit and Intel® Initial Many Core Instructions (Intel® IMCI)

- Vector Processing Unit Execute Intel IMCI
- 512-bit Vector Execution Engine
  - 16 lanes of 32-bit single precision and integer operations
  - 8 lanes of 64-bit double precision and integer operations
  - 32 512-bit general purpose vector registers in 4 thread
  - 8 16-bit mask registers in 4 thread for predicated execution
- Read/Write
  - One vector length (512-bits) per cycle from/to Vector Registers
  - One operand can be from memory
- IEEE 754 Standard Compliance
  - 4 rounding models, even, 0, +∞, -∞
  - Hardware support for SP/DP denormal handling
  - Sets status register VXCSR flags but not hardware traps

Vector Instruction Performance

- VPU contains 16 SP ALUs, 8 DP ALUs

- Most VPU instructions have a latency of 4 cycles and TPT 1 cycle
  - Load/Store/Scatter have 7-cycle latency
  - Convert/Shuffle have 6-cycle latency

- VPU instruction are issued in u-pipe

- Certain instructions can go to v-pipe also
  - Vector Mask, Vector Store, Vector Packstore, Vector Prefetch, Scalar

Module Outline

- Intel® Many Integrated Core (MIC) Architecture
- Intel® Xeon Phi™ Coprocessor Overview
- Core and Vector Processing Unit
- Software Ecosystem
- Performance
- Summary

Programming Considerations - Setting Expectations (1)

- Getting full performance from the Intel® MIC architecture requires both a high degree of parallelism *and* vectorization
  - Not all code can be written this way
  - Not all programs make sense on this architecture

- The Intel® Xeon® processor is not an Intel® Xeon® processor
  - It specializes in running highly parallel and vectorized code
  - New vector instruction set and 512-bit wide registers
  - Not optimized for processing serial code

Programming Considerations - Setting Expectations (2)

Thread setup and comm overhead

Off load

- Coprocessor comes with 8 GB of memory
  - Only ~7 GB is available to your program
    - The other ~1GB is used for data transfer and is accessible to your coprocessor code as buffers.
- Very short (low-latency) tasks not optimal for offload to the coprocessor
  - Costs that you need to amortize to make it worthwhile:
    - Code and data transfer
    - Process/thread creation
  - Fastest data transfers currently require careful data alignment
- This architecture is not optimized for serial performance

Intel® MIC Programming Considerations – This is not a GPU

- Very different memory architectures
  - The Intel MIC Architecture is not optimized for concurrent out-of-cache random memory accesses by large numbers of threads (GPUs are)
  - The Intel MIC Architecture has a “traditional” coherent-cache architecture
  - GPUs have a memory architecture specialized for localized “shared memory” processing
- “Threads” and “cores” mean something very different - GPU versions of these are limited and lighter-weight
- Each architecture (host CPU, Intel MIC Architecture, or GPU) is really good at some things, and not others
  - Because the Intel MIC Architecture is similar to the Intel® Xeon® processor, probably your best choice for further accelerating highly parallel and vectorized code developed on Intel Xeon processor

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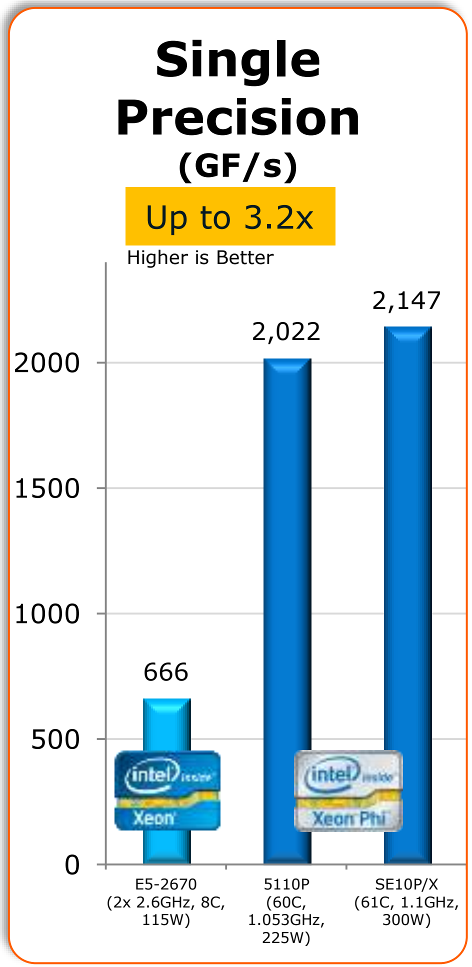
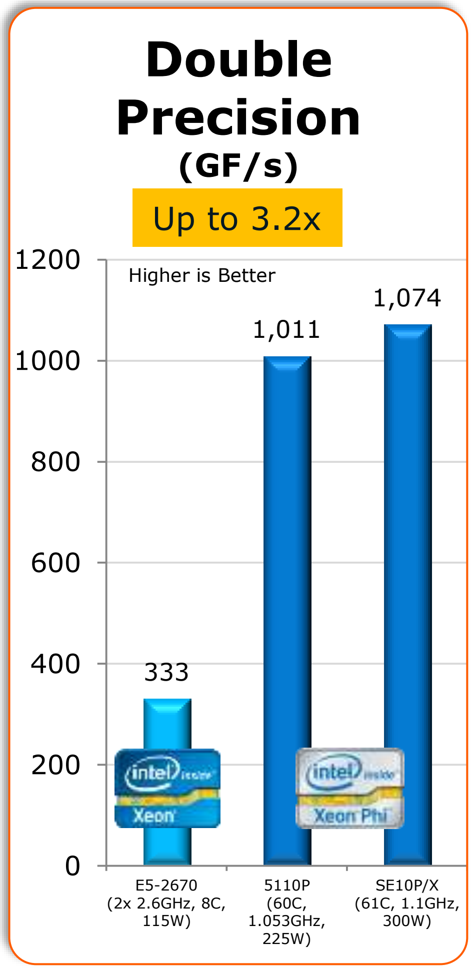
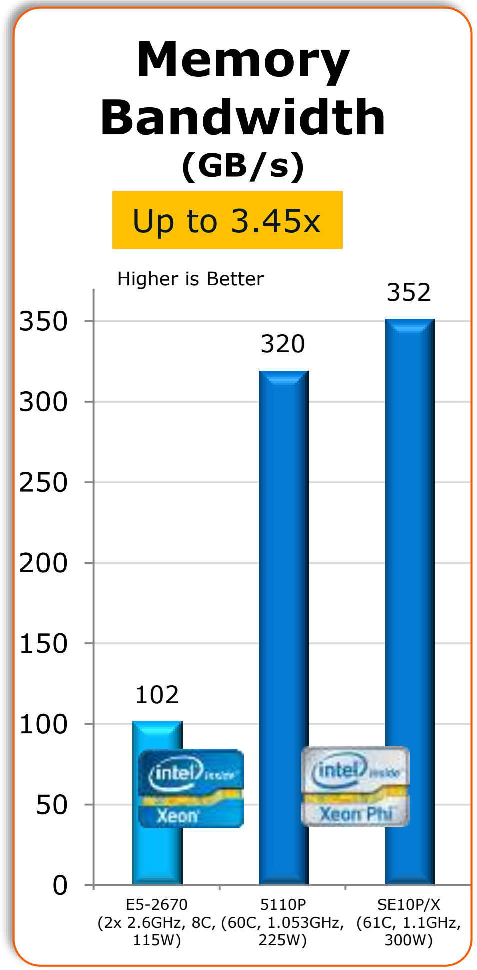
Theoretical Maximum

(Intel® Xeon® processor E5-2670 vs. Intel® Xeon Phi™ coprocessor 5110P & SE10P/X)

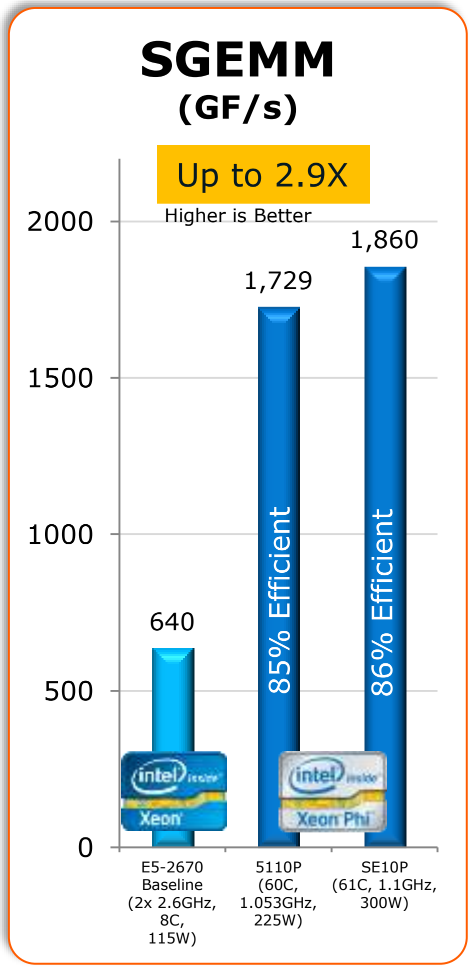


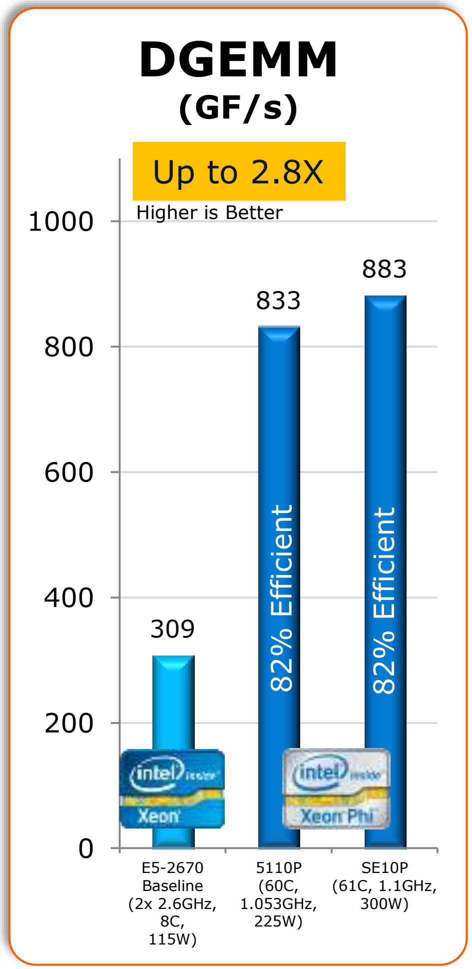


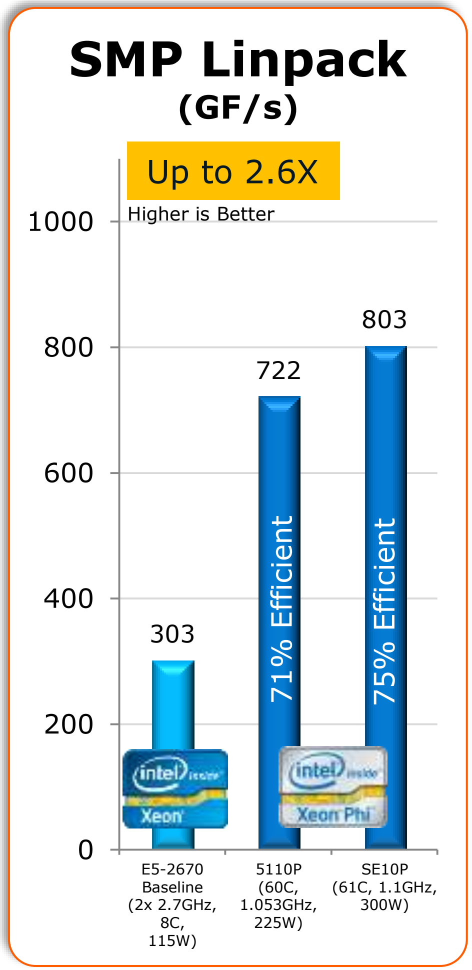


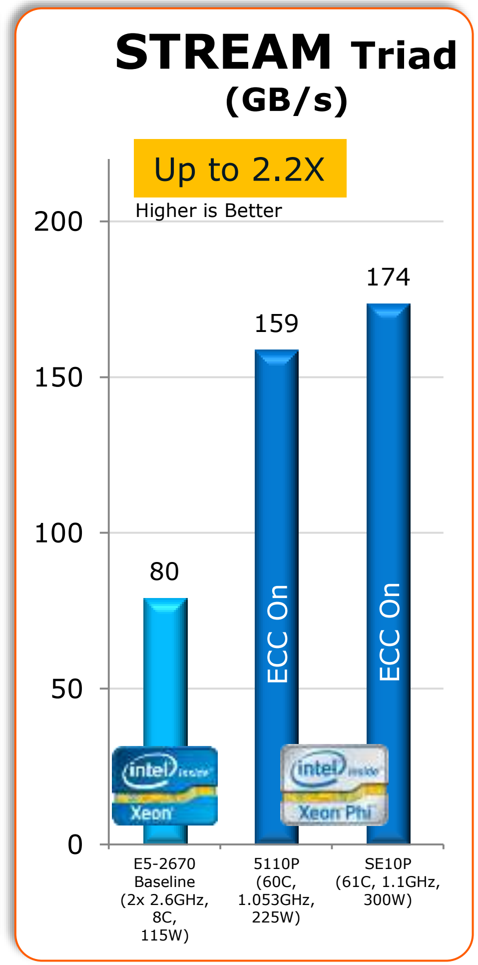
Source: Intel as of October 17, 2012 Configuration Details: Please reference slide speaker notes.
For more information go to http://www.intel.com/performance

Synthetic Benchmark Summary



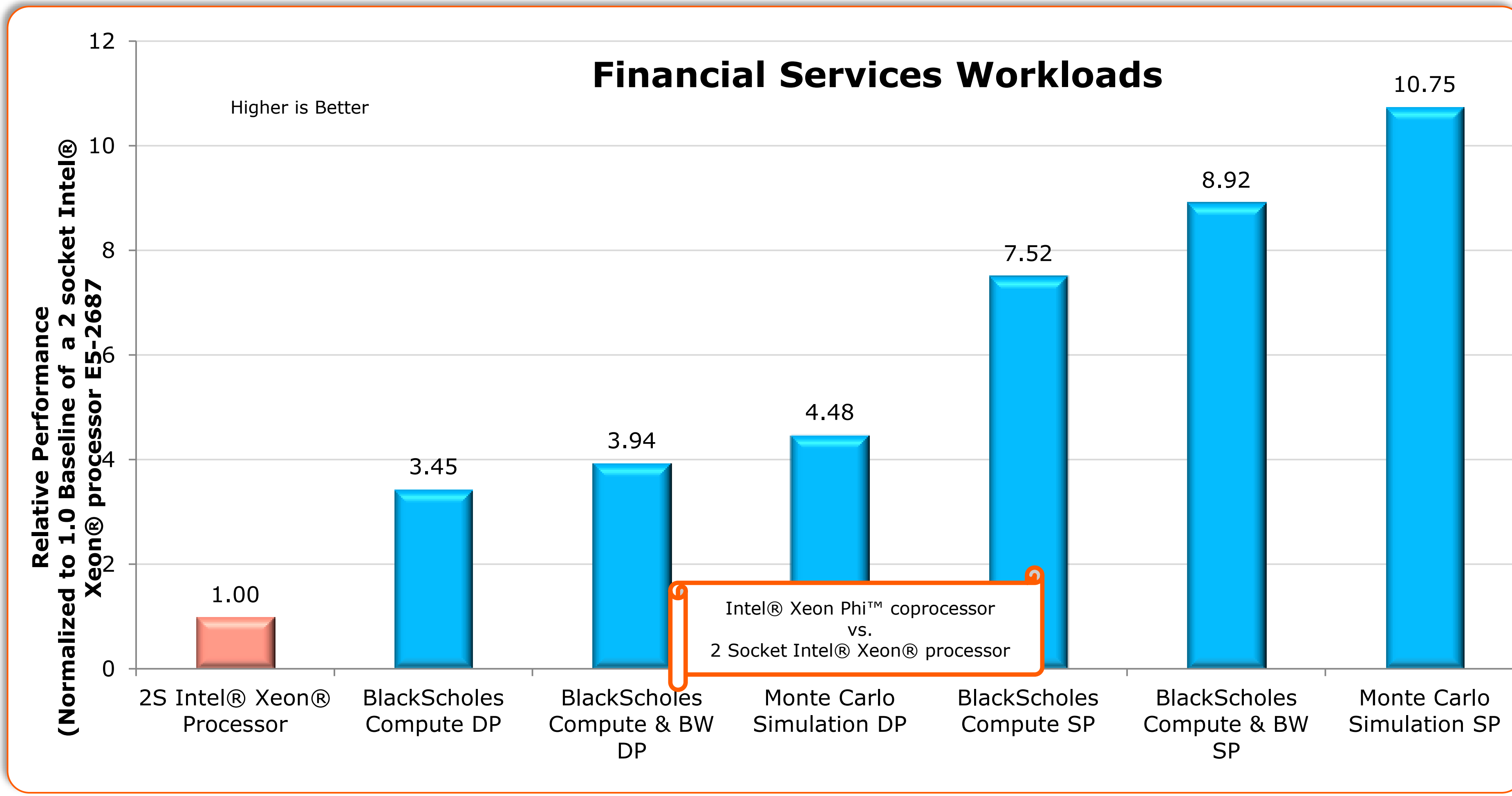






Coprocessor results: Benchmark runs 100% on coprocessor, no help from Intel® Xeon® processor host (aka native). For more information go to http://www.intel.com/performance

Intel® Xeon Phi™ Coprocessor vs. Intel® Xeon® Processor



Coprocessor results: Benchmark runs 100% on coprocessor, no help from Intel® Xeon® processor host (aka native). For more information go to http://www.intel.com/performance

Notes
1. 2 X Intel® Xeon® Processor E5-2670 (2.6GHz, 8C, 115W)
2. Intel® Xeon Phi™ coprocessor SE10 (ECC on) with pre-production SW stack

Higher SP results are due to certain Single Precision transcendental functions in the Intel® Xeon Phi™ coprocessor that are not present in the Intel® Xeon® processor

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Architecture Summary

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