February 2017 Newsletter

Upcoming Intel® PCC Meeting & IXPUG Conference

Join us for the Intel® PCC members only meeting on April 10, 2017 from 1:00PM-5:00PM (GMT) at University of Cambridge in Cambridge, England. This members only event is by direct invitation only and if you did not receive the email, please send a message to IPCC.Program.Office@intel.com.

This will be followed by the IXPUG Annual Spring Conference on April 11-14, 2017 in the same location. This is open to the public and requires registration**.** See the preliminary agenda on the website.

Intel® PCC Members Only Agenda:

Time	Title
1:00PM-1:30PM	Welcome
1:30PM-2:30PM	Intel® Hardware Roadmap
2:30PM-3:00PM	Break
3:00PM-4:00PM	Intel® Software Tools
4:00PM-4:30PM	New Intel® PCCs Introduction
4:30PM-5:00PM	Program Office Direction and Closing Remarks

Speaker Opportunities

We encourage you to share best practices, techniques, results, etc. at all of the following events. These events do require registration and have deadlines for abstract submissions.

Events and Details	Event Date	Deadlines	Speaking Opportunities
ISC 2017	Jun 18-22, 2017	Feb 15, 2017 Mar 3, 2017	Workshops, Tutorials, BoF Sessions, PhD Forum Research Posters, Project Posters
IXPUG Annual Spring Conference	Apr 10-14, 2017	Feb 26, 2017	Presentation Template and Abstract Submission
IXPUG ISC17 Workshop	Jun 22, 2017	Mar 31, 2017	Paper Submission
ACM Gordon Bell Prize	Nov 12-17, 2017	Apr 15, 2017	Nomination Submission Form
IXPUG Working Groups	Monthly	Monthly	Share your real-code experience and/or questions during the meeting or discussion forum.
IXPUG Discussion Forum	Anytime	Anytime	

Remote Intel® Xeon Phi™ Processor Cluster Access

We encourage you to optimize your application for multi-node by testing on the following clusters:

Texas Advanced Computing Center (TACC) Stampede Cluster:

- Click **HERE** and create a new account (**do not click on PI-eligible**) and follow the email instructions.
- Register account by emailing **ipcc.program.office@intel.com** with username.

Zuse Institute Berlin's (ZIB) Cluster:

- Request account by following the instructions on the application document, located **HERE**.

Intel® Application Development Cluster (Endeavor):

- Request account by completing the form located **HERE**.

Training Opportunities

Continue your growth as a developer by taking part in the following training opportunities.

Date	Location	Event
Feb 9, 2017	Virtual	Simplify your HPC System Software - Intel® HPC Orchestrator
Feb 13-24, 2017	Virtual	HOW Series "Deep Dive": Webinars on Performance Optimization
Feb 15, 2017	Seoul, South Korea	Intel HPC, Xeon Phi and Python
Feb 16, 2017	Seoul, South Korea	Intel HPC, Xeon Phi and Python
Feb 22-23, 2017	New Haven, CT	Optimization for Intel® Architecture and Machine Learning
Feb 23, 2017	Seoul, South Korea	Intel Xeon Phi and Tools Workshop
Feb 24, 2017	Seoul, South Korea	Intel Xeon Phi and Tools Workshop
Mar 8-11, 2017	Seattle, WA	SIGCSE Technical Symposium
Mar 10, 2017	Seoul, South Korea	Intel HPC Cluster Workshop
Apr 5, 2017	Virtual	Fast Insights to Optimized Vectorization and Memory
Apr 12, 2017	Virtual	Navigate Machine Learning & Deep Learning
Apr 19, 2017	Virtual	Get Onboard with the Intel® Parallel Studio XE 2018 Beta
Apr 26, 2017	Virtual	Deep Learning At Your Finger Tips
May 3, 2017	Virtual	Healthy, Happy Performing Clusters
May 10, 2017	Virtual	Snapshot Your Performance and Improve!
May 17, 2017	Virtual	HPC Applications Deserve High Performance Analytics
May 24, 2017	Virtual	Boosting Application Performance with Standard C++ Algorithm
May 31, 2017	Virtual	Accelerate Application Performance
Jun 7, 2017	Virtual	CPUs, GPUs, FPGAs: Managing the Alphabet Soup
Jun 14, 2017	Virtual	Julia for Machine Learning and Deep Learning

*NEW: Case Studies

Purdue University: **NEMO5** is used to model the behavior of electronics at the atomic level. Their work is able to unveil finer details of nanotransistors, and discusses how a physical Intel® Xeon Phi™ processor is partitioned into several virtual processors using the hStreams library and organized into a MPI parallelization scheme.

Argonne National Laboratory: **QMCPack** is used for computing the electric structure of atoms, molecules, and solids. The B-spline based orbital represented in QMC simulations of solids has been optimized and parallelized with nested threading on kernels, achieving results of 5.7x speedup on Intel's® Xeon Phi™ 7120P.

More News...

Learn more about recent work in the HPC community in the following articles:

- **Bolstering Lustre on ZFS: Highlights of Continuing Work**
- **3D Isotropic Acoustic Finite-Difference Wave Equation Code: Implementation and Analysis**
- **Intel® Xeon Phi™ Processor 7200 Family Memory Management Optimizations**
- **Research Report on In-Memory Computing**
- **Parallel Universe Magazine: The Present and Future of OpenMP***