December 2017 Newsletter

Intel® HPC Developer Conference & SC17 Highlights

We want to thank all of the speakers who participated in the Intel HPC Developer Conference and during SC17. The sharing of your experiences and best known methods in optimizing applications, using industry open standards truly helps the broader developer community to reach new discoveries fast.

- Intel® HPC Developer Conference;
- SC17 IXPUG BoF: Usability, Scalability and Productivity on Many-Core Processors: Intel Xeon Phi and Beyond
- SC17: Intel Demonstrates Future of AI Convergence and Delivers Targeted HPC Solutions for Workload Optimization
- SC17: Intel Boasts Record-Breaking Top500 Position with Fastest Ramp of a New Xeon Processor on List

Speaker & Publication Opportunities

There are several opportunities for you to share your learnings, best practices and techniques around the benefits you've received in leveraging Intel® architecture. We would like bring to your attention some key abstract submission deadlines for 2018 conferences and workshops. Feel free to submit abstracts to all that interest you.

Date	Location	Event
December 7, 2017	Frankfurt, Germany	ISC18 Workshops
December 22, 2017	Frankfurt, Germany	ISC18 Research Papers
February 13, 2018	Frankfurt, Germany	ISC18 Tutorials
February 21, 2018	Frankfurt, Germany	ISC18 PhD Forum
February 28, 2018	Frankfurt, Germany	ISC18 BoF
March 9, 2018	Frankfurt, Germany	ISC18 Research Posters
March 16, 2018	Frankfurt, Germany	ISC18 Project Posters
January 28 -31, 2018	Tokyo Japan	IXPUG HPC Asia 2018

April 22,-25, 2018	Thuwal, Saudi Arabia	IXPUG Workshop at KAUST

Free Training Opportunities: Join, Learn and Excel

Join us at any of these upcoming educational workshops and conferences and learn about new Parallel Programming concepts, Intel® Libraries, Software Development tools and Artificial Intelligence frameworks. They are open to the public and free to attend.

Date	Location	Event
December 5, 2017	Germany	Software Developers Conference
December 8, 2017	Seoul, South Korea	Dae Han Code Mod Workshop
December 21, 2017	Harbin, PRC	Paratera Code Mod Workshop
Jan 16-18, 2018	Virtual	Leverage multi-core performance using Intel® Threading Building Blocks (Intel® TBB) by NAG
Jan 28-31, 2018	Tokyo, Japan	IXPUG Workshop at HPC Asia

Access to Intel® Xeon Phi™ Processor

We encourage all Intel PCC members to leverage the TACC cluster to testing your optimized application for multi-node. To request access, please click **HERE** and create a new account (do not click on PI-eligible) and follow the email instructions. Please email the **ipcc.program.office@intel.com** account and include your username in the communication.

More News...

Check out these latest HPC news stories:

- Julia Language Delivers Petascale HPC Performance
- New Intel® Xeon® Scalable Processor Scalable Family Improves HPC Performance
- Intel looks to Nervana as a path to artificial intelligence
- The Future Is Scalable—Intel® Scalable System Framework (Intel® SSF)
- Unleashing High-Performance Computing Today and Tomorrow