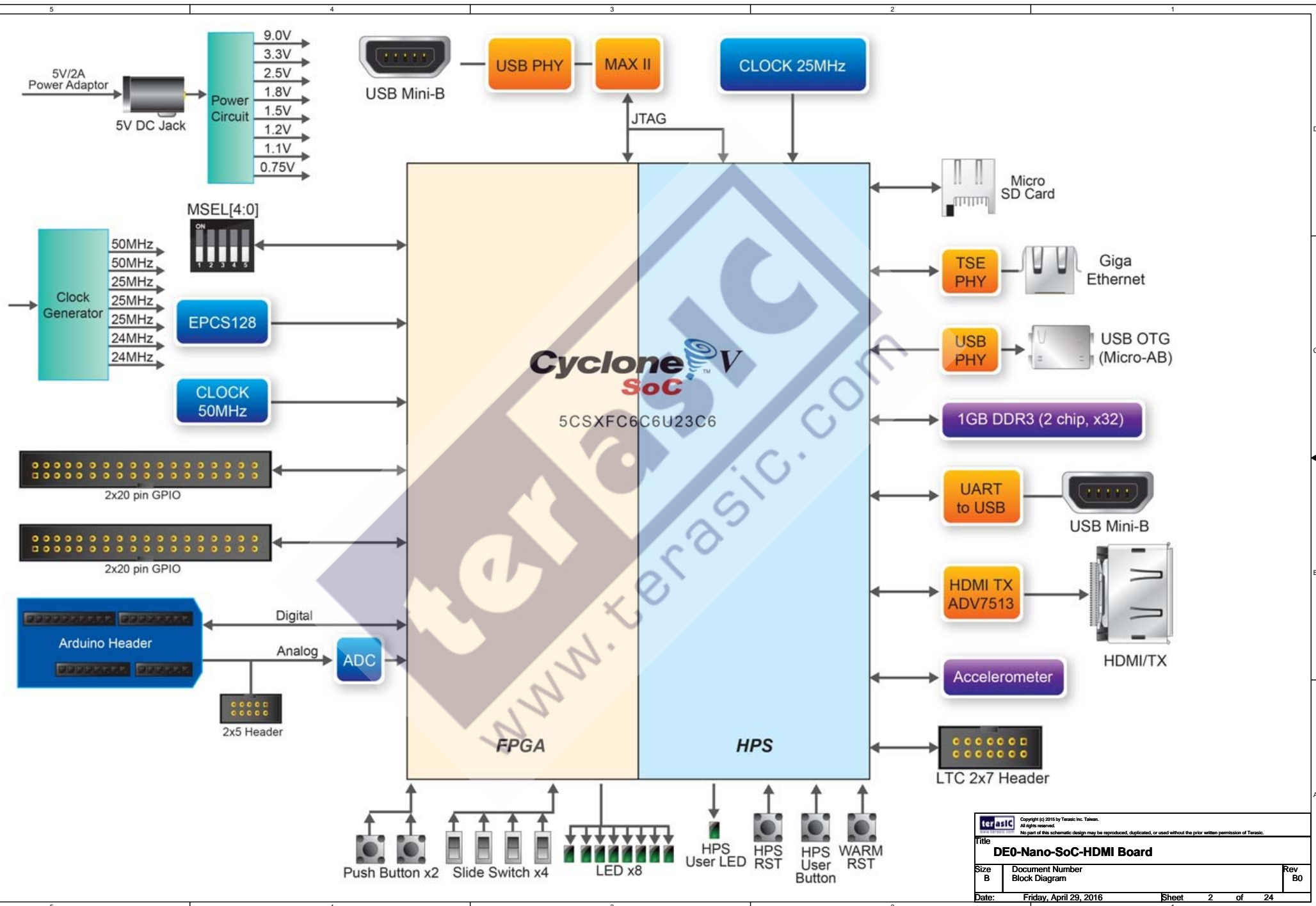


Cyclone V SoC Development & Education Board (DE0-Nano-SoC-HDMI)

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Title DE0-Nano-SoC-HDMI Board	
Size B	Document Number Block Diagram
Date: Friday, April 29, 2016	Rev B0
Sheet 2	of 24

U1I
CYCLONE V SoC BANK 3

Bank 3A
VCCIO = 3.3V

GPIO 0 D32	Y11	IO_3A/PR_ERROR/DIFFIO_RX_B7P
GPIO 0 D35	AA11	IO_3A/PR_DONE/DIFFIO_RX_B7N
GPIO 0 D10	AD5	IO_3A/DIFFIO_TX_B8P/DQ1B
GPIO 0 D13	AE6	IO_3A/PR_READY/DIFFIO_TX_B8N/DQ1B

Bank 3B
VCCIO = 3.3V

HDMI_TX_D16	AE4	IO_3B/DIFFIO_TX_B9P/B_WEN/DQ2B	IO_3B/DIFFIO_TX_B17P/B_BA_0/DQ3B
GPIO 0 D8	AF4	IO_3B/DIFFIO_TX_B9N/GND	IO_3B/DIFFIO_TX_B17N/GND
HDMI_TX_D5	AD10	IO_3B/DIFFIO_RX_B10P/B_A_14/DQ2B	IO_3B/DIFFIO_RX_B18P/B_BA_1/DQ3B
HDMI_TX_D10	AE9	IO_3B/DIFFIO_RX_B10N/B_A_15/DQ2B	IO_3B/DIFFIO_RX_B18N/B_BA_2/DQ3B
HDMI_LRCLK	T11	IO_3B/DIFFIO_RX_B11P/B_CSN_0/DQS2B	IO_3B/DIFFIO_RX_B19P/B_CK/DQS3B
HDMI_MCLK	U11	IO_3B/DIFFIO_RX_B11N/B_CSN_1/DQS2B	IO_3B/DIFFIO_RX_B19N/B_CKN/DQS3B
HDMI_TX_D12	AE7	IO_3B/DIFFIO_TX_B12P/B_A_12	IO_3B/DIFFIO_TX_B20P/B_A_6
HDMI_TX_D14	AF8	IO_3B/DIFFIO_TX_B12N/B_A_13/DQ2B	IO_3B/DIFFIO_TX_B20N/B_A_7/DQ3B
HDMI_TX_D23	AE8	IO_3B/DIFFIO_TX_B13P/B_A_10/DQ2B	
HDMI_TX_D22	AF9	IO_3B/DIFFIO_TX_B13N/B_A_11/DQ2B	
HDMI_TX_D4	AD11	IO_3B/DIFFIO_RX_B14P/B_A_8/DQ2B	IO_3B/DIFFIO_RX_B22P/B_A_4/DQ3B
HDMI_TX_D6	AE11	IO_3B/DIFFIO_RX_B14N/B_A_9/DQ2B	IO_3B/DIFFIO_RX_B22N/B_A_5/DQ3B

HDMI_TX_D15	AF5	IO_3B/DIFFIO_TX_B16P/B_CASN/DQ2B	IO_3B/DIFFIO_TX_B24P/B_A_0/DQ3B
HDMI_TX_D13	AF6	IO_3B/DIFFIO_TX_B16N/B_RASN/DQ2B	IO_3B/DIFFIO_TX_B24N/B_A_1/DQ3B

5CSXFC6C6U23C6N

U1K
CYCLONE V SoC BANK 5

Bank 5A
VCCIO = 3.3V

LED4	AF26	IO_5A/RZQ_1/DIFFIO_TX_R1P/DQ1R
LED5	AE26	IO_5A/PR_REQUEST/DIFFIO_TX_R1N/DQ1R

Bank 5B
VCCIO = 3.3V

GPIO 0 D30	AB25	IO_5B/RZQ_2/DIFFIO_TX_R24N
------------	------	----------------------------

5CSXFC6C6U23C6N

U1J
CYCLONE V SoC BANK 4

Bank 4A
VCCIO = 3.3V

Arduino_Reset_n	AH7	IO_4A/RZQ_0/DIFFIO_TX_B25N
Arduino_IO6	AG8	IO_4A/DIFFIO_RX_B25P/B_DQ_2/DQ4B

Arduino_IO0	AG13	IO_4A/DIFFIO_RX_B26P/B_DQ_1/DQ4B	IO_4A/DIFFIO_RX_B42P/B_DQ_17/DQ6B
Arduino_IO1	AF13	IO_4A/DIFFIO_RX_B26N/B_DQ_0/DQ4B	IO_4A/DIFFIO_RX_B42N/B_DQ_16/DQ6B
Arduino_IO4	U14	IO_4A/DIFFIO_RX_B27P/B_DQS_0/DQS4B	IO_4A/DIFFIO_RX_B43P/B_DQS_2/DQS6B
Arduino_IO5	U13	IO_4A/DIFFIO_RX_B27N/B_DQS_0/DQS4B	IO_4A/DIFFIO_RX_B43N/B_DQS_2/DQS6B
Arduino_IO3	AG9	IO_4A/DIFFIO_TX_B28P/B_ODT_0	IO_4A/DIFFIO_TX_B44P/B_RESETN
Arduino_IO7	AH8	IO_4A/DIFFIO_TX_B28N/B_DQ_3/DQ4B	IO_4A/DIFFIO_TX_B44N/B_DQ_19/DQ6B
Arduino_IO2	AG10	IO_4A/DIFFIO_TX_B29P/B_DQ_6/DQ4B	IO_4A/DIFFIO_TX_B45P/B_DQ_22/DQ6B
Arduino_IO14	AH9	IO_4A/DIFFIO_TX_B29N/B_ODT_1/DQ4B	IO_4A/DIFFIO_TX_B45N/GND/DQ6B
Arduino_IO10	AF15	IO_4A/DIFFIO_RX_B30P/B_DQ_5/DQ4B	IO_4A/DIFFIO_RX_B46P/B_DQ_21/DQ6B
Arduino_IO9	AE15	IO_4A/DIFFIO_RX_B30N/B_DQ_4/DQ4B	IO_4A/DIFFIO_RX_B46N/B_DQ_20/DQ6B

Arduino_IO15	AG11	IO_4A/DIFFIO_TX_B32P/B_DM_0/DQ4B	IO_4A/DIFFIO_TX_B48P/B_DM_2/DQ6B
Arduino_IO12	AH11	IO_4A/DIFFIO_TX_B32N/B_DQ_7/DQ4B	IO_4A/DIFFIO_TX_B48N/B_DM_23/DQ6B

Arduino_IO13	AH12	IO_4A/DIFFIO_TX_B33P/B_DQ_10/DQ5B	IO_4A/DIFFIO_TX_B49P/B_DQ_26/DQ7B
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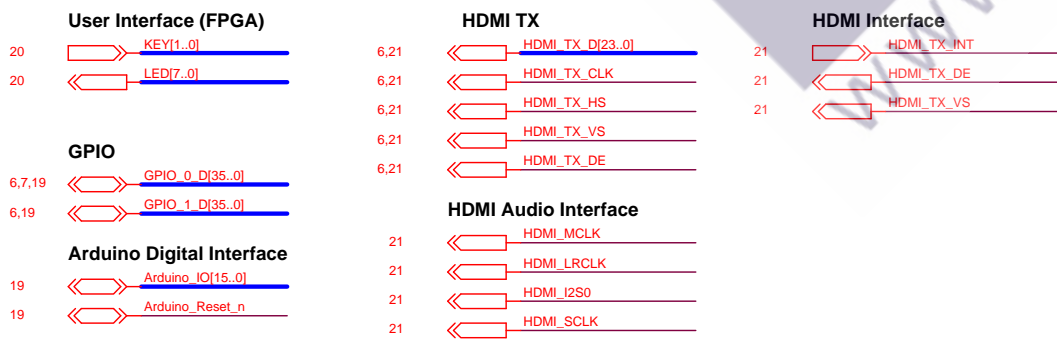
Arduino_IO8	AF17	IO_4A/DIFFIO_RX_B34P/B_DQ_9/DQ5B	IO_4A/DIFFIO_RX_B50P/B_DQ_25/DQ7B
Arduino_IO11	AG16	IO_4A/DIFFIO_RX_B34N/B_DQ_8/DQ5B	IO_4A/DIFFIO_RX_B50N/B_DQ_24/DQ7B
GPIO 0 D27	W14	IO_4A/DIFFIO_RX_B35P/B_DQS_1/DQS5B	IO_4A/DIFFIO_RX_B51P/B_DQS_3/DQS7B
HDMI_TX_VS	V13	IO_4A/DIFFIO_RX_B35N/B_DQS_1/DQS5B	IO_4A/DIFFIO_RX_B51N/B_DQS_3/DQS7B
GPIO 0 D11	AG14	IO_4A/DIFFIO_TX_B36P/B_CKE_1	IO_4A/DIFFIO_TX_B52N/B_DQ_27/DQ7B
GPIO 0 D5	AH13	IO_4A/DIFFIO_TX_B36N/B_DQ_11/DQ5B	IO_4A/DIFFIO_TX_B53P/B_DQ_30/DQ7B
GPIO 1 D32	AG15	IO_4A/DIFFIO_TX_B37P/B_DQ_14/DQ5B	IO_4A/DIFFIO_TX_B53N/GND/DQ7B
GPIO 0 D7	AH14	IO_4A/DIFFIO_TX_B37N/B_CKE_0/DQ5B	IO_4A/DIFFIO_RX_B54P/B_DQ_29/DQ7B
GPIO 0 D19	AD17	IO_4A/DIFFIO_RX_B38P/B_DQ_13/DQ5B	IO_4A/DIFFIO_RX_B54N/B_DQ_28/DQ7B
GPIO 1 D35	AE17	IO_4A/DIFFIO_RX_B38N/B_DQ_12/DQ5B	

KEY0	AH17	IO_4A/DIFFIO_TX_B40P/B_DM_1/DQ5B	IO_4A/DIFFIO_TX_B56P/B_DM_3/DQ7B
KEY1	AH16	IO_4A/DIFFIO_TX_B40N/B_DQ_15/DQ5B	IO_4A/DIFFIO_TX_B56N/B_DM_31/DQ7B

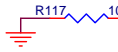
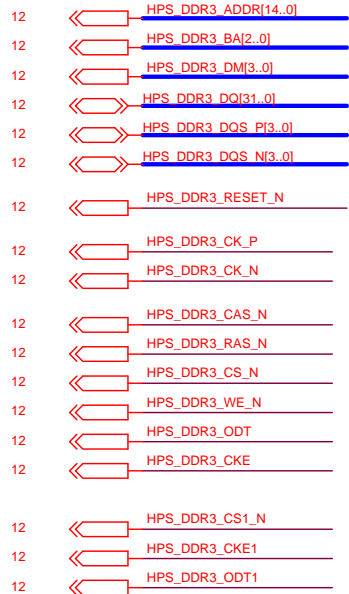
		IO_4A/DIFFIO_TX_B57P/B_DQ_34/DQ8B	
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		IO_4A/DIFFIO_RX_B59P/B_DQS_4/DQS8B	IO_4A/DIFFIO_RX_B59N/B_DQS_4/DQS8B
		IO_4A/DIFFIO_TX_B60N/B_DQ_35/DQ8B	IO_4A/DIFFIO_TX_B61P/B_DQ_38/DQ8B
		IO_4A/DIFFIO_TX_B61P/B_DQ_38/DQ8B	IO_4A/DIFFIO_TX_B61N/GND/DQ8B
		IO_4A/DIFFIO_RX_B62P/B_DQ_37/DQ8B	IO_4A/DIFFIO_RX_B62N/B_DQ_36/DQ8B
		IO_4A/DIFFIO_TX_B64P/B_DM_4/DQ8B	IO_4A/DIFFIO_TX_B64N/B_DQ_39/DQ8B

			IO_4A/DIFFIO_TX_B64P/B_DM_4/DQ8B	AF27	GPIO 1 D7
			IO_4A/DIFFIO_TX_B64N/B_DQ_39/DQ8B	AF28	GPIO 1 D5

5CSXFC6C6U23C6N



DDR3 Interface (HPS)



U1L

CYCLONE V SoC BANK 6 (HPS)

Bank 6A
VCCIO = 1.5V

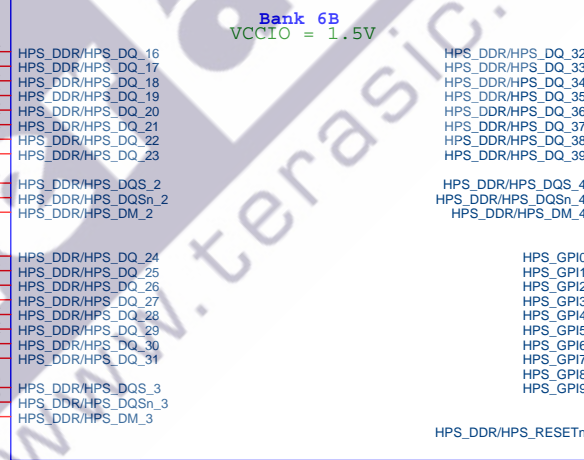
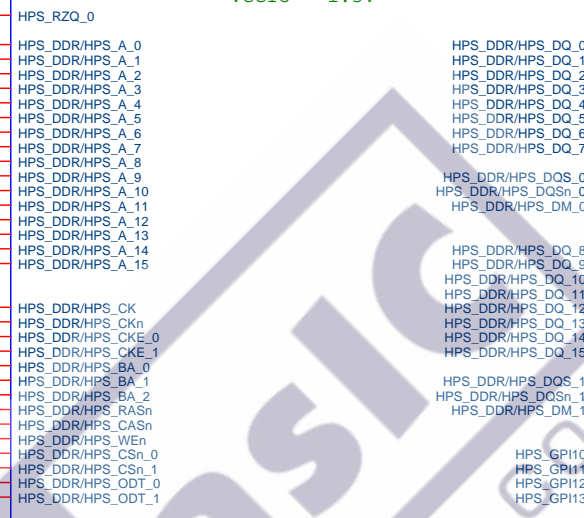
HPS_DDR3_ADDR0	C28
HPS_DDR3_ADDR1	B28
HPS_DDR3_ADDR2	E26
HPS_DDR3_ADDR3	D26
HPS_DDR3_ADDR4	J21
HPS_DDR3_ADDR5	J20
HPS_DDR3_ADDR6	C26
HPS_DDR3_ADDR7	B26
HPS_DDR3_ADDR8	F26
HPS_DDR3_ADDR9	F25
HPS_DDR3_ADDR10	A24
HPS_DDR3_ADDR11	B24
HPS_DDR3_ADDR12	D24
HPS_DDR3_ADDR13	C24
HPS_DDR3_ADDR14	G23
HPS_DDR3_ADDR14	F24

HPS_DDR3_CK_P	N21
HPS_DDR3_CK_N	N20
HPS_DDR3_CKE	L28
HPS_DDR3_CKE1	K28
HPS_DDR3_BA0	A27
HPS_DDR3_BA1	H25
HPS_DDR3_BA2	G25
HPS_DDR3_RAS_N	A25
HPS_DDR3_CAS_N	A26
HPS_DDR3_WE_N	E25
HPS_DDR3_CS_N	L21
HPS_DDR3_CS1_N	L20
HPS_DDR3_ODT	D28
HPS_DDR3_ODT1	G26

HPS_DDR3_DQ16	N24
HPS_DDR3_DQ17	N25
HPS_DDR3_DQ18	T28
HPS_DDR3_DQ19	U28
HPS_DDR3_DQ20	N26
HPS_DDR3_DQ21	N27
HPS_DDR3_DQ22	R27
HPS_DDR3_DQ23	V27
HPS_DDR3_DQS_P2	T19
HPS_DDR3_DQS_N2	T18
HPS_DDR3_DM2	W28

HPS_DDR3_DQ24	R26
HPS_DDR3_DQ25	R25
HPS_DDR3_DQ26	AA28
HPS_DDR3_DQ27	W26
HPS_DDR3_DQ28	R24
HPS_DDR3_DQ29	T24
HPS_DDR3_DQ30	Y27
HPS_DDR3_DQ31	AA27

HPS_DDR3_DQS_P3	U19
HPS_DDR3_DQS_N3	T20
HPS_DDR3_DM3	AB28



5CSXFC6C6U23C6N

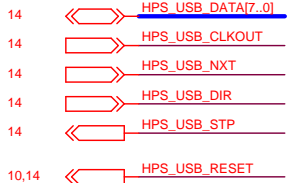
J25	HPS_DDR3_DQ0
J24	HPS_DDR3_DQ1
E28	HPS_DDR3_DQ2
D27	HPS_DDR3_DQ3
J26	HPS_DDR3_DQ4
K26	HPS_DDR3_DQ5
G27	HPS_DDR3_DQ6
F28	HPS_DDR3_DQ7
R17	HPS_DDR3_DQS_P0
R16	HPS_DDR3_DQS_N0
G28	HPS_DDR3_DM0
K25	HPS_DDR3_DQ8
L25	HPS_DDR3_DQ9
J27	HPS_DDR3_DQ10
J28	HPS_DDR3_DQ11
M27	HPS_DDR3_DQ12
M26	HPS_DDR3_DQ13
M28	HPS_DDR3_DQ14
N28	HPS_DDR3_DQ15
R19	HPS_DDR3_DQS_P1
R18	HPS_DDR3_DQS_N1
P28	HPS_DDR3_DM1
U15	
U16	
AC27	
V24	

T26	
U25	
AC28	
V25	
V19	
V20	
AE27	
AD28	
V18	
V17	
AE28	
M25	
K27	
R20	
R21	
R28	
P26	
T17	
T16	
Y28	
Y26	
HPS_GPI9	
V28	HPS_DDR3_RESET_N

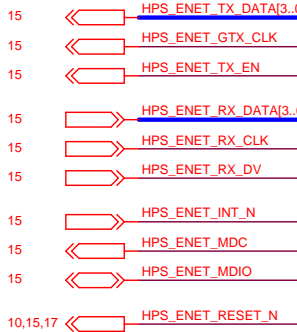
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Title		
DE0-Nano-Soc-HDMI Board		
Size	Document Number	Rev
B	FPGA Bank 6	B0
Date:	Monday, March 21, 2016	Sheet 4 of 24

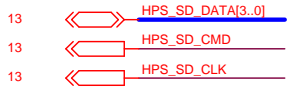
UBS PHY Interface (ULPI)



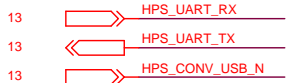
Ethernet PHY Interface (RGMII)



SD Card Interface



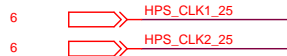
UART Interface



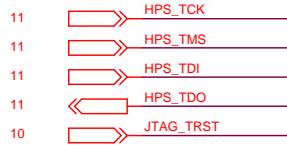
HPS Reset



HPS Clock



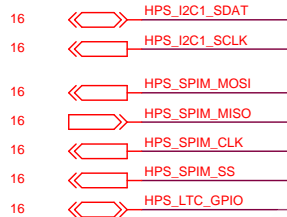
HPS JTAG INTERFACE



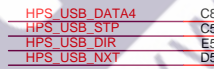
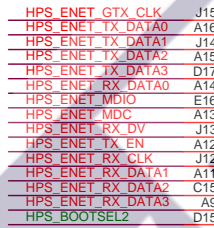
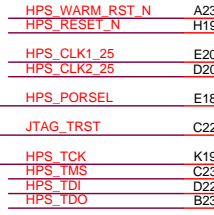
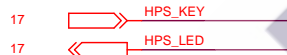
Accelerometer Interface



LTC Interface

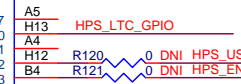
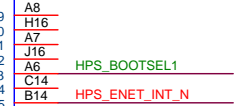
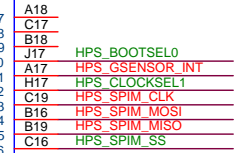
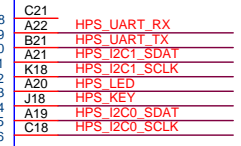
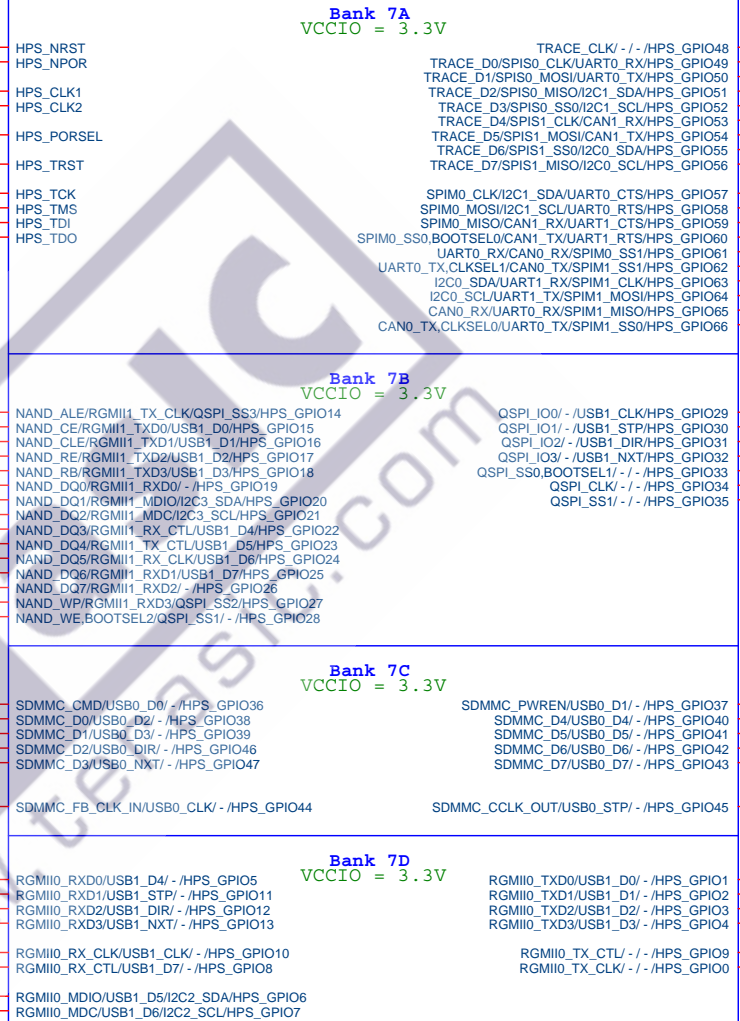


HPS Key and LED



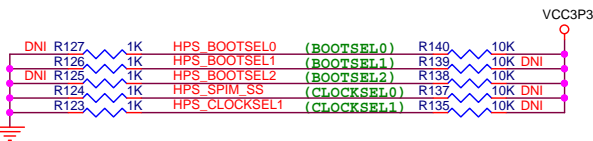
U1M

CYCLONE V SoC BANK 7 (HPS)



5CSXFC6C6U23C6N

Default Setting: BOOTSEL[2:0]=101 (Boot from SD CARD)
 CLKSEL[1:0] =00



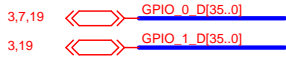
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Title: **DE0-Nano-Soc-HDMI Board**

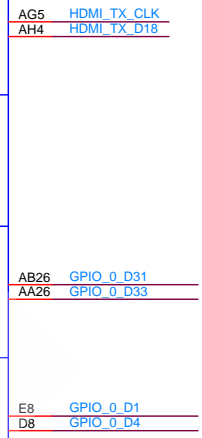
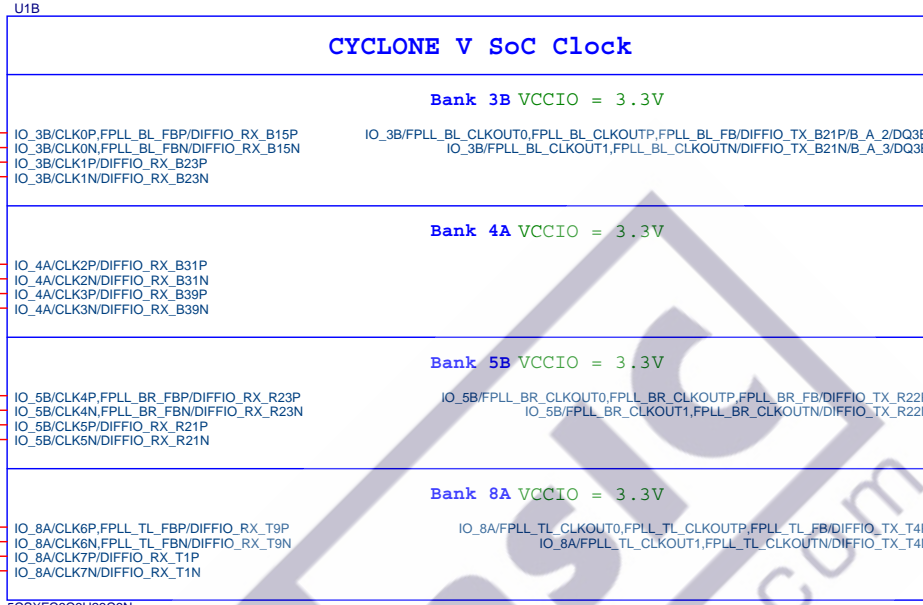
Size: B Document Number: FPGA Bank 7 Rev: B0

Date: Monday, March 21, 2016 Sheet: 5 of 24

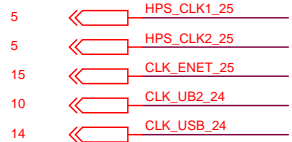
GPIO



User Interface (FPGA)



Clock Generator

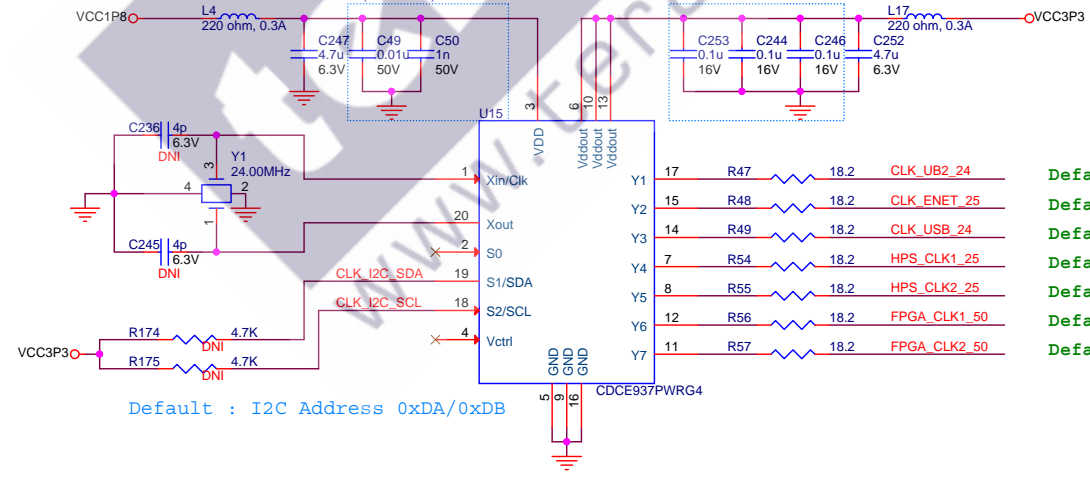


Factory Default Configuration:

- 50MHz x2
- 25MHz x3
- 24MHz x2

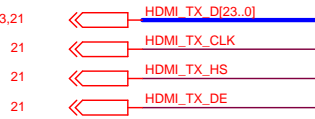
CAD Note: Place near pin 3 and 5 (C3 & C322)

CAD Note: Place near IC power pin



- 17 R47 18.2 CLK_UB2_24 Default: 24MHz
- 15 R48 18.2 CLK_ENET_25 Default: 25MHz
- 14 R49 18.2 CLK_USB_24 Default: 24MHz
- 7 R54 18.2 HPS_CLK1_25 Default: 25MHz
- 8 R55 18.2 HPS_CLK2_25 Default: 25MHz
- 12 R56 18.2 FPGA_CLK1_50 Default: 50MHz
- 11 R57 18.2 FPGA_CLK2_50 Default: 50MHz

HDMI TX



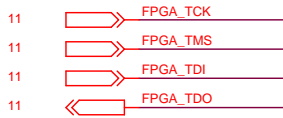
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Title: **DE0-Nano-Soc-HDMI Board**

Size B	Document Number FPGA Clock and Clock Generator	Rev B0
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Date: Thursday, April 28, 2016 Sheet 6 of 24

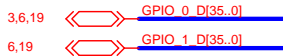
FPGA JTAG INTERFACE



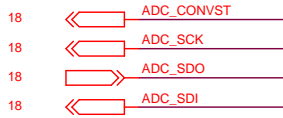
USB Blaster



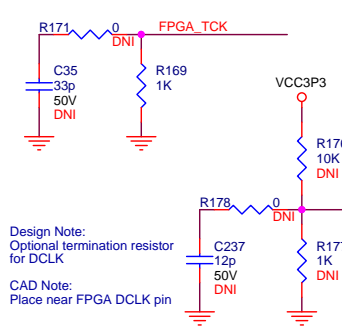
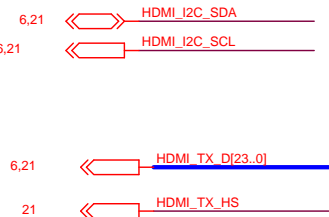
GPIO



ADC

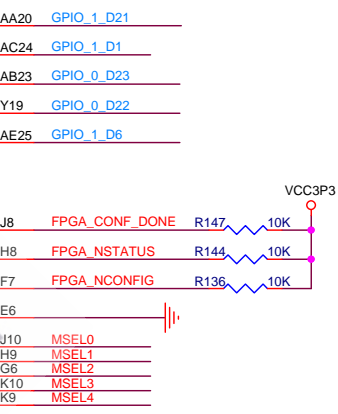
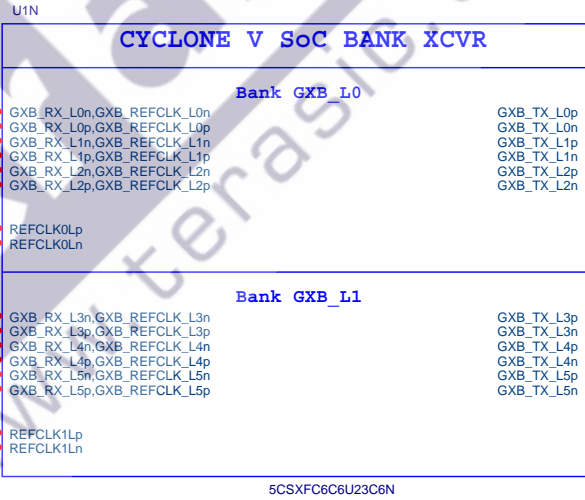
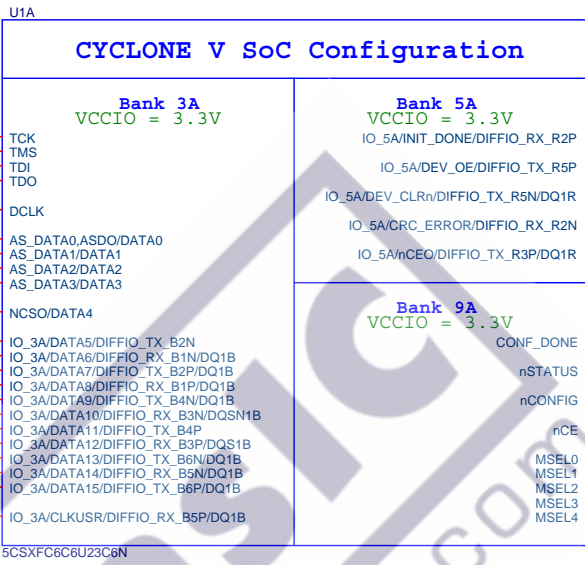
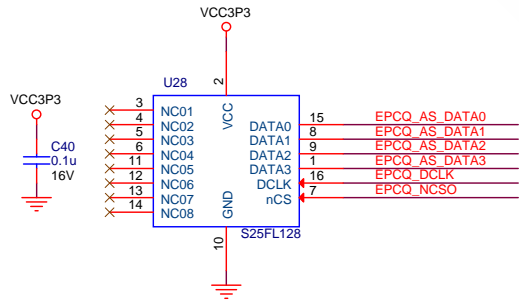


I2C Interface

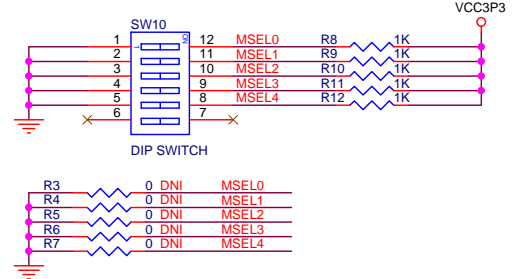


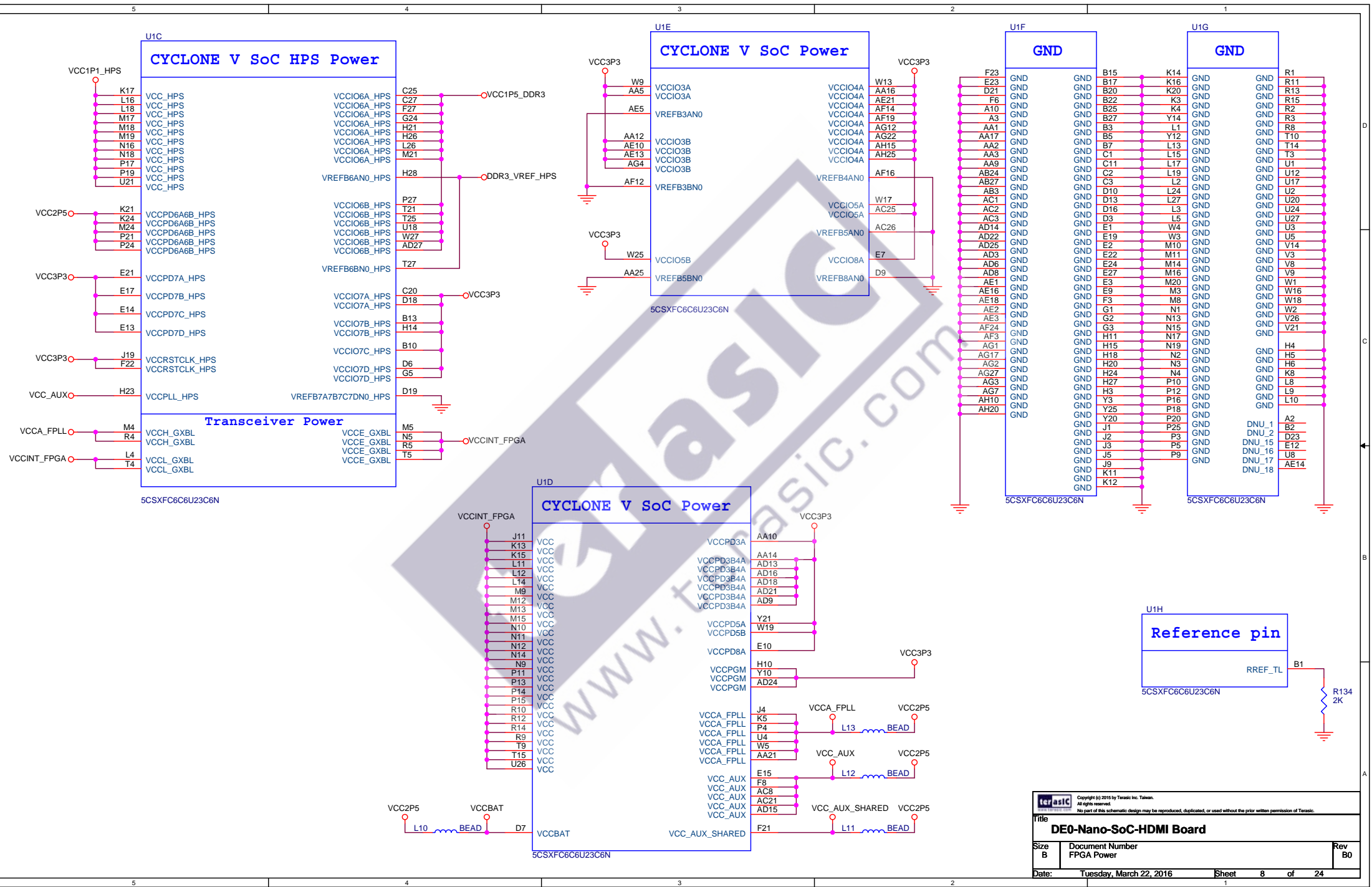
Design Note:
Optional termination resistor for DCLK

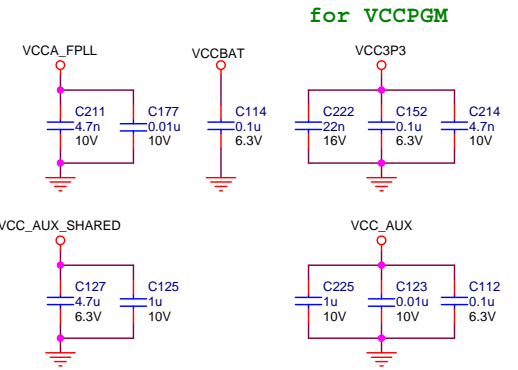
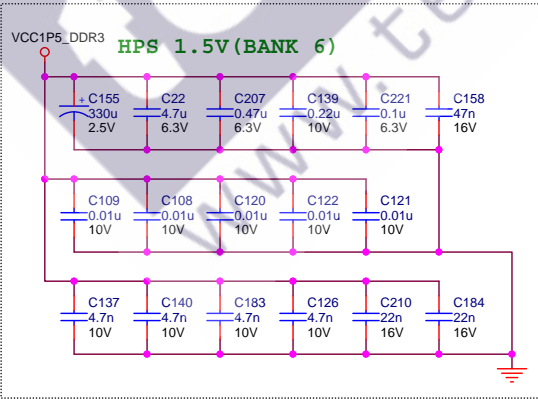
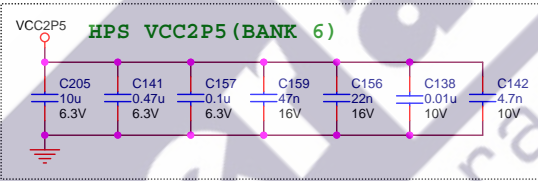
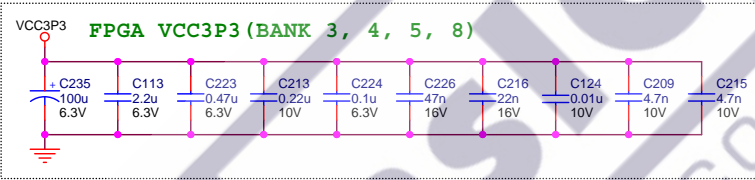
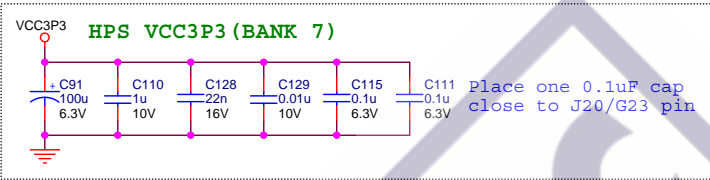
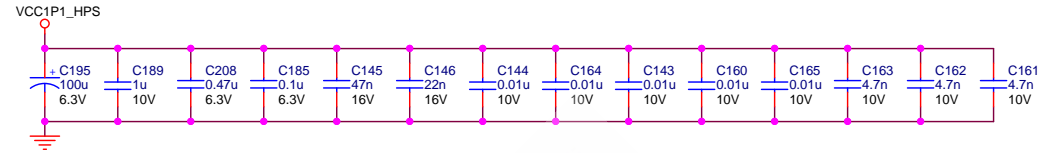
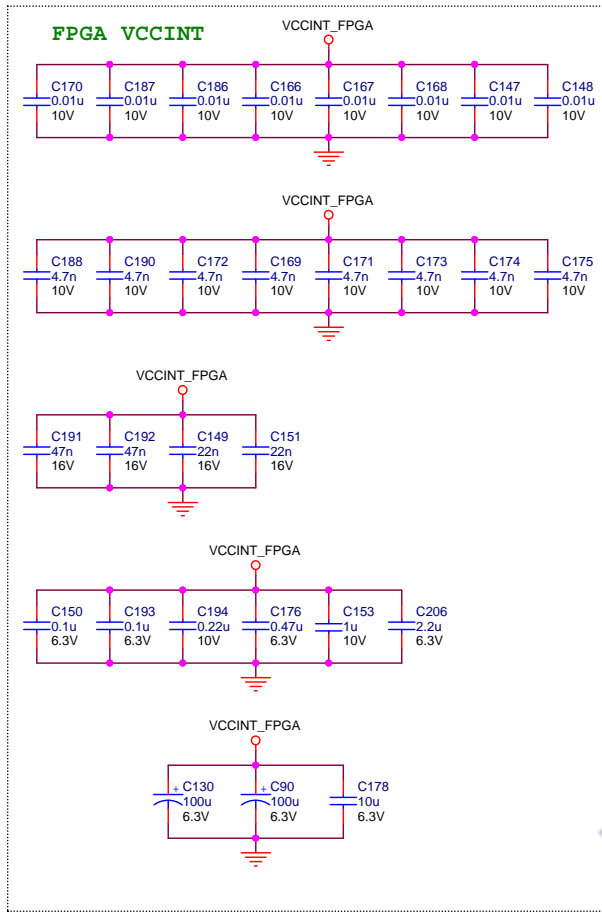
CAD Note:
Place near FPGA DCLK pin

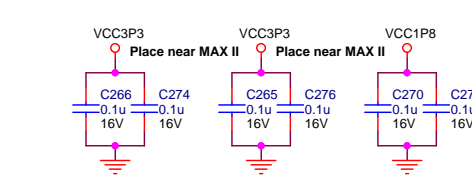
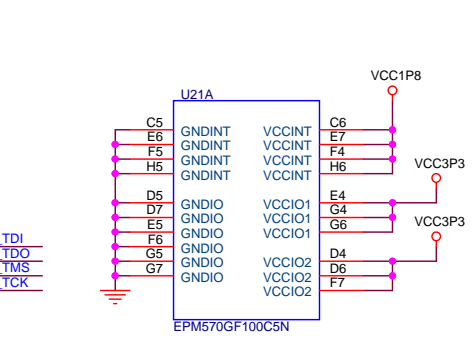
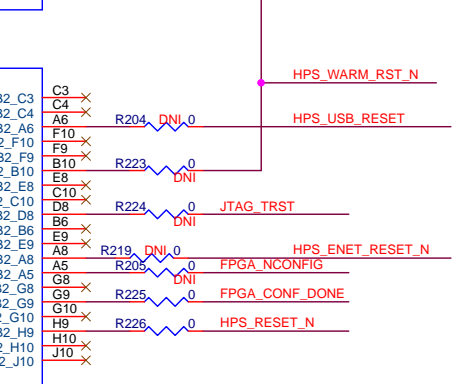
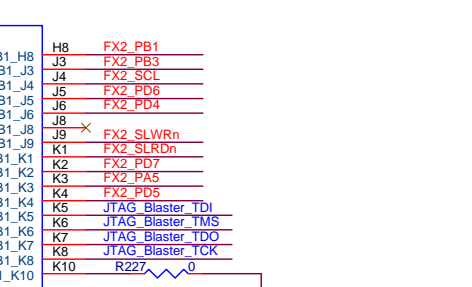
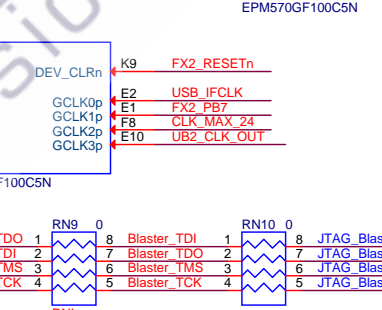
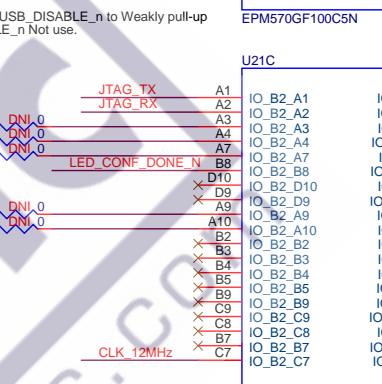
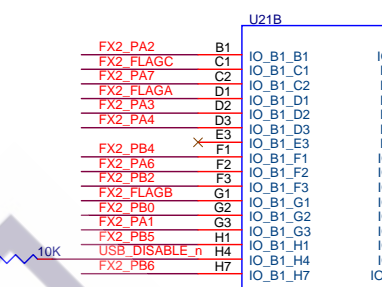
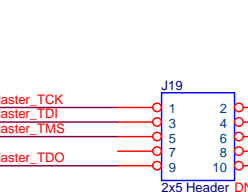
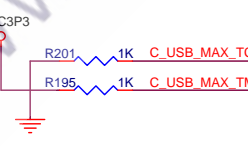
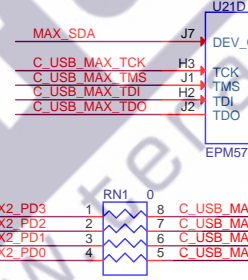
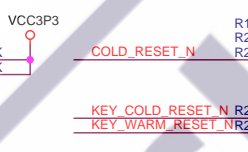
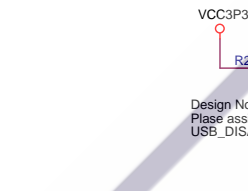
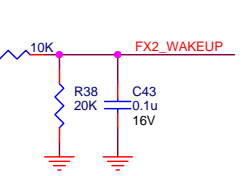
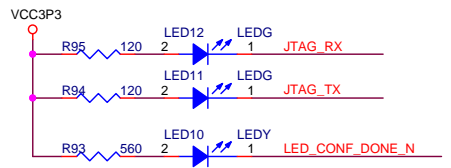
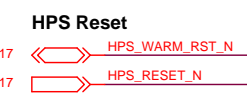
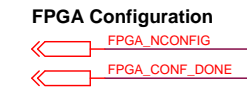
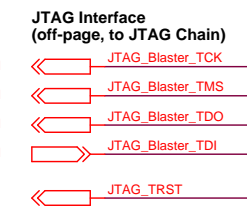
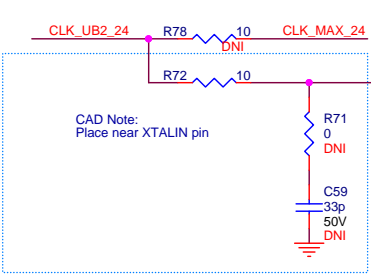
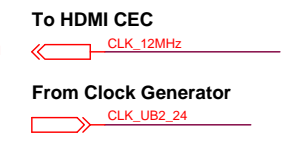
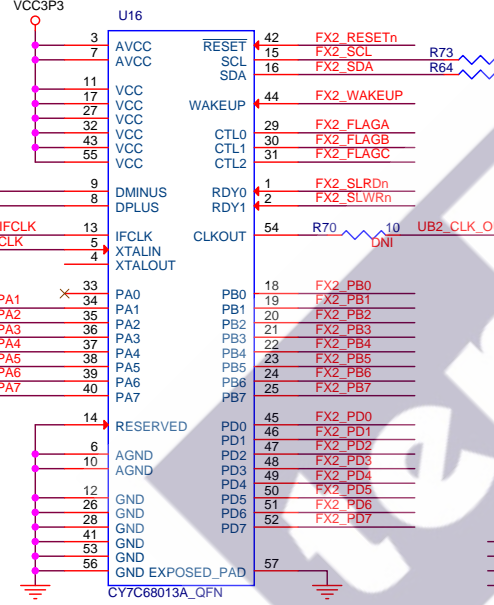
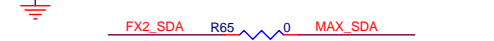
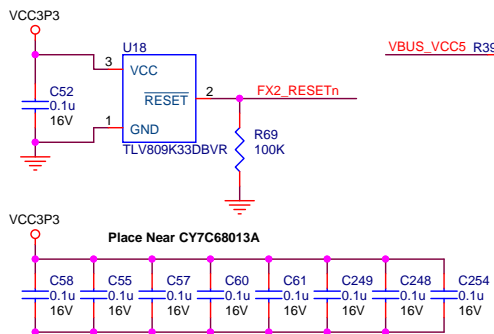
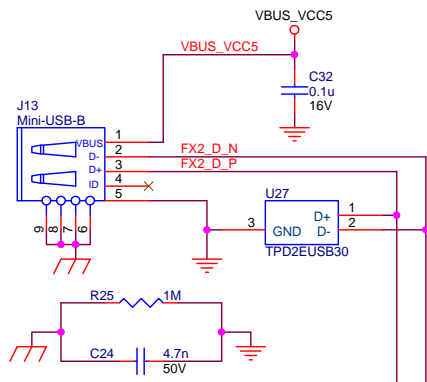


Default Setup MSEL[4:0] = 10010, AS Fast Mode









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Title DE0-Nano-Soc-HDMI Board

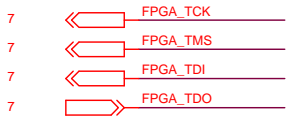
Size B **Document Number** USB Blaster II **Rev** B0

Date: Thursday, April 28, 2016 **Sheet** 10 of 24

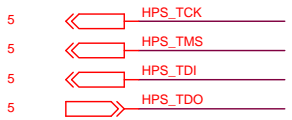
USB Blaster



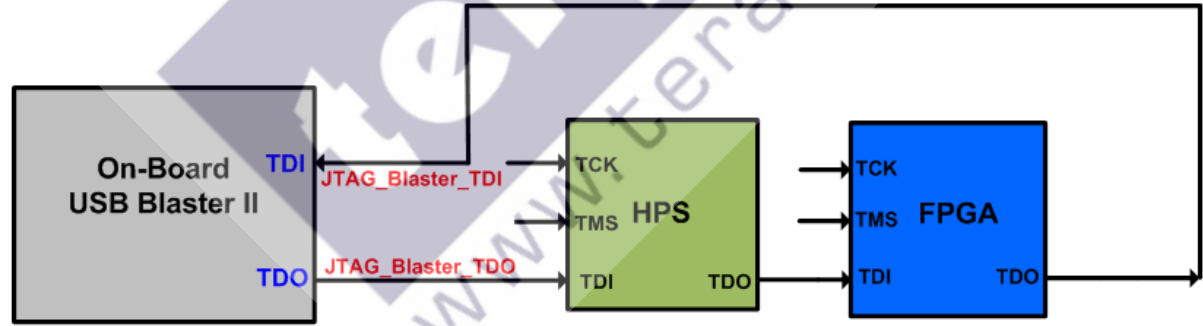
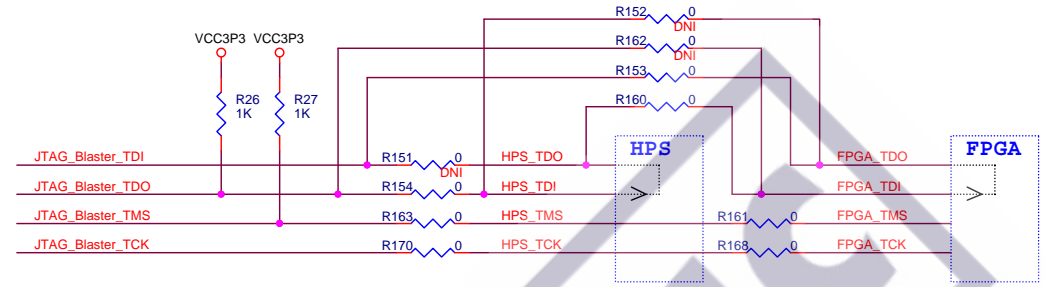
FPGA JTAG INTERFACE



HPS JTAG INTERFACE



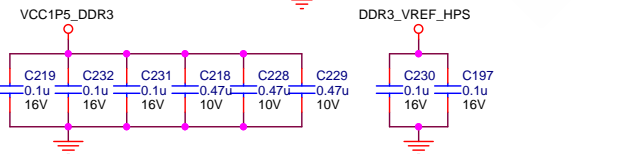
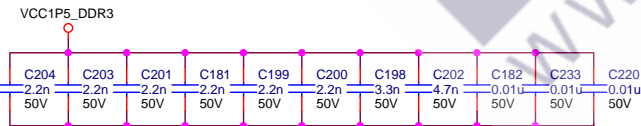
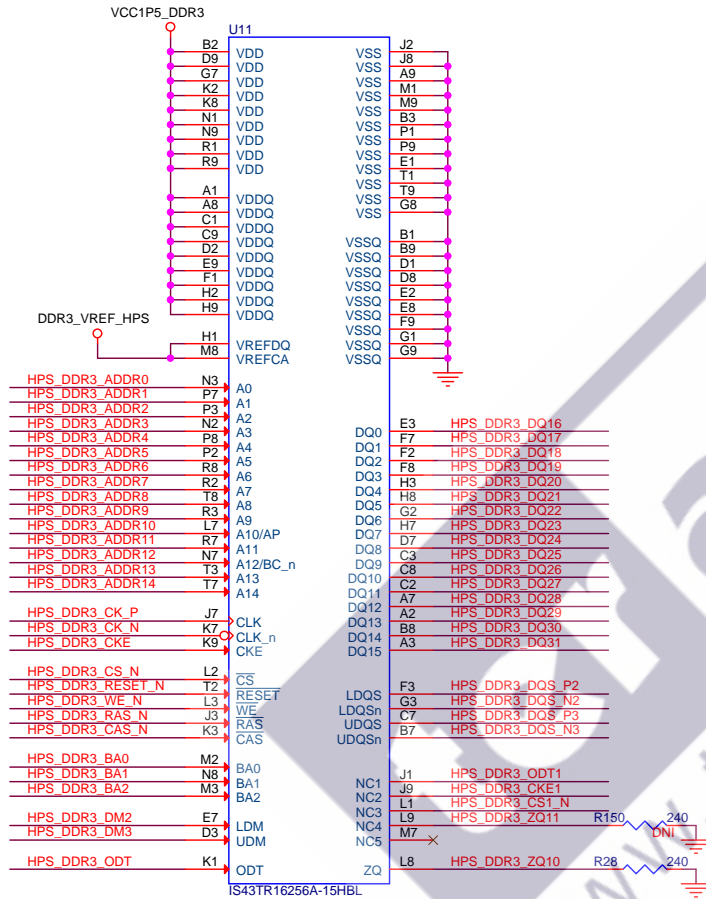
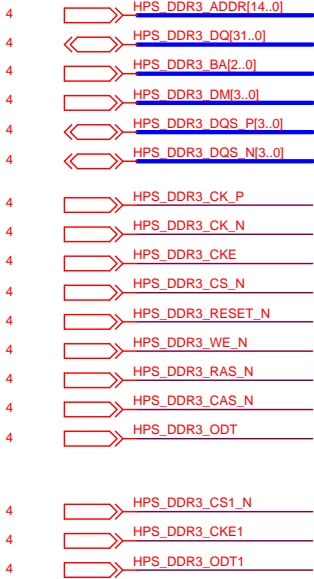
JTAG Chain



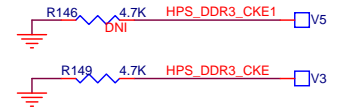
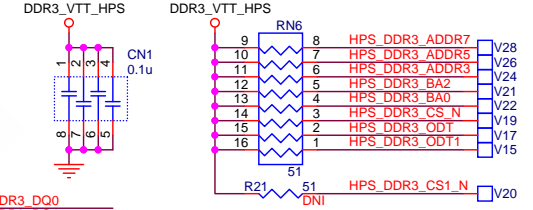
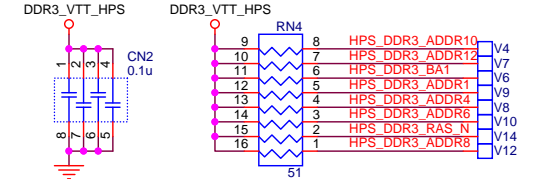
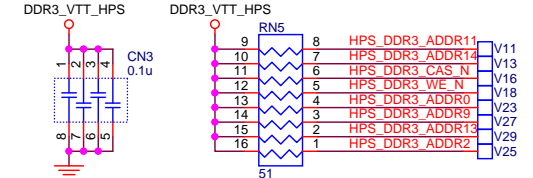
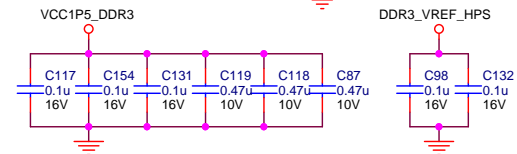
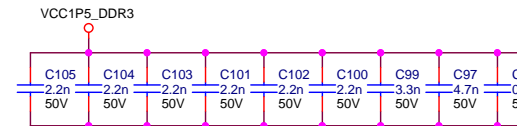
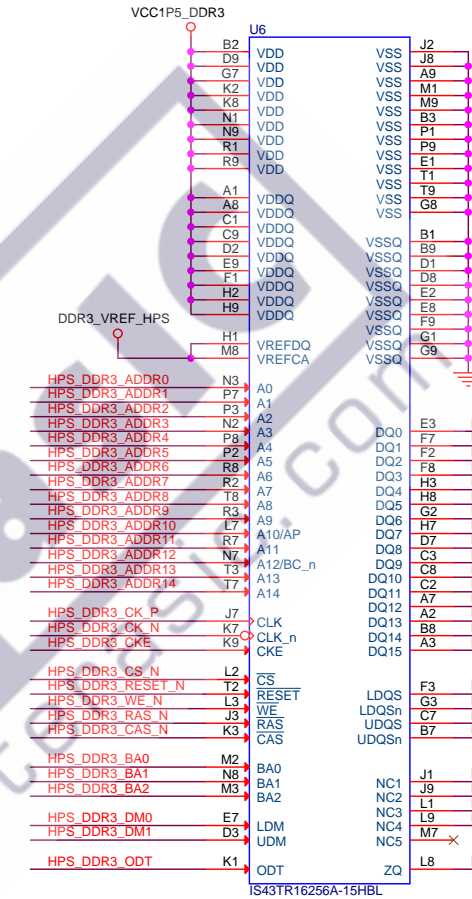
DDR3 Interface (HPS)

Note :
you can only swap the DQ signals
within x8 group (e.g. 0-7,8-15,16-23,24-31)
on the DDR3 chips

Note : you can swap the signals on the OCT resistor array
(include NC pin)



CAD Note:
Place close to DDR3 chip



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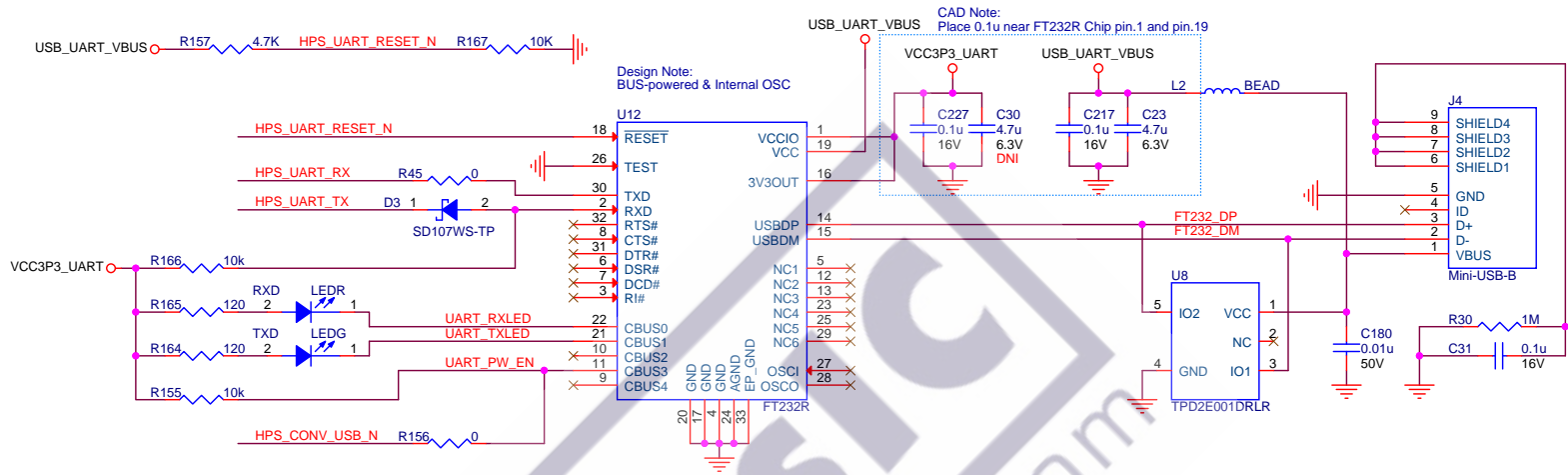
Title: **DE0-Nano-Soc-HDMI Board**

Size: B Document Number: HPS : DDR3 SDRAM Rev: B0

Date: Wednesday, March 23, 2016 Sheet: 12 of 24

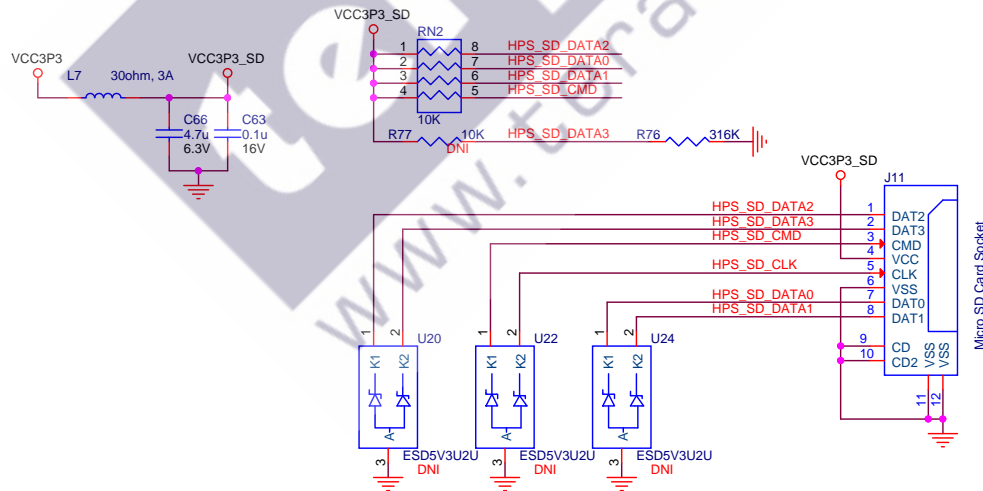
UART Interface

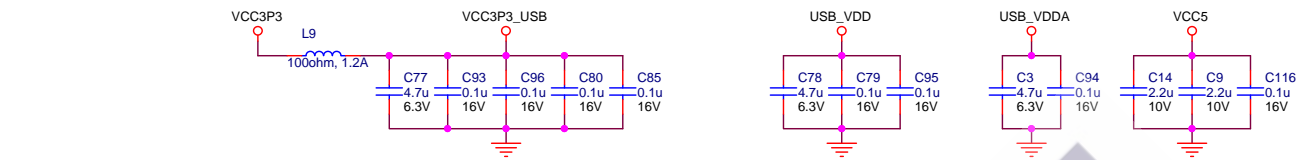
- 5 << HPS_UART_RX
- 5 << HPS_UART_TX
- 5 << HPS_CONV_USB_N
- 17 << HPS_UART_RESET_N



SD Card Interface

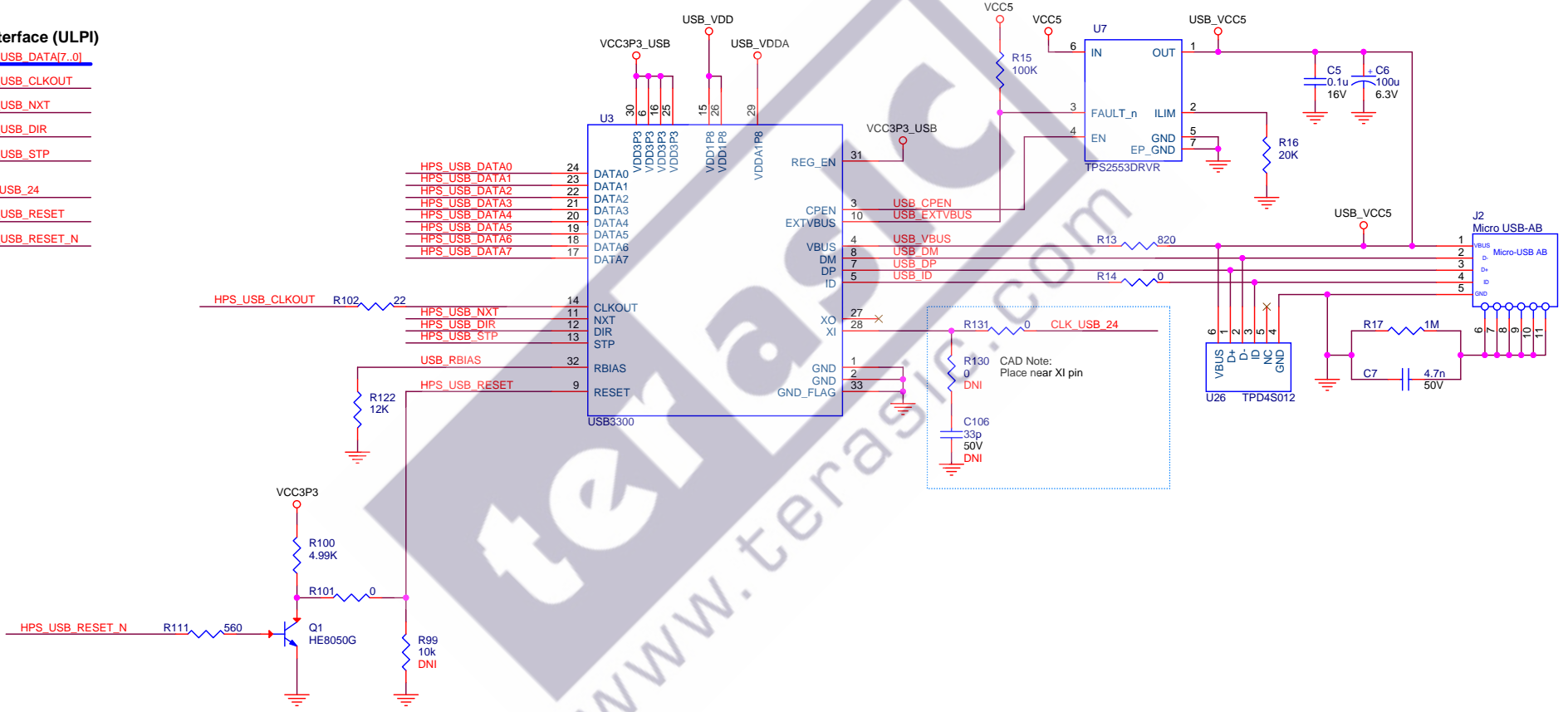
- 5 << HPS_SD_DATA[3..0]
- 5 << HPS_SD_CMD
- 5 << HPS_SD_CLK



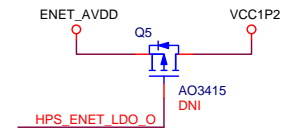
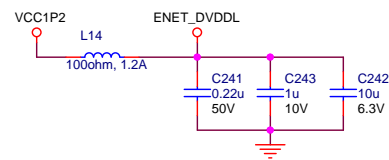
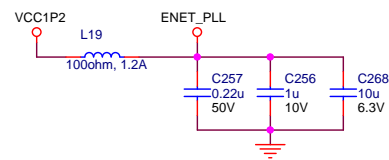
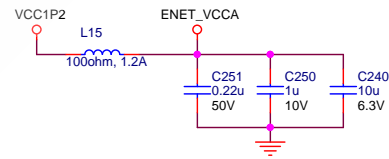
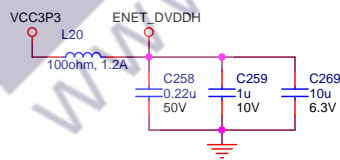
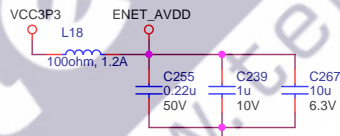
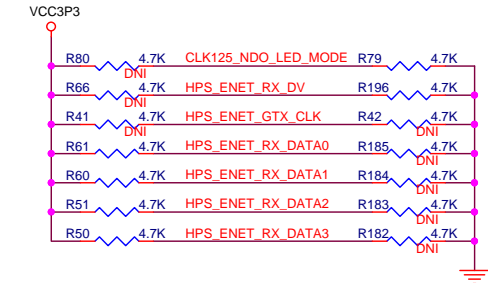
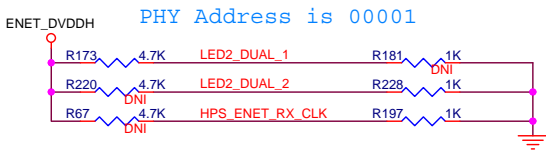
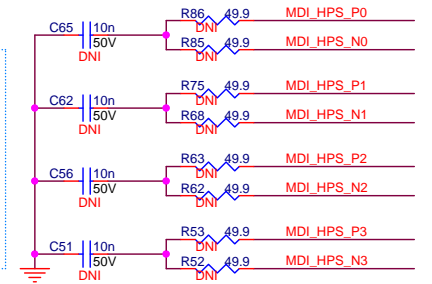
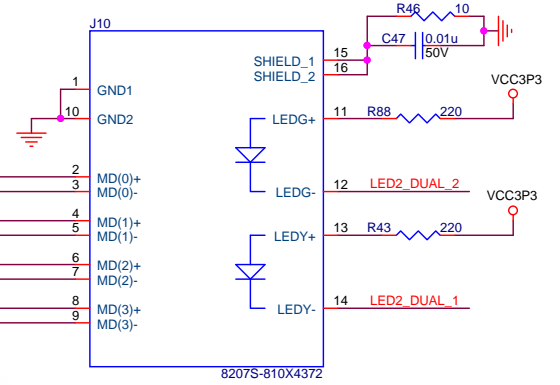
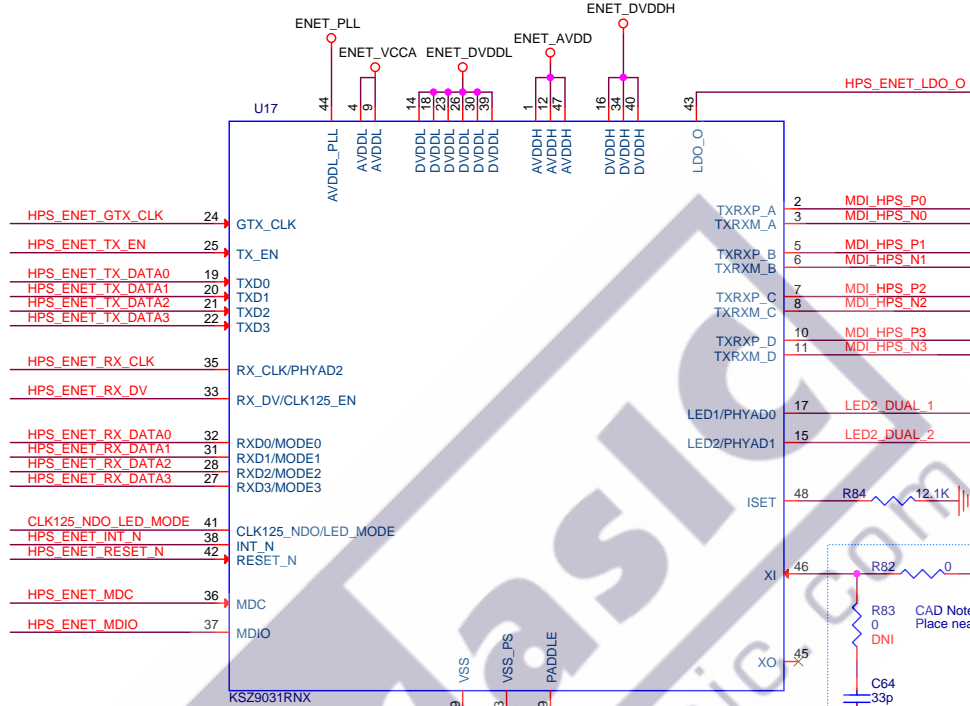
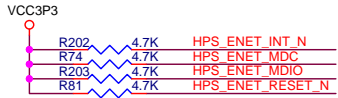
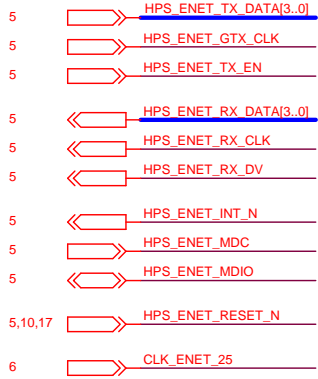


UBS PHY Interface (ULPI)

- 5 << HPS_USB_DATA[7..0]
- 5 << HPS_USB_CLKOUT
- 5 << HPS_USB_NXT
- 5 << HPS_USB_DIR
- 5 << HPS_USB_STP
- 6 << CLK_USB_24
- 5,10 << HPS_USB_RESET
- 17 << HPS_USB_RESET_N



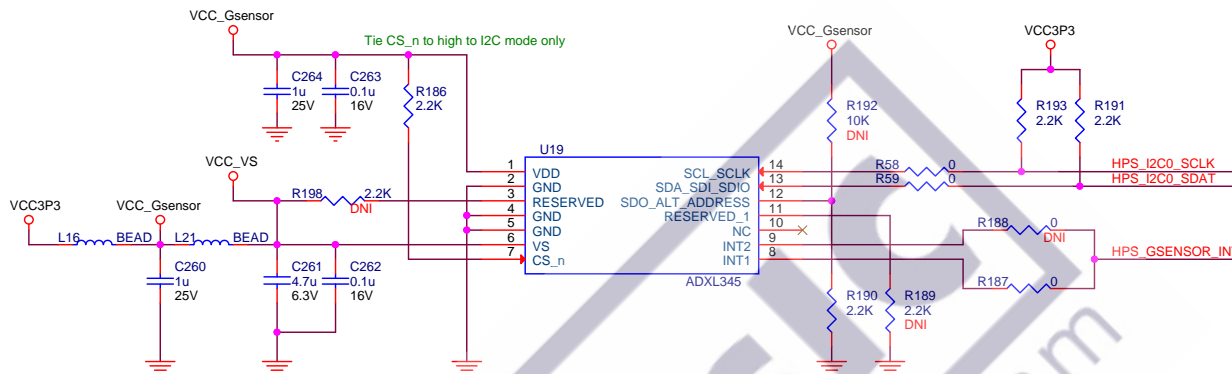
Ethernet PHY Interface (RGMII)



Digital Accelerometer

Accelerometer Interface

- 5 HPS_I2C0_SDAT
- 5 HPS_I2C0_SCLK
- 5 HPS_GSENSOR_INT

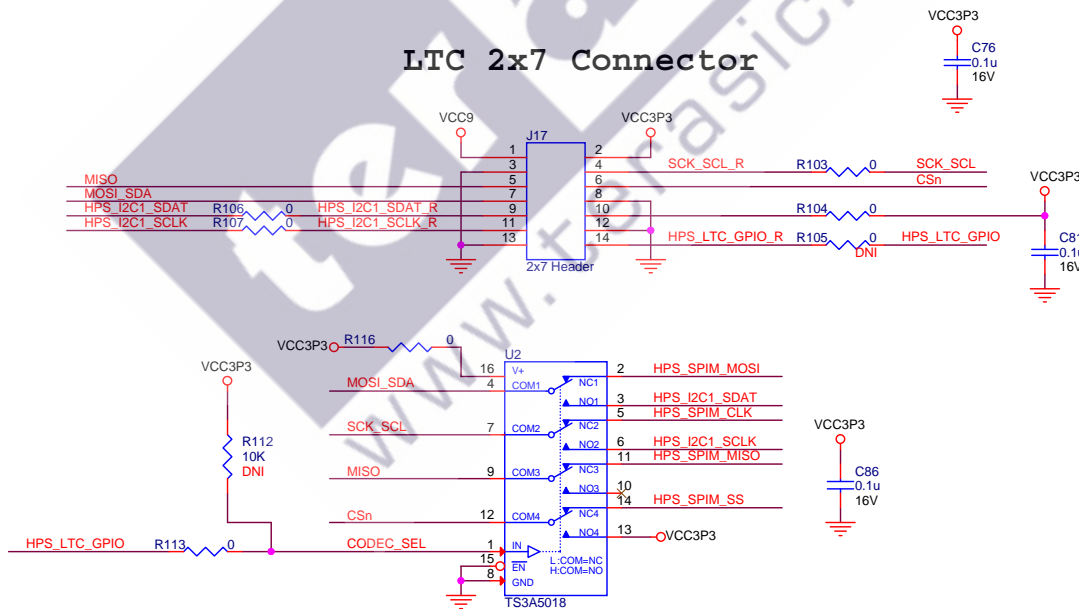


Default : I2C Address 0xA6/0xA7

LTC Interface

- 5 HPS_I2C1_SDAT
- 5 HPS_I2C1_SCLK
- 5 HPS_SPIM_MOSI
- 5 HPS_SPIM_MISO
- 5 HPS_SPIM_CLK
- 5 HPS_SPIM_SS
- 5 HPS_LTC_GPIO

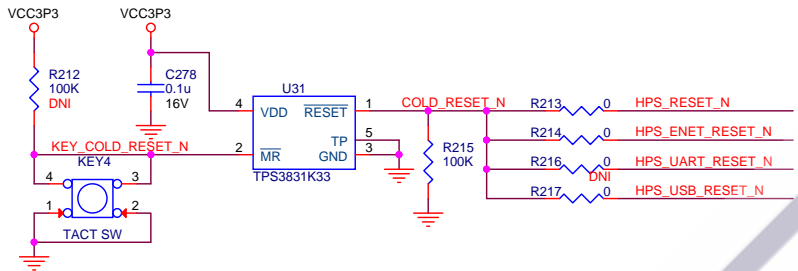
LTC 2x7 Connector



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Title DE0-Nano-Soc-HDMI Board		
Size B	Document Number HPS : Accelerometer, LTC Connector	Rev B0
Date: Wednesday, March 23, 2016	Sheet 16 of 24	

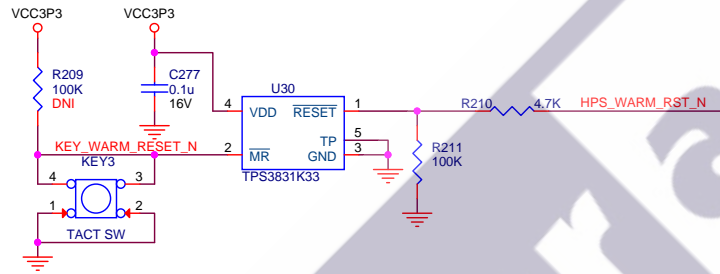
HPS Cold Reset

- HPS Cold Reset**
- 5,10 <<> HPS_RESET_N
 - 5,10,15,17 <<> HPS_ENET_RESET_N
 - 13 <<> HPS_UART_RESET_N
 - 14 <<> HPS_USB_RESET_N
-
- 5,10,14 <<> HPS_USB_RESET
 - 5,10,15,17 <<> HPS_ENET_RESET_N
 - 10 <<> COLD_RESET_N
 - 10 <<> KEY_COLD_RESET_N
 - 10 <<> KEY_WARM_RESET_N



HPS Warm Reset

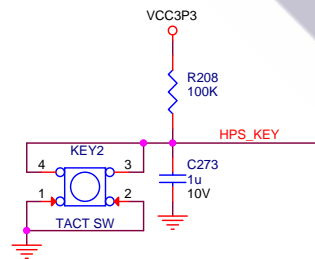
- HPS Warm Reset**
- 5,10 <<> HPS_WARM_RST_N



HPS Key and LED

- 5 <<> HPS_KEY
- 5 <<> HPS_LED

HPS User Button



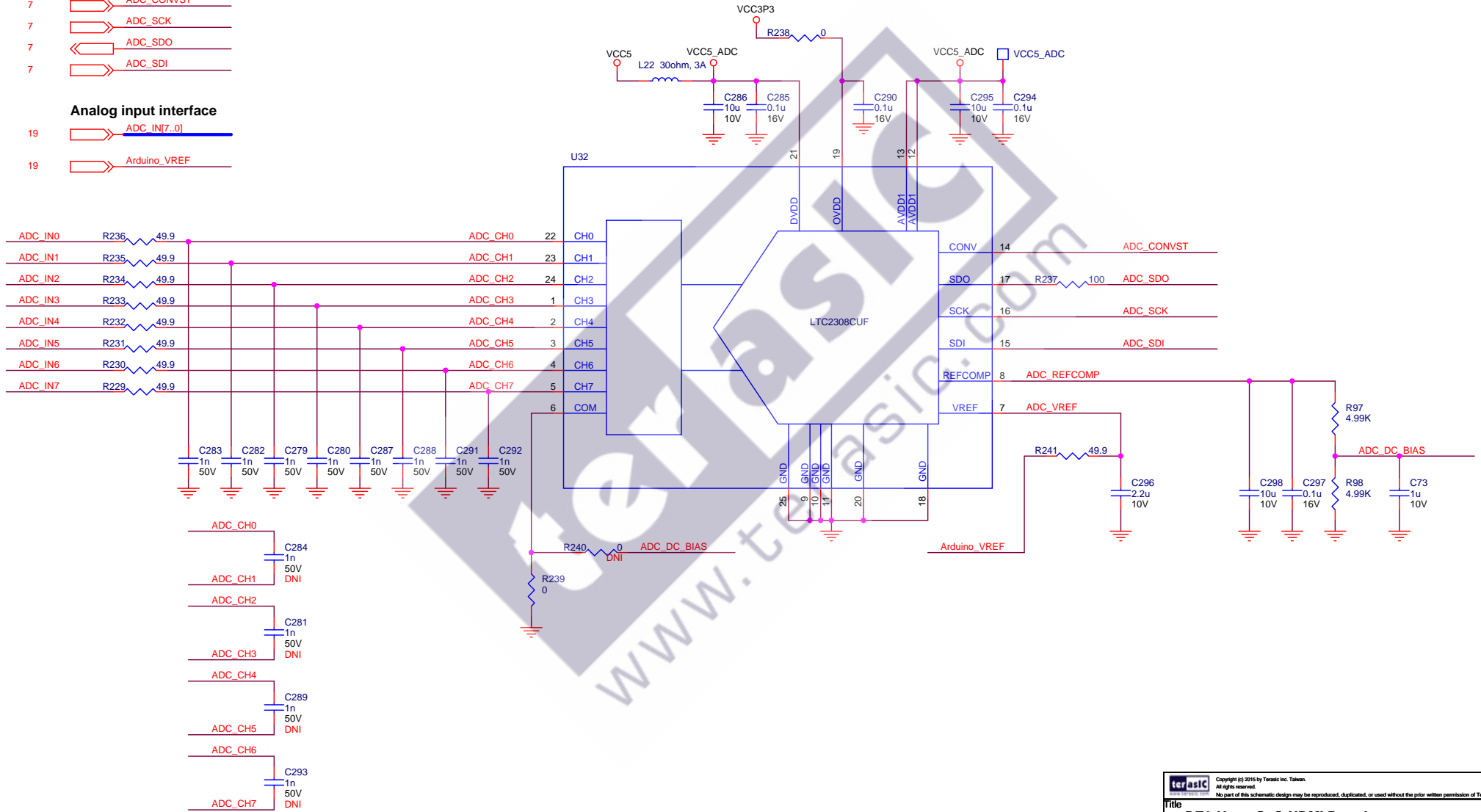
HPS User LED



ADC



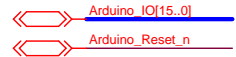
Analog input interface



GPIO



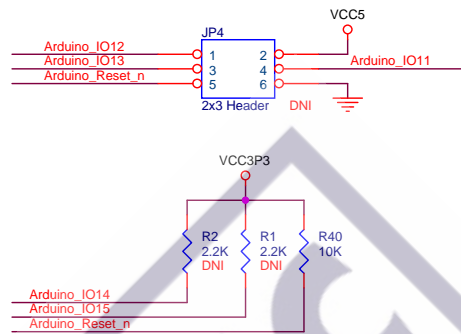
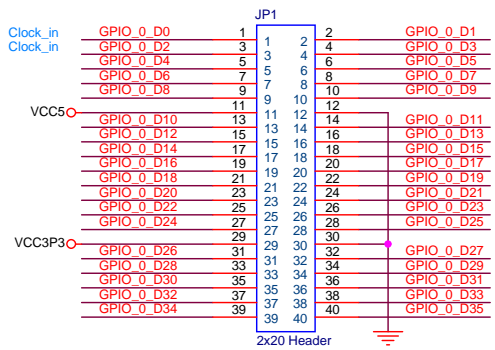
Arduino Digital Interface



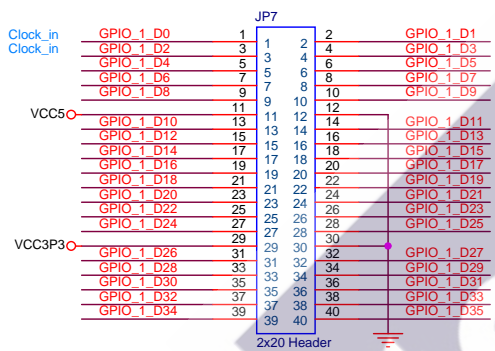
Analog input interface



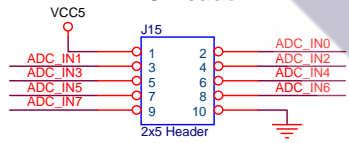
GPIO 0 Header



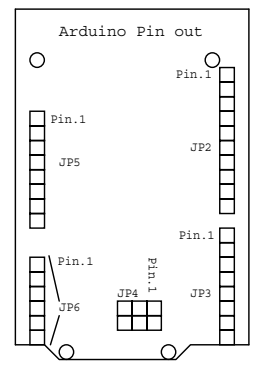
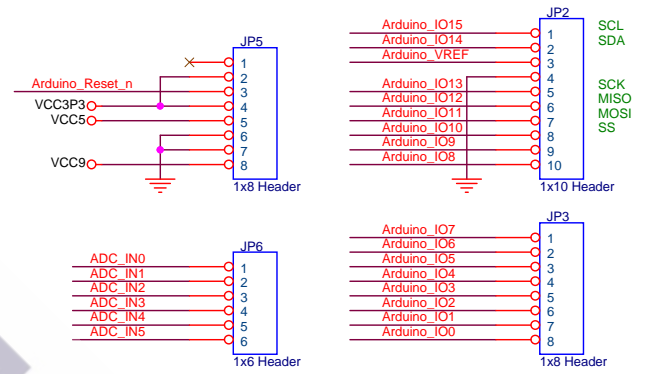
GPIO 1 Header



ADC Header



Arduino UNO Rev3



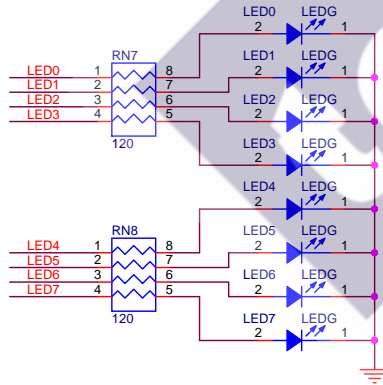
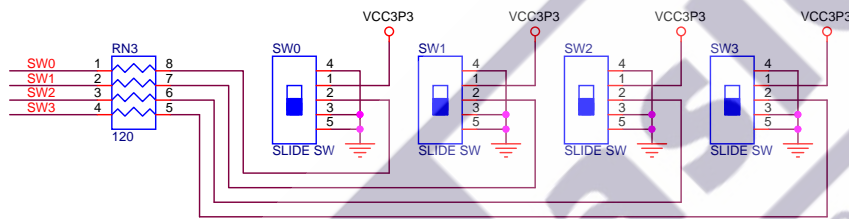
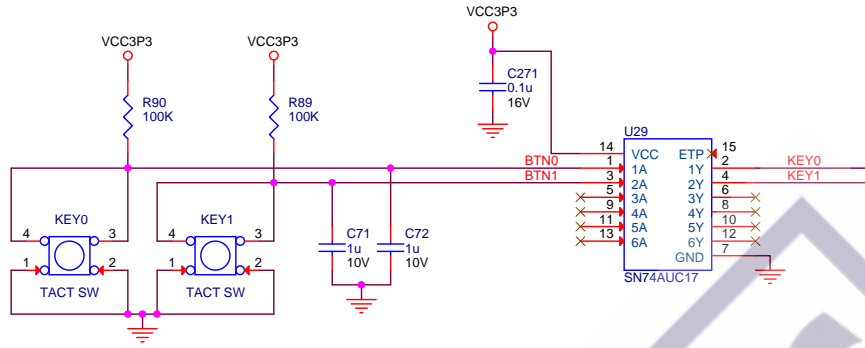
KEY



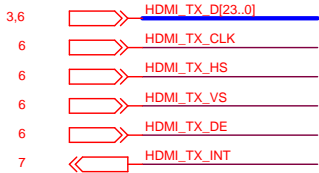
SWITCH



LED



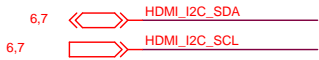
HDMI TX



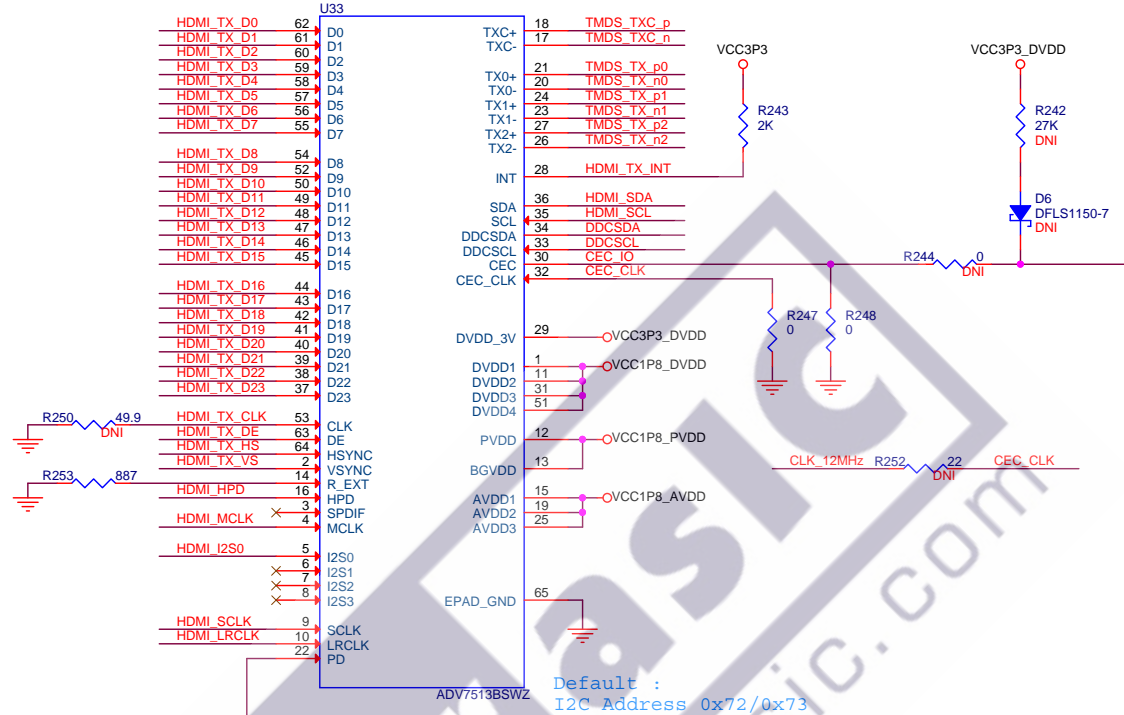
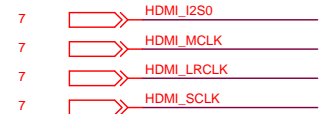
From MAX



I2C Interface

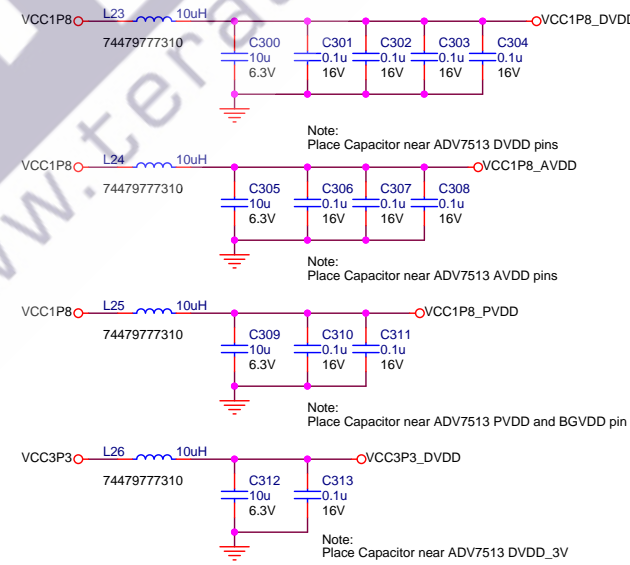
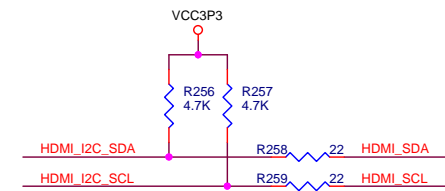
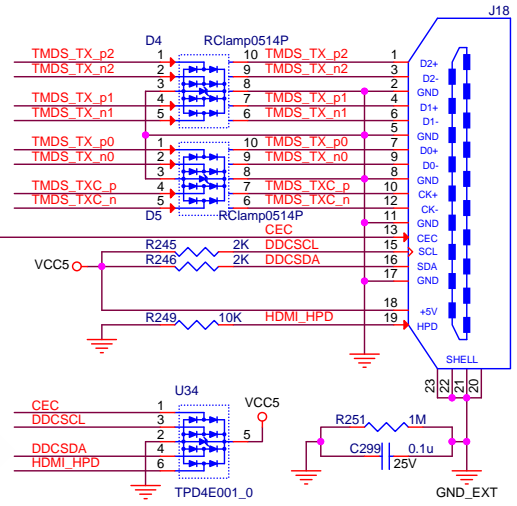


HDMI Audio Interface



Default :
I2C Address 0x72/0x73

HDMI TX



Note: Place Capacitor near ADV7513 DVDD pins

Note: Place Capacitor near ADV7513 AVDD pins

Note: Place Capacitor near ADV7513 PVDD and BGVDD pin

Note: Place Capacitor near ADV7513 DVDD_3V

