Altera Quartus II Software v13.1 — Subscription Edition vs. Web Edition

Categories	Features	Web Edition Software	Subscription Edition Software
General Information	Getting started	Download (www.altera.com/download) and DVD (www.altera.com/dvdrequest)	
	Operating system support	Windows: XP (32/64 bit), 7 (32/64 bit), 8 (64 bit) Windows Server 2008 R2 (64 bit) Linux: Red Hat Enterprise Linux 5 (32/64 bit), Red Hat Enterprise Linux 6(64 bit)	Windows: XP (32/64 bit), 7 (32/64 bit), 8 (64 bit) Windows Server 2008 R2 (64 bit) Linux: Red Hat Enterprise Linux 5 (32/64 bit), Red Hat Enterprise Linux 6 (64 bit)
Device Support	CPLD	MAX® series devices: All (Excluding MAX7000 / 3000)	MAX series devices: All (Excluding MAX7000 / 3000)
	Low-cost FPGA	Cyclone® V FPGAs: All (Excluding 5CEA9, 5CGXC9, and 5CGTD9) Cyclone IV FPGAs: All Cyclone III FPGAs: All	Cyclone V FPGAs: All Cyclone IV FPGAs: All Cyclone III FPGAs: All
	Mid-range FPGA	Arria® V FPGAs: None Arria II FPGAs: EP2AGX45	Arria V FPGAs: All Arria II FPGAs: All
	High-end FPGA	Stratix® series devices: None	Stratix III, IV, and V FPGAs: All
	SoCs	Cyclone V SoCs: All	Cyclone V SoCs: All
Intellectual Property (IP)	Altera and partner IP	Yes, including free OpenCore Plus evaluation feature	
	Full-license IP base suite	IP available for purchase	DSP: FIR / FIR II, FFT, and NCO Compilers Protocols: SerialLite II Memory controllers: DDR, DDR2, and DDR3 for ALTMEMPHY, DDR2, DDR3, and LPDDR2 for UniPHY, RLDRAM II, QDR II, RLDRAM II for UniPHY and QDR II / II+ for UniPHY
Design Entry	Qsys	Yes	
	Schematic entry and language support	Schematic entry, Verilog, VHDL, and System Verilog	
Design Environment	Tcl scripting and command-line support	Yes	
Implementation and Optimization	Incremental compilation and team-based design	No	Yes
	LogicLock™ incremental design capability	No	Yes
	Multiprocessor support	Available with TalkBack enabled	Yes
	Rapid Recompile	No	Yes
	Physical synthesis optimizations	Yes	
	Chip Planner	Yes	
	Live I/O checking	Yes	
	TimeQuest timing analyzer and optimization advisor	Yes	
	Synopsys Design Constraint (SDC) format support	Yes	
	Early power estimator	Available for download on www.altera.com at no cost	
	PowerPlay power analysis and optimization	Yes	
Verification and Debug	SignalTap™ II logic analyzer	Available with TalkBack enabled	Yes
	SignalProbe feature	Available with TalkBack enabled	Yes
	Transceiver Toolkit	No	Yes
	ModelSim®-Altera® Starter Edition	Included	
	ModelSim-Altera Edition	This option is sold for $945	
	Embedded logic analyzer interface	Yes	
	RTL viewer and technology map viewer	Yes	
	Pin planner	Yes	
System Design Software	Nios® II Embedded Design Suite	This software is included in both versions of the Quartus® II software	
	DSP Builder	This option is sold for both versions of Quartus II software	
	Altera SDK for OpenCL™	This option is sold for Subscription Edition only	
Third-Party Support	EDA partners	Altera offers third-party support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification	

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