Ethernet Reference Design
Quick User guide
Example on 40GBASE-KR4

Stratix V GX Signal Integrity Development Board

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Introduction
This reference design demonstrates the operation of Altera 40G base-KR4 Ethernet MAC and PHY IP solution (PDF) on a Stratix V device (5SGTMC7K2F40C2). It is configured to demonstrate on a Signal Integrity Development Kit, Stratix V GT Edition Board using Altera development tool Quartus Prime release 15.1. This design provides a flexible test and demonstration platform which effectively control, test, and monitor 40Gbps Ethernet packets.

This hardware demonstration reference design offers the following features:

- Auto-Negotiation (AN) as defined in Clause 63 (only negotiation to 40GBASE-KR4 mode is supported).
- The 40GBASE-KR4 PMD as defined in Clause 84 which includes Link Training (LT) as defined in Clause 72.
- Forward Error Correction (FEC) as defined in Clause 74.
- System Console based (GUI control and status interface) flexible, reusable, and extendable user control interface allows users to dynamically configure and monitor any configuration registers provided by this demo design.
System Overview and Functional Description

The hardware platform consists of three sub-systems:

- The 40GBase-KR4 MAC and PHY IP
- Packet Client with random packet generator and monitor
- System Console for configuration and control of the system

This system can be represented by the following diagram:

![System Overview Diagram](image-url)

Figure 1 System Overview
40GBASE-KR4 Ethernet MAC and PHY IP

The Altera 40G Ethernet MAC and PHY IP core is implemented in compliance with the IEEE 802.3ba 2010 Higher Speed Ethernet Standard. It is including Auto-Negotiation (AN), Link Training (LT) and Forward Error Correction (FEC). This module handles the frame encapsulation and flow of data between a client logic and Ethernet network via a 40GbE Ethernet PCS and PMA (PHY). In the TX direction, the MAC accepts client frames, inserts inter-packet gap (IPG), preamble, start of frame delimiter (SFD), header, padding, and checksum before passing them to the PHY. The PHY encodes the MAC frame as required for reliable transmission over the media to the remote end. Similarly, in the RX direction, the MAC accepts frames from the PHY, performs checks, updates statistics counters, strips out the CRC, preamble, and SFD, and passes the rest of the frame to the client.

Packet Client with Random Packet Generator and Monitor:

The Packet Client includes a Packet Generator and a Packet Monitor. These modules have 256-bit Avalon-ST interface for the data-path and connect to the 40G Ethernet MAC. There is also a 32-bit Avalon-MM configuration and status interface associated with both the generator and monitor. The generator can generate random packets. Monitor parses all packets received from MAC and checks the integrity of the packets.

Terminal System Controller (sterm.exe):

This reference design provides a windows terminal program sterm.exe which can run on a PC (windows based operating system). User must provide byte addresses in order to access registers on chip using this interface.
**40Gbps Ethernet MAC and PHY IP Overview**

As mentioned in previous sections, the 40G Ethernet sub-system consists of 40G MAC and PHY sub-modules. The MAC client side data path interface has two options: Avalon ST interface and Custom ST interface. This reference design uses an Avalon-ST interface which includes interface adapter. This adapter then provides a standard Avalon-ST interface for the MAC client. The MAC connects to the PHY core over XLGMII interface. The 40G Ethernet IP core can be demonstrated as the following simplified diagram:

![Figure 2 Ethernet MAC and PHY IP](image)

Additional Functional Details of 40GE Ethernet IP Core:

The additional details of the IP core can be found in the User guide. The IP core evaluation package and the user guide can be downloaded from Altera website: [http://www.altera.com/products/ip/iup/ethernet/m-alt-40-100gb-ethernet.html](http://www.altera.com/products/ip/iup/ethernet/m-alt-40-100gb-ethernet.html)
Quick Start Guide
The reference design setup essentially consists of software and hardware.

Software Requirement:
- Quartus Prime 15.1 or above (with system console feature)
- Transceiver Signal Integrity Development Kit – Stratix V GX Edition v12.0.0 or above (with clock control feature) [if the software says current active Quartus version isn’t the correct version then the board is broken, you need to switch to another board.]

Hardware Requirement:
- Stratix V GX SI Development Kit
- 24 inch Backplane (XCEDE 715-9914-000 REV-D)
- Backpanel (XCEDE SI TEST BOARD NELCO 4000-1351 PCB93 REV-P)
- SMA cable*16 (ST18/SMAm/36)
- 120W, 20VDC @6.32A Power Supply
- USB Type B cable (Square)
The relevant setups for each of these components are provided in detail as shown below:

Figure 3  Hardware Setup

The Signal Integrity Stratix V GT development board requires minimum hardware setup. Switch 6 (SW6), all 4 pin need to set to logic 0 (close). See below.

Figure 4  Hardware Switches
**Signal Integrity Stratix V GT Edition Setup**


Program Y3 clock frequency to 644.53125MHz.

![Clock Control](image)

**Figure 5 Clock Control**

**Compile, Build, Load and Run the Software**

1. Open the project file alt_e40_avalon_top_sv_kr4.qpf file in alt_e40_avalon_top_sv_kr4_13_1 directory.
2. Re-compiled the alt_e40_avalon_top_sv_kr4_13_1 project to generate .sof file.
3. Open the SignalTap II Logic Analyzer by double clicking on “Tool” -> “SignalTap II Logic Analyzer”.
4. Download the alt_e40_avalon_top_sv.sof to development board.

Make sure the pins are assigned as compatible pairs. In this design transceiver bank B2L is used for 4 pairs of TX/RX.
Figure 6  Transceiver Bank
Viewing the Result
Connect the cables to the corresponding pinouts. (Note that cables should be in orders of negative and positive) Run the main_run.tcl under system_console folder in system console and go to KR4_Status tab, change KR4 Settings by reading and writing registers.

Figure 7  System Console Interface

Figure 8  KR4 Settings
You need to reset SEQ and write register and uncheck reset SEQ and rewrite register until all registers are as the below picture.

Click on “Read all Register” and you can access the register values.

<table>
<thead>
<tr>
<th>KR4 Status Register</th>
<th>LT TX Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit Name Value</td>
<td>Lane0 Lane1 Lane2 Lane3</td>
</tr>
<tr>
<td>0  SEQ Link Ready Ready</td>
<td>LT VOD setting 0x38 0x28 0x38 0x28</td>
</tr>
<tr>
<td>1  SEQ AN timeout no timeout</td>
<td>LT Post-tap setting 0x12 0x10 0x14 0x12</td>
</tr>
<tr>
<td>2  SEQ LT timeout no timeout</td>
<td>LT Pre-tap setting 0x29 0x9 0x1b 0x19</td>
</tr>
<tr>
<td>13-8 SEQ Reconfig Mode 40G FEC Mode</td>
<td>RKEQ CTELE Setting 0xc 0xc 0xc 0xc</td>
</tr>
<tr>
<td>16  KR4 FEC ability no</td>
<td>RKEQ CTELE Mode 0x0 0x0 0x0 0x0</td>
</tr>
<tr>
<td>17  KR4 FEC err. indability no</td>
<td>RKEQ DFE Mode 0x1 0x1 0x1 0x1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>0xC2 = 0x8130</th>
<th>0xD2 = 0x1010101</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit Name Value</td>
<td>Link Trained Complete</td>
</tr>
<tr>
<td>1  AN page received no</td>
<td>Link Trained Frame lock</td>
</tr>
<tr>
<td>2  AN Complete no</td>
<td>Link Trained Frame lock error</td>
</tr>
<tr>
<td>3  AN ADV Remote Fault no</td>
<td>Link Trained Start-up protocol</td>
</tr>
<tr>
<td>4  AN RXGM idle yes</td>
<td>Link Trained Failure</td>
</tr>
<tr>
<td>5  AN Ability yes</td>
<td>Link Trained Error</td>
</tr>
<tr>
<td>6  AN Status link down</td>
<td>RKEQ Frame lock Loss</td>
</tr>
<tr>
<td>7  LP AN Ability no</td>
<td>CTELE Fine-grained Tuning Error</td>
</tr>
<tr>
<td>8  FEC negotiated yes</td>
<td></td>
</tr>
<tr>
<td>9  AN Failure no failure</td>
<td></td>
</tr>
<tr>
<td>17-12 KR4 An Link Ready 40G Base-KR4</td>
<td></td>
</tr>
</tbody>
</table>

Figure 9 KR4 Status Register

The example capture is a TX to RX loopback test setting.

1. Auto negotiation function must turn off for TX to RX loopback test.
2. Force negotiated to FEC mode.
3. Reset SEQ is the reset of initiate auto negotiate and link training function.

The KR4 status control panel needs to configure first before the device able the do auto negotiation and link training process. Register 0xB0, 0xC0 and 0xD0 need to set as the example above.

Register 0xD0:
- Bit[22:20]: 011 = rx_ctle_mode set to “Fine-gained turning at being of LT”.
- Bit[23] : 1 = Search upper VOD set.
- Bit[26:24]: 010 = Rx_ctle_mode set to “Trigger DFE at end of LT”.
Register 0xC0:
Bit[0] : 0 = Disable the KR4 AN function.

Register 0xB0:
Bit[0] : 1 = Force Negotiate to FEC mode set.

Note: All change will effect only after “Reset SEQ” bit is set.

Note: For normal two device setup, register 0xB0 and 0xC0 don’t need to change. Only register 0xD0 needs to change to 0x82b85111 for long backplane.

**System Monitor Panel**
The system monitor panel contains all the error message and status information. The example of the capture below is one of the error free conditions. The system monitor panel will not refresh automatically. It needs to manually click on the “Update” button to refresh status.

![System Monitor Panel](image)

Figure 10  System Monitor Panel
System Control Panel
There are three major functions in the system control panel, Soft Reset, Serial/parallel loopback, and PRBs testing function. The current test doesn’t need to use those functions. See capture below.

Packet Monitor Panel
This hardware demo design only able to generate randomize size packet. Continually generate packet can be trigger by press “Send Pkt” button. “Stop Pkt” button is stopped the traffic generation.

The packet monitor has TX/RX packet count, Error packet count and TX and RX packet count difference. See example capture below.
Note: For this TX to RX loopback test, checking the TX packet count and RX packet count is one of the methods to confirm the test pass or fail. If all TX counter are equal to RX counter, that means pass. Otherwise it could be a hardware issue. Try to reconnect your cables, replace cables or change pinout. Make sure your positive and negative TXs and RXs are connected correctly.
Possible Issues

In the previous update, one lane of signal didn’t work because one of the hardware pin wasn’t transmitting data. To resolve the problem, check pin assignments and try to use alternative pins in the same transceiver bank. Quartus strictly requires TX/RX to use compatible pins, so user might need to try multiple pairs to find the right pair. Please see the picture below as reference for this specific design.

<table>
<thead>
<tr>
<th>clk ref r</th>
<th>Input</th>
<th>PIN W32</th>
<th>B2L</th>
<th>PIN W32</th>
<th>L5-V PCML</th>
</tr>
</thead>
<tbody>
<tr>
<td>cpu resetn</td>
<td>Input</td>
<td>PIN J31</td>
<td>B6C</td>
<td>B6C N0</td>
<td>PIN J31</td>
</tr>
<tr>
<td>rx serial r[3]</td>
<td>Input</td>
<td>PIN T38</td>
<td>B2L</td>
<td>PIN T38</td>
<td>1.5-V PCML</td>
</tr>
<tr>
<td>rx serial r[2]</td>
<td>Input</td>
<td>PIN U36</td>
<td>B2L</td>
<td>PIN U36</td>
<td>1.5-V PCML</td>
</tr>
<tr>
<td>rx serial r[1]</td>
<td>Input</td>
<td>PIN P38</td>
<td>B2L</td>
<td>PIN P38</td>
<td>1.5-V PCML</td>
</tr>
<tr>
<td>rx serial r[0]</td>
<td>Input</td>
<td>PIN V38</td>
<td>B2L</td>
<td>PIN V38</td>
<td>1.5-V PCML</td>
</tr>
<tr>
<td>tx serial r[3]</td>
<td>Output</td>
<td>PIN R36</td>
<td>B2L</td>
<td>PIN R36</td>
<td>1.5-V PCML</td>
</tr>
<tr>
<td>tx serial r[2]</td>
<td>Output</td>
<td>PIN T34</td>
<td>B2L</td>
<td>PIN T34</td>
<td>1.5-V PCML</td>
</tr>
<tr>
<td>tx serial r[1]</td>
<td>Output</td>
<td>PIN P34</td>
<td>B2L</td>
<td>PIN P34</td>
<td>1.5-V PCML</td>
</tr>
<tr>
<td>tx serial r[0]</td>
<td>Output</td>
<td>PIN V34</td>
<td>B2L</td>
<td>PIN V34</td>
<td>1.5-V PCML</td>
</tr>
<tr>
<td>tx serial r[3]</td>
<td>Output</td>
<td>PIN R37</td>
<td>B2L</td>
<td>PIN R37</td>
<td>1.5-V PCML</td>
</tr>
<tr>
<td>tx serial r[2]</td>
<td>Output</td>
<td>PIN P35</td>
<td>B2L</td>
<td>PIN P35</td>
<td>1.5-V PCML</td>
</tr>
<tr>
<td>tx serial r[1]</td>
<td>Output</td>
<td>PIN V35</td>
<td>B2L</td>
<td>PIN V35</td>
<td>1.5-V PCML</td>
</tr>
<tr>
<td>clk ref r</td>
<td>Input</td>
<td>PIN W33</td>
<td>B2L</td>
<td>PIN W33</td>
<td>1.5-V PCML</td>
</tr>
</tbody>
</table>

Figure 13  Pinout Planner
Reference Documents

Altera 40 and 100Gbps Ethernet MAC and PHY MegaCore Function User Guide


Signal Integrity Development Kit, Stratix V GT Edition Board


Altera Wiki, 40G Base-KR4 Ethernet Hardware Demo