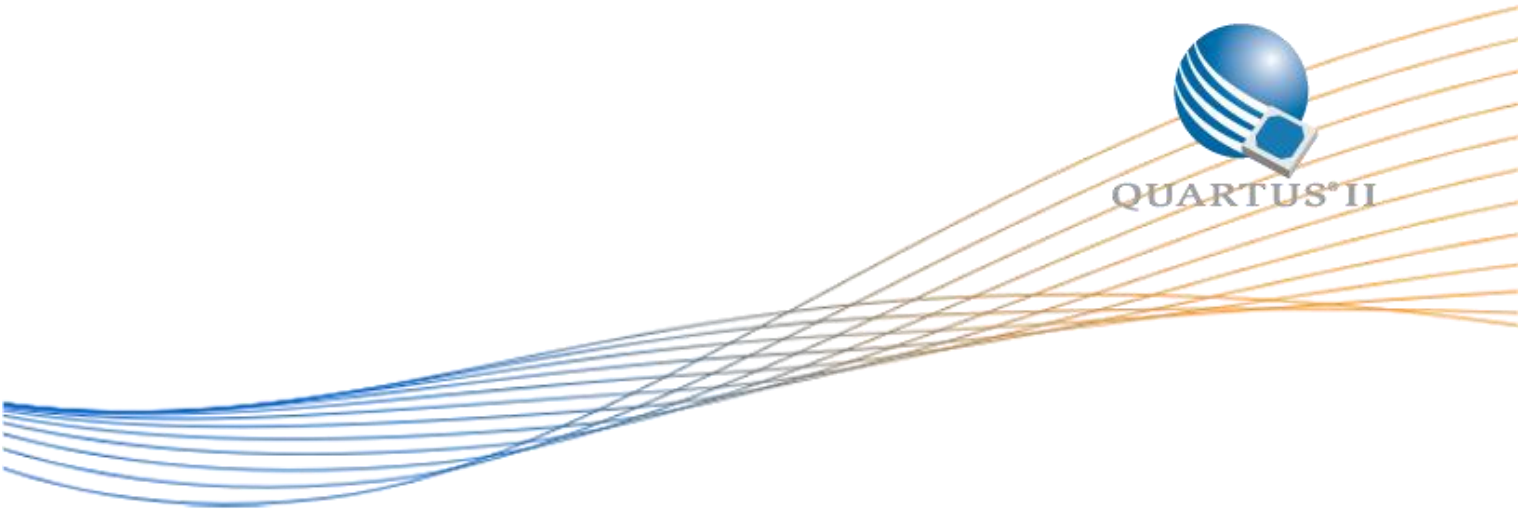


Arria 10 Internal Temperature Sensor Reference Design User Guide

Date: 2016 January 6

Revision: 1.0

Contents

Overview

This reference design is targeted on Arria 10 GX FPGA Develompent Kit. It demonstrates on the usage of Arria 10 internal temperature sensor.

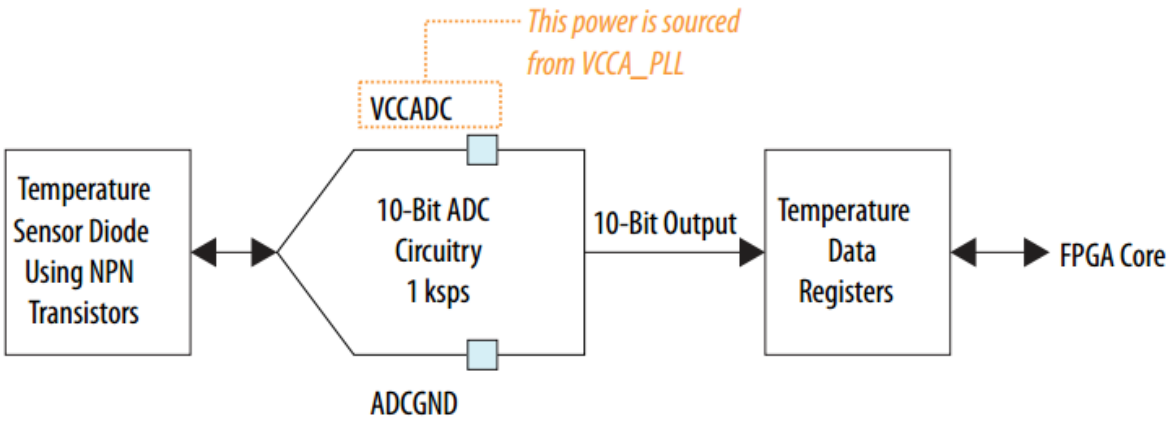
Theory of operation

Arria 10 device contains a temperature sensing diode (TSD) that uses the characteristics of a PN junction diode to determine die temperature. It comes with a built-in 10-bit analog-to-digital converter (ADC) circuitry that allow user to monitor die temperature.

Altera developed an IP, named *Altera Temperature Sensor IP core* to allow user to read the temperature using internal temperature sensing diode. The IP contains 4 signals named *CORECTL, RESET, EOC, and TEMPOUT*. To read the temperature of the die during user mode, assert the *CORECTL* signal from low to high. Active high *RESET* signal is used to reset the register at any time. The ADC circuitry takes 1,024 clock cycles to complete one conversion. The *EOC* signal goes high for one clock cycle indicating completion of the conversion. The FPGA core reads out the data on the *TEMPOUT* signal at the falling edge of the *EOC* signal.

For more information of the Arria 10 temperature sensor diode, user can refer to Chapter 10 (Power Management in Arria 10 Devices) in Arria 10 Core Fabric and General Purpose I/Os handbook and Altera Temperature Sensor IP Core User Guide

Figure 1: Internal TSD Block Diagram



Software requirements

In order to run the reference design in Windows system, the following software is needed:

- Altera Complete Design Suite (ACDS). Refer to the version indicated at the Quartus II version field of this reference design in the Design Store
- Altera Arria 10 GX FPGA Development Kit Installer

Hardware setup

In order to run the reference design, the following hardware is needed:

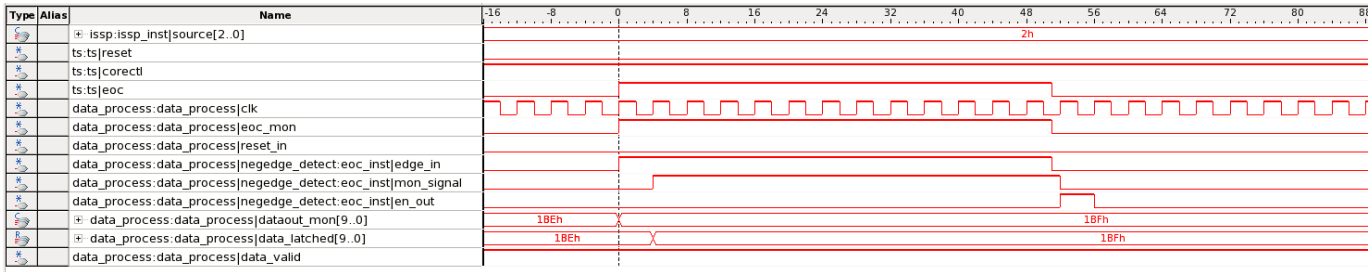
- Arria 10 GX FPGA Development Kit
- USB Blaster

Quick start guide

Follow the following steps to run the reference design:

- Download the reference design in ***.par** format and open the **New Project Wizard** (File menu) in Quartus II software
- Use the **Design Template Installation** dialog box to install the template
- Compile the design by select **Start compilation** (Processing menu). A successful compilation creates a ***.sof** file accordingly
- Program the FPGA with the ***.sof** using USB Blaster
- In the design, user can use the In-System Sources and Probes (ISSP) to control *CORECTL* and *RESET* signal respectively.
- User can monitor the *TEMPOUT* signal using *SignalTap II*
- The figure below demonstrates an example of waveform that is generated by the reference design.

Figure 2: Waveform of internal temperature sensor reference design



Revision History

Date	Version	Changes
2016 January	1.0	Initial release