GPIOs Flash Uart Interfaces Using the MAX 10 FPGA Development Kit
1. **Description**

This design example is used to check out general purpose user I/O components on MAX 10 FPGA development kit, such as LEDs, DIPSW, PB, USB side-bus, PMOD, QSPI Flash, DAC, UART as well as GPIO-attribute ADC interface. Please download the installer of MAX 10 FPGA development kit and use BTS GUI to try it out.

![Max10 FPGA Development Kit](image)

2. **Operation of the Design:**

This design example demonstrates the working of general purpose I/O interfaces, such as LEDs, Push Buttons, DIP Switches and PMOD interfaces. It also allows you to interact with quad SPI flash, UART and DAC components on the Max 10 Development Kit.

The MAX 10 FPGA development kit provides a 512-Mb (megabit) quad SPI flash memory. Altera Generic QUAD SPI controller core is used by default to erase, read, and write quad SPI flash in reference designs of the Board Test System (BTS) installer. If you use the parallel flash loader (PFL) IP to program the quad SPI flash, you need to generate a .pof to configure the device. Please resort to the User Guide for MAX 10 FPGA development kit for more details.

3. **Reconstruct the Design:**

This design example has a system Qsys component which includes all general purpose user I/O components, quad SPI flash core, UART core, USB-side Bus core, dual-configuration core and JTAG-Avalon MM interface. JTAG-Avalon MM interface allows you to access and monitor the design via system-console. Qsys platform here is pretty easy to use and facilitate you to reconstruct the design to meet your design requirements.
4. How to run the GPIO design example on the MAX 10 Development kit

1) Download the bts_config.par from the design store.
2) Use the command "quartus_sh --platform_install -package <directory-path>/bts_config.par" to install the design template
3) Use the command "quartus_sh --platform -name bts_config" to unarchive the project and get all the design files.
4) Recompile the design or directly use SOF image at master_image folder
5) Power off the kit and install loopback installers for both ADC related IOs and PMOD interfaces
6) Power on the kit and configure SOF to MAX 10 FPGA
7) Double click “BoardTestSystem” at “\examples\board_test_system\” to open BTS GUI to test this design.
Detected tbs_config. sof on FPGA.
Acknowledgment
This design is based on general purpose user I/O components for MAX 10 FPGA Development Kit produced by Altera Corporation.

Document Revision History

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<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
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<tbody>
<tr>
<td>May 2015</td>
<td>V1.0</td>
<td>Initial Release</td>
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