



QUARTUS<sup>II</sup>

## DDR3 Using the MAX 10 FPGA Development Kit

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## 1. Description

The MAX 10 FPGA development kit has one 64-Mx16 1Gb DDR3 SDRAM and one 128-Mx8 1Gb DDR3 SDRAM. The MAX 10 FPGA provides full-speed support to a DDR3 300-MHz interface with error correction code (ECC) feature. This design example is used to check out a x24 DDR3 300MHz interface, please download the installer of MAX 10 development kit and use BTS GUI to try it out for a straightforward experience.

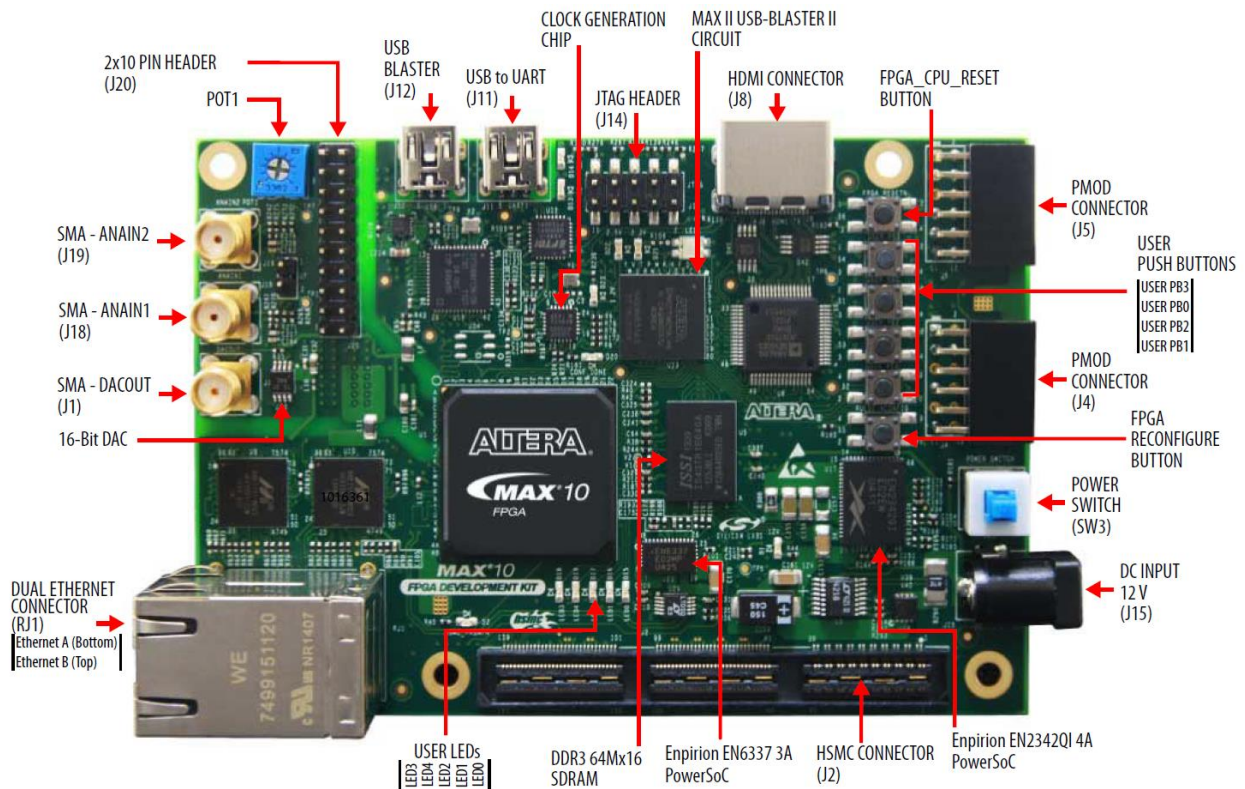


Fig: Max10 FPGA Development Kit

## 2. Operation of the Design:

This design example demonstrates the working of DDR3 interface by reading and writing to a selected amount of addresses.

Please note some address pins for DDR3 interface have been changed from Rev B to Rev C to fix pin assignment violation issue with v15.0 or later version. In addition, DDR3 dedicated reference clock is only working on Rev C kit. Please turn to the User Guide [https://www.altera.com/content/dam/altera-www/global/en\\_US/pdfs/literature/ug/ug-max10m50-fpga-dev-kit.pdf](https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/ug/ug-max10m50-fpga-dev-kit.pdf) for more details about DDR3 interface.

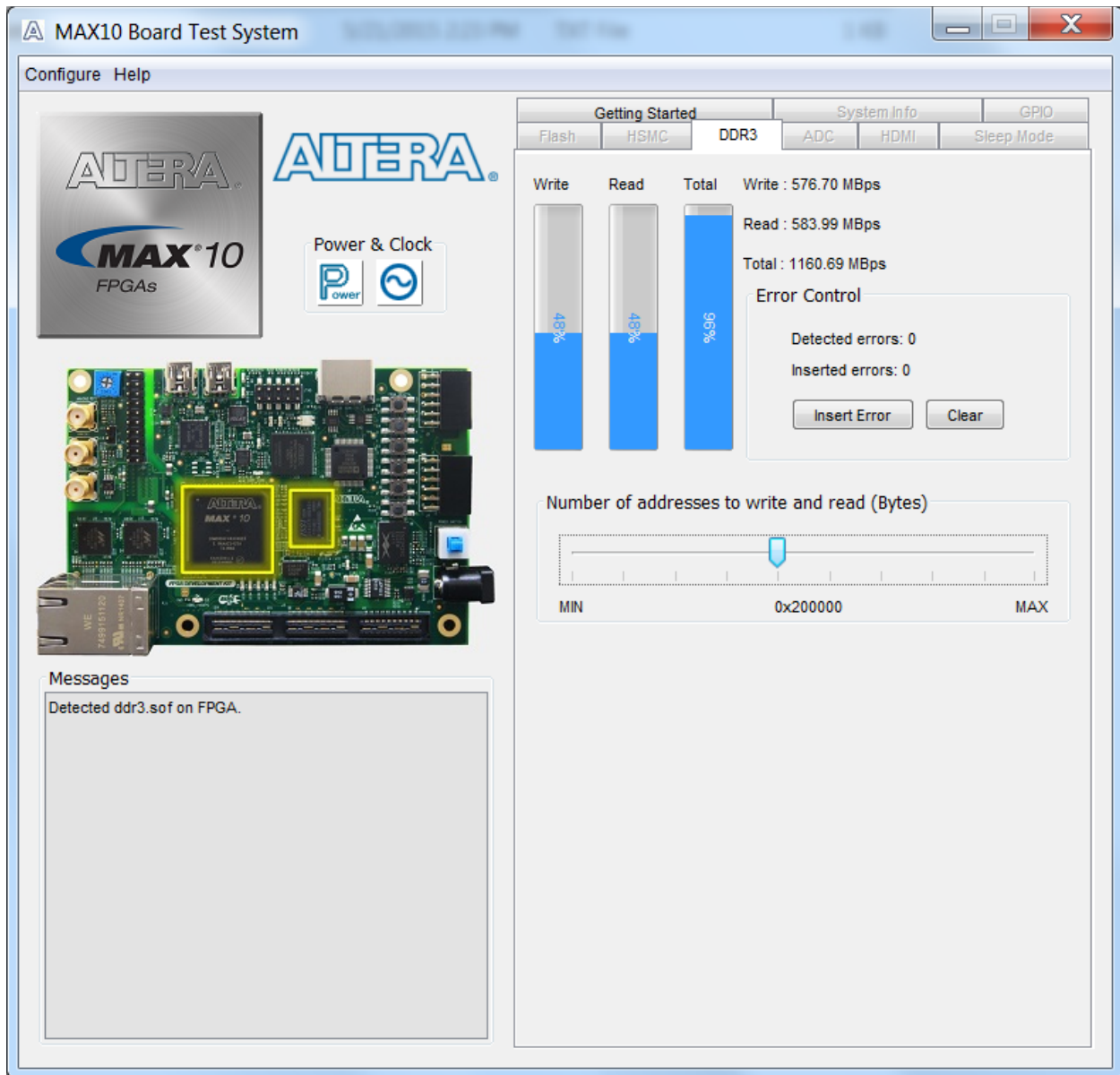
## 3. Reconstruct the Design:

This design example has a system Qsys component which includes DDR3 core, user-defined memory drive test component and JTAG-Avalon MM interface. It allows you to kick off the traffic test and monitor its status over memory components via system-console.

Use	Connections	Name	Description	Export	Clock	Base
<input checked="" type="checkbox"/>		<b>sys_clk</b>	Clock Source			
		clk_in	Clock Input	sys_clk		
		clk_in_reset	Reset Input	reset	exported	
		clk	Clock Output			
		clk_reset	Reset Output	Double-click to export	sys_clk	
				Double-click to export		
<input checked="" type="checkbox"/>		<b>master_0</b>	JTAG to Avalon Master Bridge			
		clk	Clock Input	Double-click to export	sys_clk	
		clk_reset	Reset Input	Double-click to export		
		master	Avalon Memory Mapped Master	Double-click to export	[clk]	
		master_reset	Reset Output	Double-click to export		
				Double-click to export		
<input checked="" type="checkbox"/>		<b>product_info_0</b>	product_info			
		clock_reset	Clock Input	Double-click to export	sys_clk	
		clock_reset_reset	Reset Input	Double-click to export	[clock_reset]	
		avalon_slave_0	Avalon Memory Mapped Slave	Double-click to export		# 0x0000_0000
<input checked="" type="checkbox"/>		<b>msgdma_0</b>	msgDMA			
		cal_fail_mon	Conduit	msgdma_0_cal_fail_mon		
		cal_success_mon	Conduit	msgdma_0_cal_success_mon		
		clk	Clock Input	Double-click to export	mem_if_ddr3_emif_0_af1_clk	
		clk_0	Clock Input	Double-click to export	sys_clk	
		dispatcher_read_csr_irq	Interrupt Sender	Double-click to export	[clk]	
		dispatcher_write_csr_irq	Interrupt Sender	Double-click to export	[clk]	
		dma_read_master	Avalon Memory Mapped Master	Double-click to export	[clk]	
		dma_write_master	Avalon Memory Mapped Master	Double-click to export	[clk]	
		reset_source	Reset Output	Double-click to export	[clk]	
		mrm_bridge_slv	Avalon Memory Mapped Slave	Double-click to export		# 0x0020_0000
		reset	Reset Input	Double-click to export		
		reset_0	Reset Input	Double-click to export		
		status_mon_0_init_done_mon	Conduit	msgdma_0_status_mon_0_init_done_mon		
		status_mon_in	Conduit	Double-click to export		
<input checked="" type="checkbox"/>		<b>master_driver_msgdma_0</b>	master_driver_msgdma			
		reset	Reset Output	Double-click to export	[clock]	
		clock	Conduit [conduit_end 15.0]	Double-click to export	sys_clk	
		csr	Interrupt Receiver	Double-click to export	[clock]	# 0x0010_0000
		interrupt_receiver	Interrupt Receiver	Double-click to export	[clock]	
		avalon_master	Avalon Memory Mapped Master	Double-click to export	[clock]	
		reset_source	Reset Output	Double-click to export	[clock]	
		conduit_end	Conduit	master_driver_msgdma_0_conduit_end	[clock]	
<input checked="" type="checkbox"/>		<b>refclk_clock_bridge</b>	Clock Bridge			
		in_clk	Clock Input	refclk_clock_bridge_in_clk	exported	
		out_clk	Clock Output	Double-click to export	refclk_clock_bridge_out_clk	
<input checked="" type="checkbox"/>		<b>mem_if_ddr3_emif_0</b>	DDR3 SDRAM Controller with UniPHY			
		pll_ref_clk	Clock Input	Double-click to export		
		global_reset	Reset Input	Double-click to export		
		soft_reset	Reset Input	Double-click to export		
		af1_clk	Clock Output	Double-click to export		
		af1_half_clk	Clock Output	Double-click to export	mem_if_ddr3_emif_0_af1_clk	
		af1_reset	Reset Output	Double-click to export	[clock]	
		af1_reset_export	Reset Output	Double-click to export	mem_if_ddr3_emif_0_af1_half_clk	
		memory	Conduit	Double-click to export		
		av1	Avalon Memory Mapped Slave	Double-click to export	mem_if_ddr3_emif_0_af1_clk	# 0x0000_0000
		status	Conduit	Double-click to export		
		pll_sharing	Conduit	Double-click to export		
		csr	Avalon Memory Mapped Slave	Double-click to export	mem_if_ddr3_emif_0_af1_clk	#

#### 4. How to run the DDR3 design example on the MAX 10 Development kit

- 1) Download the ddr3.par from the design store.
- 2) Use the command **quartus\_sh --platform\_install -package <directory-path>/ddr3.par** to install the design template
- 3) Use the command **quartus\_sh --platform -name ddr3** to unarchive the project and get all the design files.
- 4) Recompile the design or directly use SOF image at master\_image folder
- 5) Power on the kit and configure SOF to MAX 10 FPGA
- 6) Double click "BoardTestSystem" at \*\\examples\\board\_test\_system\\ to open BTS GUI to test this design.



### Acknowledgment

This design is based on DDR3 components for MAX 10 FPGA Development Kit produced by Altera Corporation.

### Document Revision History

Date	Version	Changes
May 2015	V1.0	Initial Release