

# Intel® Stratix® 10 TX PAM4 8 x 51Gbps with QSFPDD 1x1 Example Design 18.1 User Guide

Date: 6/10/2019

Revision: 1.0

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## Introduction

The objective of this this design example is to demonstrate Intel<sup>®</sup> Stratix<sup>®</sup> 10 TX PAM4 8x51Gbps channels interfacing with QSFPDD 1x1 module. QSFPDD 1x1 loopback module is used to perform loopback from the transmitters back to the receivers. Transceiver toolkit is used to demonstrate the link BER testing as well as for links status monitoring. In-System Sources and Probes (ISSP) is used to provide reset control to the transceivers.

The reference design requires the following hardware and software to run the test:

- Intel<sup>®</sup> Quartus<sup>®</sup> Prime Pro Edition 18.1
- Intel<sup>®</sup> Stratix<sup>®</sup> 10 TX Signal Integrity Development Kit <u>https://www.intel.com/content/www/us/en/programmable/products/boards\_and\_kits/dev-kits/altera/kits-s10-tx-si.html</u>
- One QSFP-DD Electrical Passive Loopback Module ML4062
  <u>https://multilaneinc.com/product/ml4062/</u>



Figure 1. Intel<sup>®</sup> Stratix<sup>®</sup> 10 TX Signal Integrity Development Kit

## **Theory of Operation**



Figure 2. Block diagram of modules in the reference design

Figure 2 shows the high-level modules in the example design as well as the interfaces among the modules. The Intel<sup>®</sup> Stratix<sup>®</sup> 10 TX E-Tile Transceiver Native PHY is used to configure and implement the hard transceiver channels. ISSP allows real time user control on the resets for the transceivers. The Transceiver Toolkit is used to allow real time control on the transceiver channels, status monitoring and BER link testing. During BER test, Transceiver Toolkit will interface with the internal data generator and checker to generate PRBS pattern as well as to check for bit error.

In this design, there are 8 PAM4 channels configured to run at 51Gbps. The data from transmitter is loopback to receiver using QSFPDD 1x1 loopback module. We will use Transceiver Toolkit to simultaneously monitor and control all the 8 channels.

For further details on E-Tile transceiver architecture, you may refer to the E-Tile Transceiver PHY User Guide -> "E-Tile Transceiver PHY Architecture" section.

For further details on E-Tile transceiver data generator and verifier, you may refer to the E-Tile Transceiver PHY User Guide -> "Data Pattern Generation" and "Data Pattern Verifier" sections.

## How to Setup the Hardware for Link Test

Follow these steps to setup the hardware to run the reference design:

- Connect the QSFPDD loopback module to the QSFPDD 1x1 optical transceiver cage on the Intel<sup>®</sup> Stratix<sup>®</sup> 10 TX Signal Integrity Development Kit as in Figure 3
- 2. Use the default switching settings of the development kit
- 3. Connect the USB cable to the USB Blaster connector on the development kit
- 4. Connect the power adapter shipped with the development board to power supply jack
- 5. Turn On the power for the development kit. The hardware system is now ready for programming



Figure 3. QSFPDD 1x1 optical transceiver cage

#### How to Reconstruct and Running the Reference Design

Follow these steps to reconstruct, compile and run the design:

- 1. Follow the instruction in the Design Store to prepare the design template and load the design into Intel<sup>®</sup> Quartus<sup>®</sup> Prime Pro Edition Version 18.1
- 2. Perform full compilation with the design
- 3. Program the SOF file generated into the development kit
- After the programming is completed, open the Tools -> System Debugging Tools -> Transceiver Toolkit and establish connection to the Intel<sup>®</sup> Stratix<sup>®</sup> 10 TX device as shown in Figure 4.
- 5. You should observe ten channels auto-populated in Transceiver Toolkit. We will focus on the 8 PAM4 channels which are logical channel 2 to 9 as highlighted in the figure. Logical channel 0 and 1 are for SMA interface which are not discussed in this user guide
- 6. Go to the Receiver Channels tab. By default, you should see the status = Running for all channels. Select all channels and Right click -> Stop the receivers as shown in the Figure 5

- Go to the Transceiver Links tab. Select the 8 PAM4 channels -> right click -> Test Pattern. Then select your target Test Pattern. In this example, PRBS31 pattern is selected as shown in Figure 6
- 8. To start the BER link test, select the 8 PAM4 channels -> right click -> Start -> Start Transceiver Link as shown in Figure 7
- 9. After the link test starts, you may observe some channels with initial BER. Reset the checkers by selecting the 8 PAM4 channels -> right click -> Reset -> Reset Checker as shown in Figure 8.
- 10. After resetting, you can observe the number of bits tested and BER as shown in the Figure 9. The Status = Running and Green also indicates that the CDR has successfully locked-to-data
- 11. You may also perform real-time enabling on the loopback mode, changing VOD and preemphasis parameters from Transceiver Toolkit to facilitate link test by selecting a channel and right click as shown in the Figure 10

System Explorer 💠 🗕 🗗 🗖	Т	oolkits 💠 Welcome to the	e Transceiver Toolkit 🛛 🛛 🕇	ransceiver To	oolkit 🛛				- d' 🗆
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		xcvr_native_s10_etile_0 0	Stopped	PRBS7		0	0/0/0/0		
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		xcvr_native_s10_etile_0 2	Stopped	PRBS7		0	0/0/0/0	$\checkmark$	
		xcvr_native_s10_etile_0 3	Stopped	PRBS7		0	0/0/0/0	$\checkmark$	
		xcvr_native_s10_etile_0 4	Stopped	PRBS7		0	0/0/0/0	$\checkmark$	
		xcvr_native_s10_etile_0 5	Stopped	PRBS7		0	0/0/0/0	$\checkmark$	
		xcvr_native_s10_etile_0 6	Stopped	PRBS7		0	0/0/0/0	$\checkmark$	
		xcvr_native_s10_etile_0 7	Stopped	PRBS7		0	0/0/0/0	$\checkmark$	
		xcvr_native_s10_etile_0 8	Stopped	PRBS7		0	0/0/0/0	$\checkmark$	
		xcvr_native_s10_etile_0/9	Stopped	PRBS7		0	0/0/0/0	$\checkmark$	
		Control Transmitter Chann	nel						
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The script doesn't exist: C:\Use	Executing startup script C:\intelfpga_pro\18.1\quartus\sopc_builder\system_console\scripts\syste  The script doesn't exist: C:\Users\cheepinc\system_console\system_console_rc.tcl. You can custo								~

Figure 4. Opening Transceiver Toolkit and establishing connection to device

Toolkits 🛛 Welcome to the Transceive	r Toolkit 🛛 🛛 Transceiv	ver Toolkit 🛛 🖾				
Transmitter Channels Receiver Channels	5 Transceiver Links					
Show in table: Current MinM	lax Best					
Receiver Álias Status	Bits tested	BER		Test pattern	Loopback mode	Adapta
tive_s10_etile_0 0 Running	0	0		PRBS7	Off	Stop
tive_s10_etile_0 1 Running	0	0		PRBS7	Off	Stop
tive_s10_etile_0 2 Running	0			PRBS7	Off	Stop
tive_s10_etile_0 3 Running	0	0		PRBS7	Off	Stop
tive_s10_etile_0 4 Running	0	0		PRBS7	Off	Stop
tive_s10_etile_0 5 Running	0	0		PRBS7	Off	Stop
tive_s10_etile_0 6_Running	0	0		PRBS7	Off	Stop
tive_s10_etile_0]/ Running	U	0		PRBS7	Off	Stop
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	Test Pattern		>			
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	CHECKEI MOUC					
	Loopback Mode		>			
	Adaptation mode (L	Tile/H-Tile)	>			
	Adaptation mode (E	-Tile)	>			
	Start		>			
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	Deest					
Control Receiver Channel	Keset		<u>_</u>	Receiver Auto S	Sweep & Eye Viewer	
	Refresh					
✓	Status Polling					
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Figure 5. S	Stopping 1	the receivers
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Transmitter Channels Receiv	er Channels Tran	sceiver Links				
Show in table: Current	MinMax	Best				
Link Alias Status	Bits tested	BER	Tes	st pattern	Loopback mode	Adaptation
s10_etile_0 0 Stopped	0	0	PRB	S7	Off	Stop
s10_etile_0 1 Stopped	0	0	PRB	S7	Off	Stop
s10_etile_0 2 Stopped	0	0	PRB	S7	Off	Stop
s10_etile_0 3 Stopped	0	0	PRB	S7	Off	Stop
SIU_etile_0[4 Stopped	0	0	PKB	5/ c7	Off	Stop
s10_etile_015_Stopped	0	0	PKB	57 C7	Off	Stop
s10_etile_017 Stopper	Copy		>	57	Off	Stop
s10 etile 0 8 Stopped	Deate			S7	Off	Stop
s10_etile_0 9 Stoppec	Paste			S7	Off	Stop
	Test Pattern		>	USER		
	Generator/che	ecker Mode	>	PRRS7	,	
				11057		
	Loopback Mo	de	>	PRBS9		
	V			PRBS1	1	
	VOD		2	PRBS1	3	
	Pre-emphasis		>	DDDC1	- -	
	· · ·			PKBST	5	
	Adaptation m	ode (L-Tile/H-	Tile) 👌	PRBS2	3	
	Adaptation m	ode (E-Tile)	×	PRBS3	1	
	Start		>			
Control Transceiver Lin	Start			Link	Auto Sween & Ev	Viewer
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	Reset		>			
	Refresh			cl Console	8	
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ns	Export		>	va soqiro	rearing ICI 80	urce comman

Figure 6. Selecting the target test pattern

Show in table:	urrent	MinMax	Best					
Link Alias Sta	tus	Bits tested	BER	Test pattern	Loopbac	k mode	Adaptation m	V <sub>OD</sub>
s10_etile_0 0 Sto	oped	0	0	PRBS7	Off		Stop	0
s10_etile_0 1 Sto	oped	0	0	PRBS7	Off		Stop	0
s10_etile_0 2 Sto	oped	0	0	PRBS31	Off		Stop	0
s10_etile_0 3 Sto	oped	0	Comm		<u> </u>		Stop	0
s10_etile_0 4 Sto	oped	0	Сору		· · · ·		Stop	0
s10_etile_0 5 Sto	oped	0	Paste				Stop	0
s10_etile_0 6 Sto	pped	0					Stop	0
s10_etile_0 7 Sto	pped	0	Test Patter	n	>		Stop	0
s10_etile_0 8 Sto	oped	0	-				Stop	
s10_etile_0 9 Sto	oped	0	Generator/	checker Mode	>		Stop	0
			Loopback	Mode	>			
			Vop		>			
			Pre-empha	SIS	>			
			Adaptation	mode (L-Tile/H-	Tile) >			
			Adaptation	n mode (E-Tile)	>			
			Start		>	Start	Transceiver Lir	nk
			Stop					
			Stop			Start	Auto Sweep	
			Reset		>	Ctort	Fue Viewer	
Control Transceive	r Link	Link Auto Sv				Start	Eye viewei	
			Refresh			Start	Auto Sweep 8	LEye Viewer
			Status Polli	ng				
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ins			Export		>	recoury	Agaarcasti Di	

Figure 7. Starting the BER link test

Toolkits ⊠ Welc	come to the Tran	sceiver Toolkit	Transceiver	Toolkit	8	
Transmitter Chann	els Receiver Ch	annels Transcei	ver Links			
Show in table:	Current	MinMax Be	est			
Link Alias	Status	Bits tested	BER	Test pa	ttern Loopback mo	de Adaptation n
s10 etile 0 0	Stopped	0	0	PRBS7	Off	Stop
s10_etile_0 1	Stopped	0	0	PRBS7	Off	Stop
s10_etile_0 2	Running	8.6653E12	4.7476E-10	PRBS31	Off	Stop
s10_etile_0 3	Running	8.6661E12	0	PRBS31	Off	Stop
s10_etile_0 4	Running	8.6516E12	4.7476E-10	PRBS31	Off	Stop
s10_etile_0 5	Running	8.6516E12	4.7538E-10	PRBS31	Off	Stop
s10_etile_0 6	Running	C	0	Looncost.	Off	Stop
s10_etile_0 7	Running	Сору			Off	Stop
s10_etile_0 8	Running	Paste			Off	Stop
sto_etile_0[9]	Kunning				Off	Stop
		Test Pattern		>		
		Congrator/ch	ockor Modo	、 、		
		Generator/chi	ecker mode			
		Loopback Mo	de	>		
		V <sub>OD</sub>		>		
		Pre-emphasis		>		
		Adaptation m	ode (L-Tile/H-	Tile) >		
		Adaptation m	ode (E-Tile)	>		
		Start		>		
Control Transce	eiver Link	Stop			Link Auto Sweep & E	ye Viewer
		Reset		>	Reset Checker	
		Defrech			Reset Sweep	
ady registered.		Status Polling		L	dition the direct	own conservation
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3S1)@2#USB-1 to a.	.sof	Import		>	ss the functionality	v provided. Yo
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#### Figure 8. Resetting checkers

Link Alias	Status	Bits tested	BER	Test pattern	Loopback mode	Adaptation mo	V <sub>OD</sub>	Pre-emphasis	Status Polling
s10_etile_0 0	Stopped	0	0	PRBS7	Off	Stop	0	0/0/0/0	$\checkmark$
s10_etile_0 1	Stopped	0	0	PRBS7	Off	Stop	0	0/0/0/0	$\checkmark$
s10_etile_0 2	Running	2.3362E12		PRBS31	Off	Stop		0/0/0/0	$\checkmark$
s10_etile_0 3	Running	2.3418E12		PRBS31	Off	Stop		0/0/0/0	$\checkmark$
s10_etile_0 4	Running	2.3313E12		PRBS31	Off	Stop		0/0/0/0	$\checkmark$
s10_etile_0 5	Running	2.3369E12		PRBS31	Off	Stop		0/0/0/0	$\checkmark$
s10_etile_0 6	Running	2.2900E12		PRBS31	Off	Stop		0/0/0/0	$\checkmark$
s10_etile_0 7	Running	2.3314E12		PRBS31	Off	Stop		0/0/0/0	$\checkmark$
s10_etile_0 8	Running	2.3233E12		PRBS31	Off	Stop		0/0/0/0	$\checkmark$
s10_etile_0 9	Running	2.3386E12		PRBS31	Off	Stop		0/0/0/0	$\checkmark$

Figure 9. CDR lock-to-data status, number of bits tested and BER result

Toolkits 🛛 Welcome to the Transceiver	Toolki	t 🖾	Transceiver Too	lkit 🛛			
Transmitter Channels Receiver Channels	Tran	sceiver	Links				
Show in table: Current MinMa	ax	Best	:				
Link Alias Status Bits	tested		BER	Test pattern		Loopback mode	Adaptation
s10 etile 010 Stopped 0			0	PRBS7		Off	Stop
s10 etile 0 1 Stopped 0			0	PRBS7		Off	Stop
s10 etile 0 2 Running 1.69	78E13		0	PRBS31		Off	Stop
s10 etile 0 3 Running 1.69	84E13		0	PRBS31		Off	Stop
s10_etile_0 4 Running 1.69	74E13		0	PRBS31		Off	Stop
s10_etile_0 5 Running 1.69	8(	~				Off	Stop
s10_etile_0 6 Running 1.69	84	Copy	y		~	Off	Stop
s10_etile_0 7 Running 1.69	74	Paste				Off	Stop
s10_etile_0 8 Running 1.69	68					Off	Stop
s10_etile_0 9 Running 1.69	s10_etile_0 9 Running 1.6980 Test Pattern					Off	Stop
		-	- accent				
		Gene	erator/checker N	lode	>_		
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		Pre-	emphasis		>		
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		Ada	deptation mode (E Tile)				
		Ada	plation mode (E	-me)	_		
		Start	ł		>		
	_	C					
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/ II				THE OTHER PROPERTY AND		ssuing Tel sour	ce command

Figure 10. Enabling serial Loopback mode

## Conclusion

The design example provides a reference on how to perform BER link test with Intel<sup>®</sup> Stratix<sup>®</sup> 10 TX PAM4 channels running at 51Gbps interfacing with QSFPDD 1x1 module.

#### References

• E-Tile Transceiver PHY User Guide https://www.intel.com/content/dam/www/programmable/us/en/pdfs/ug\_etile\_xcvr\_phy.pdf

## **Revision History**

Date	Version	Changes
June 10, 2019	1.0	Initial Release