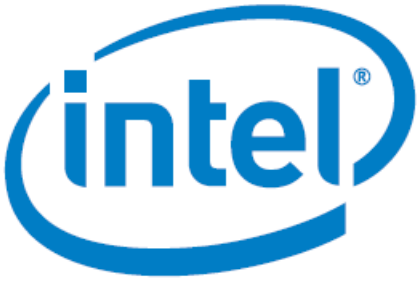

Intel® Stratix® 10 TX PAM4 8 x 51Gbps with QSFPDD 1x1 Example Design 18.1 User Guide

Date: 6/10/2019

Revision: 1.0

Table of Contents

Introduction

The objective of this this design example is to demonstrate Intel® Stratix® 10 TX PAM4 8x51Gbps channels interfacing with QSFPDD 1x1 module. QSFPDD 1x1 loopback module is used to perform loopback from the transmitters back to the receivers. Transceiver toolkit is used to demonstrate the link BER testing as well as for links status monitoring. In-System Sources and Probes (ISSP) is used to provide reset control to the transceivers.

The reference design requires the following hardware and software to run the test:

- Intel® Quartus® Prime Pro Edition 18.1
- Intel® Stratix® 10 TX Signal Integrity Development Kit
  https://www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/kits-s10-tx-si.html
- One QSFP-DD Electrical Passive Loopback Module ML4062
  https://multilaneinc.com/product/ml4062/

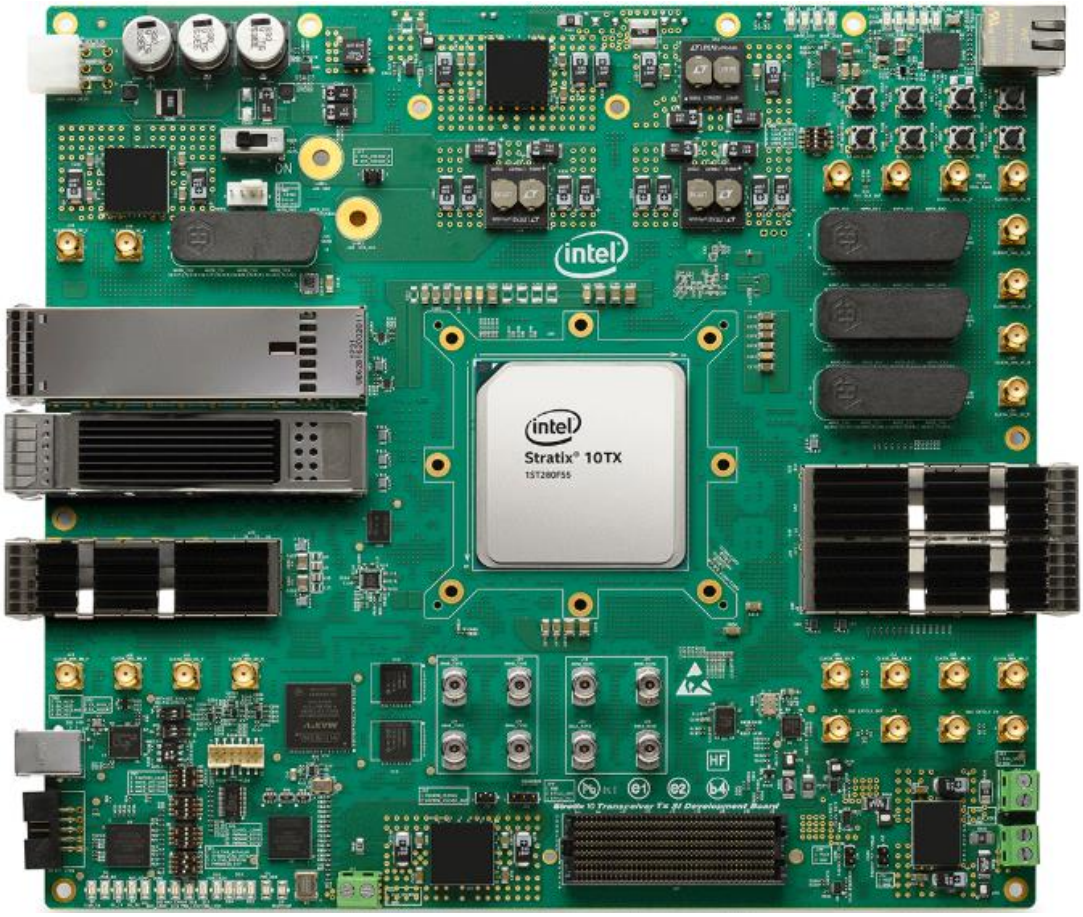

Figure 1. Intel® Stratix® 10 TX Signal Integrity Development Kit

Theory of Operation

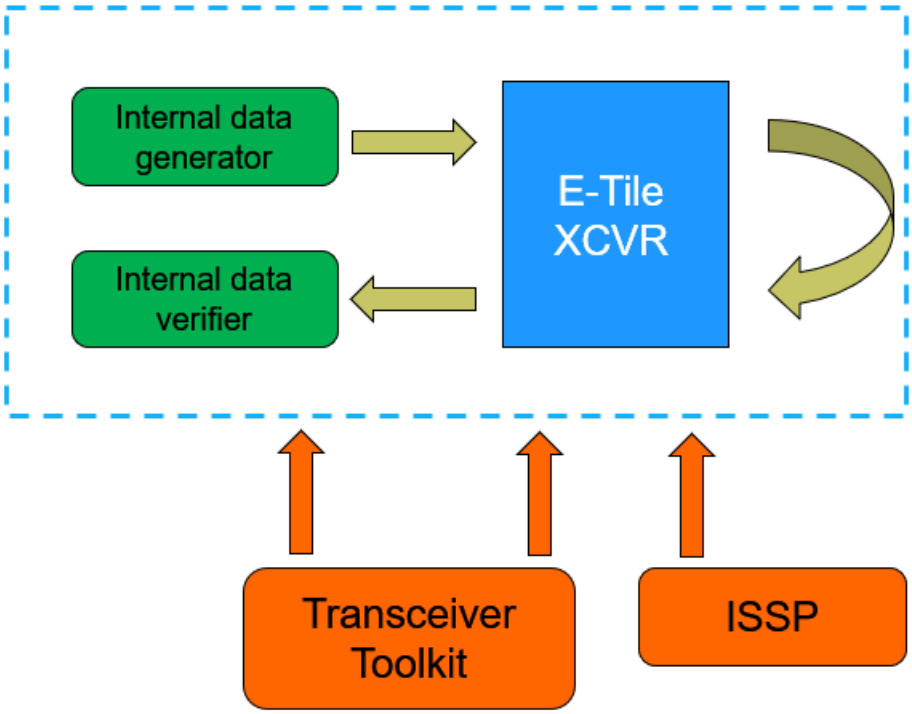

Figure 2. Block diagram of modules in the reference design

Figure 2 shows the high-level modules in the example design as well as the interfaces among the modules. The Intel® Stratix® 10 TX E-Tile Transceiver Native PHY is used to configure and implement the hard transceiver channels. ISSP allows real time user control on the resets for the transceivers. The Transceiver Toolkit is used to allow real time control on the transceiver channels, status monitoring and BER link testing. During BER test, Transceiver Toolkit will interface with the internal data generator and checker to generate PRBS pattern as well as to check for bit error.

In this design, there are 8 PAM4 channels configured to run at 51Gbps. The data from transmitter is loopback to receiver using QSFPDD 1x1 loopback module. We will use Transceiver Toolkit to simultaneously monitor and control all the 8 channels.

For further details on E-Tile transceiver architecture, you may refer to the E-Tile Transceiver PHY User Guide -> “E-Tile Transceiver PHY Architecture” section.

For further details on E-Tile transceiver data generator and verifier, you may refer to the E-Tile Transceiver PHY User Guide -> “Data Pattern Generation” and “Data Pattern Verifier” sections.

How to Setup the Hardware for Link Test

Follow these steps to setup the hardware to run the reference design:

1. Connect the QSFPDD loopback module to the QSFPDD 1x1 optical transceiver cage on the Intel® Stratix® 10 TX Signal Integrity Development Kit as in Figure 3
2. Use the default switching settings of the development kit
3. Connect the USB cable to the USB Blaster connector on the development kit
4. Connect the power adapter shipped with the development board to power supply jack
5. Turn On the power for the development kit. The hardware system is now ready for programming

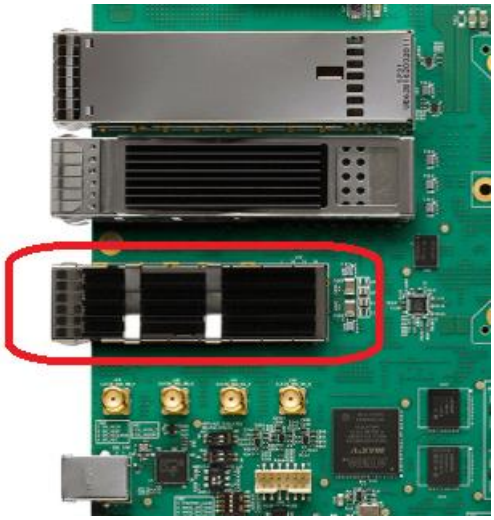

Figure 3. QSFPDD 1x1 optical transceiver cage

How to Reconstruct and Running the Reference Design

Follow these steps to reconstruct, compile and run the design:

1. Follow the instruction in the Design Store to prepare the design template and load the design into Intel® Quartus® Prime Pro Edition Version 18.1
2. Perform full compilation with the design
3. Program the SOF file generated into the development kit
4. After the programming is completed, open the Tools -> System Debugging Tools -> Transceiver Toolkit and establish connection to the Intel® Stratix® 10 TX device as shown in Figure 4.
5. You should observe ten channels auto-populated in Transceiver Toolkit. We will focus on the 8 PAM4 channels which are logical channel 2 to 9 as highlighted in the figure. Logical channel 0 and 1 are for SMA interface which are not discussed in this user guide
6. Go to the Receiver Channels tab. By default, you should see the status = Running for all channels. Select all channels and Right click -> Stop the receivers as shown in the Figure 5

7. Go to the Transceiver Links tab. Select the 8 PAM4 channels -> right click -> Test Pattern. Then select your target Test Pattern. In this example, PRBS31 pattern is selected as shown in Figure 6
8. To start the BER link test, select the 8 PAM4 channels -> right click -> Start -> Start Transceiver Link as shown in Figure 7
9. After the link test starts, you may observe some channels with initial BER. Reset the checkers by selecting the 8 PAM4 channels -> right click -> Reset -> Reset Checker as shown in Figure 8.
10. After resetting, you can observe the number of bits tested and BER as shown in the Figure 9. The Status = Running and Green also indicates that the CDR has successfully locked-to-data
11. You may also perform real-time enabling on the loopback mode, changing VOD and pre-emphasis parameters from Transceiver Toolkit to facilitate link test by selecting a channel and right click as shown in the Figure 10

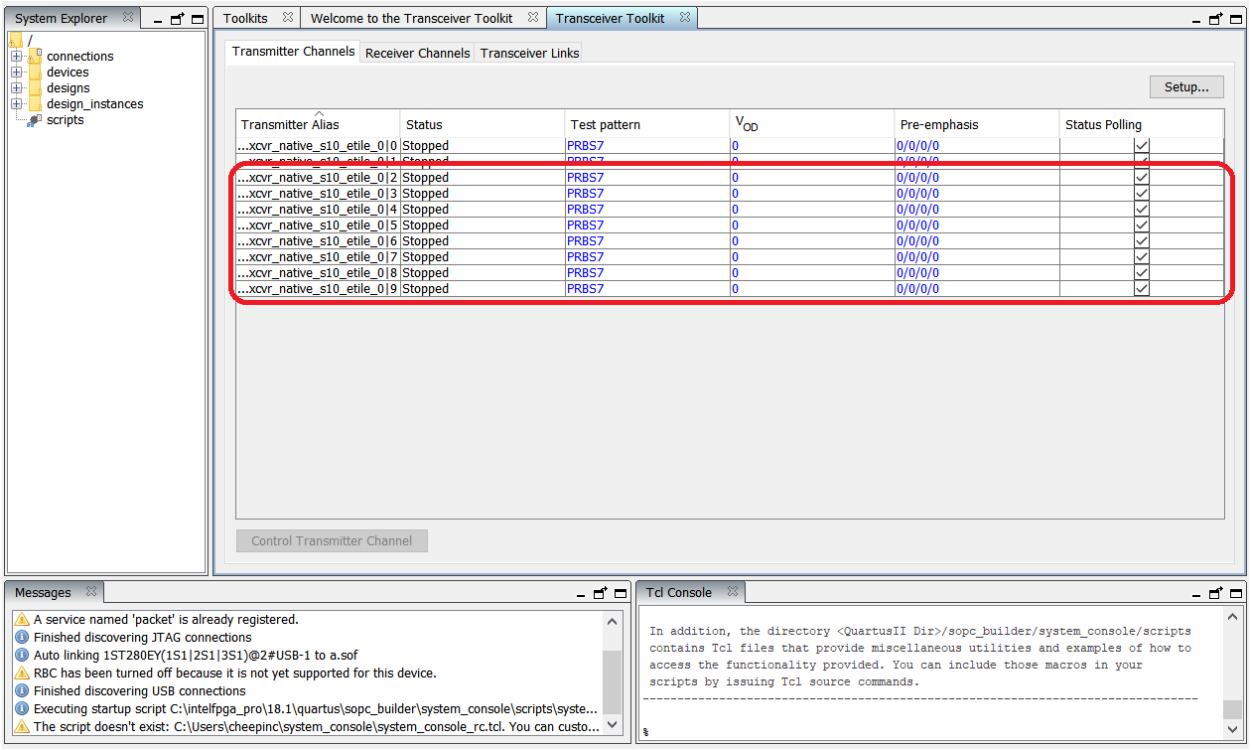

Figure 4. Opening Transceiver Toolkit and establishing connection to device

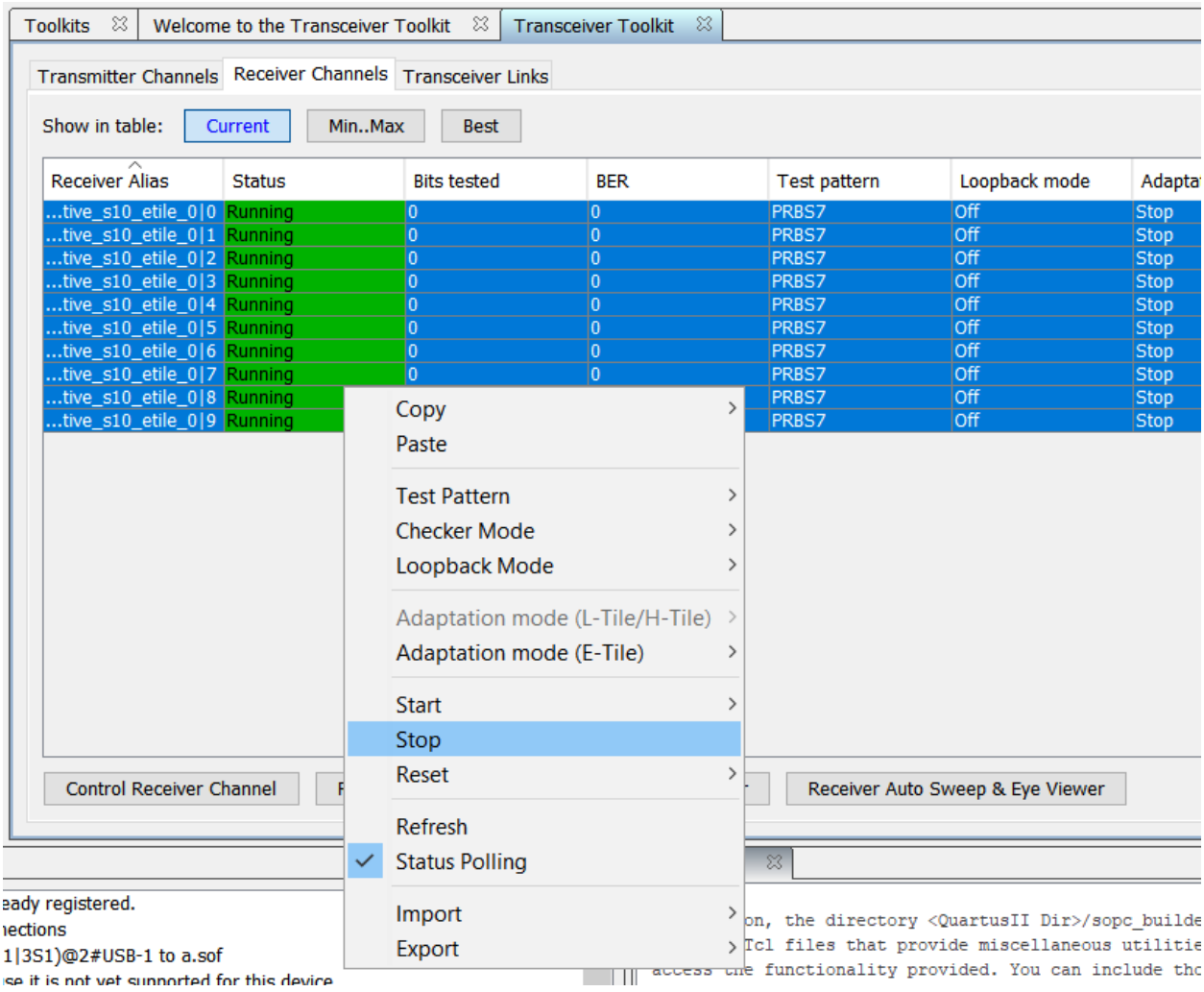

Figure 5. Stopping the receivers

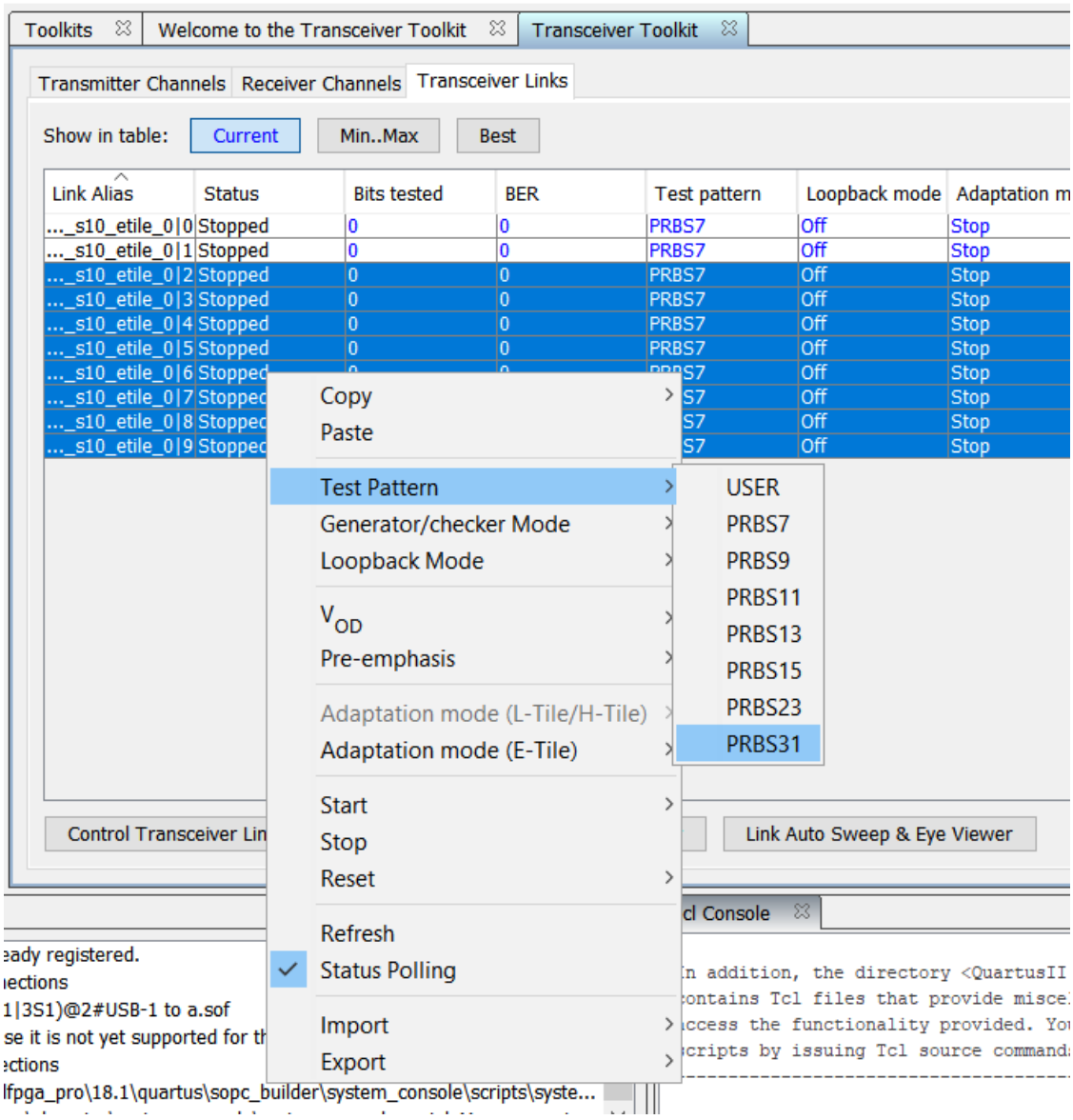

Figure 6. Selecting the target test pattern

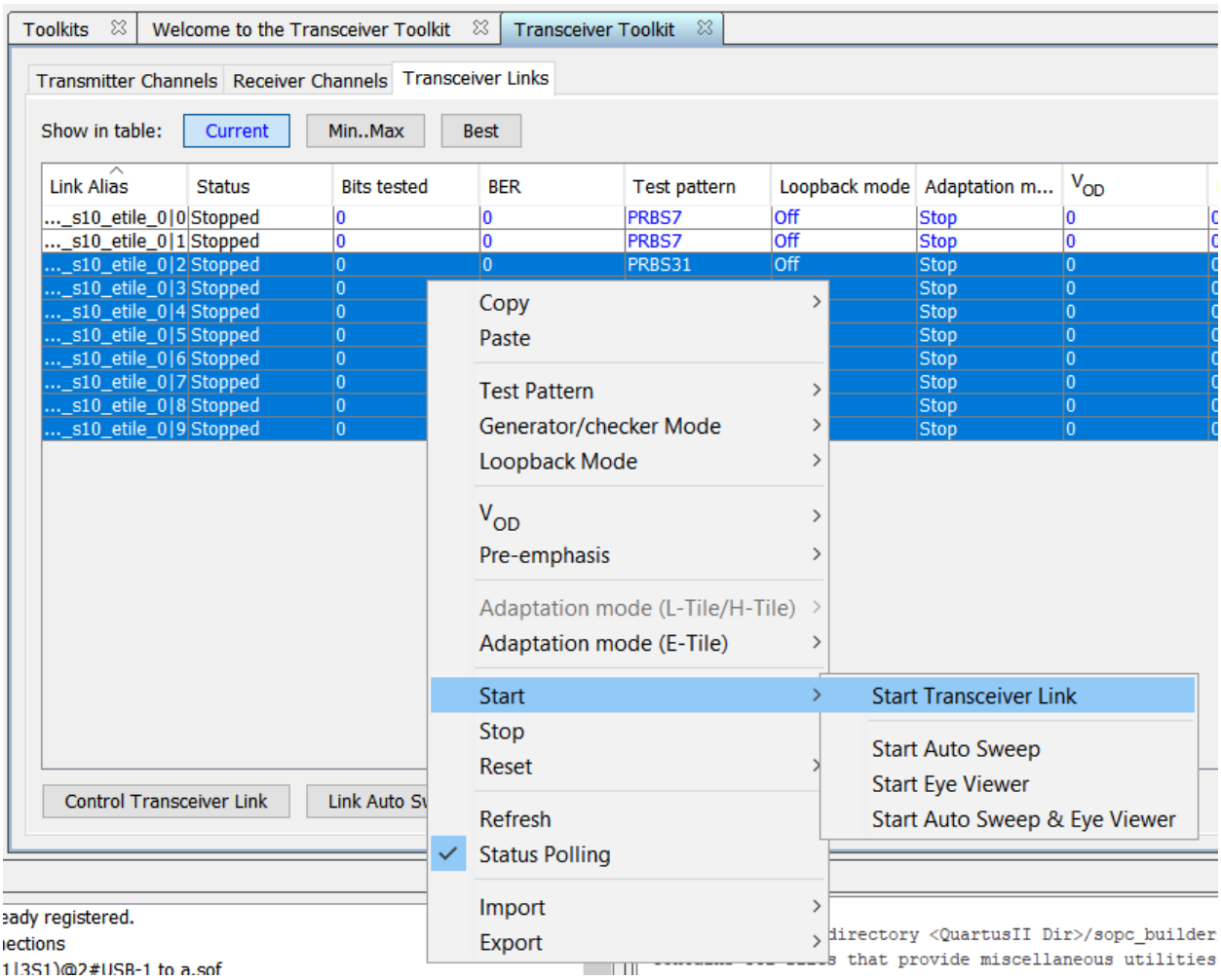

Figure 7. Starting the BER link test

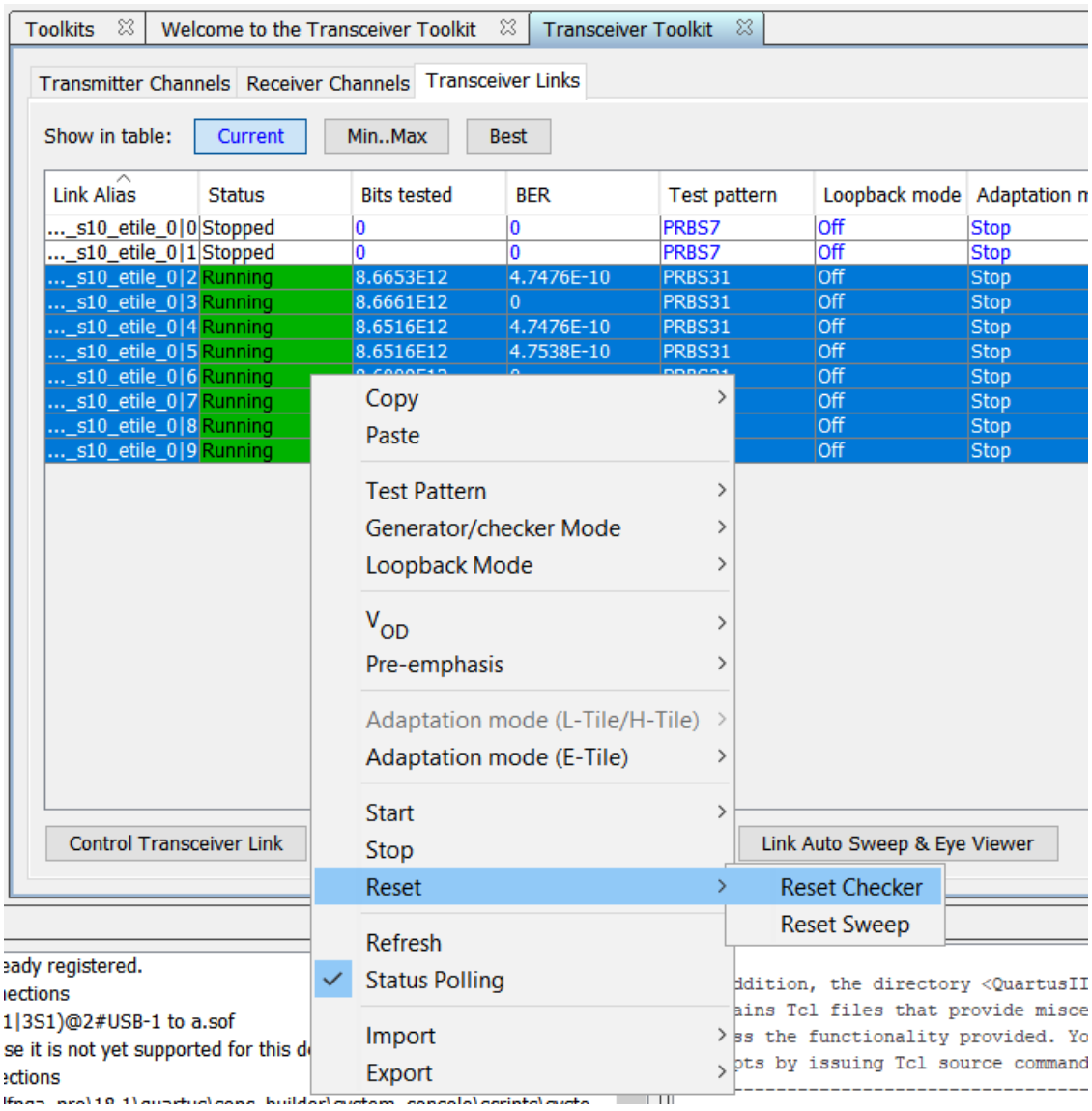

Figure 8. Resetting checkers

Link Alias	Status	Bits tested	BER	Test pattern	Loopback mode	Adaptation mo...	V_{OD}	Pre-emphasis	Status Polling
..._s10_etile_0|0	Stopped	0	0	PRBS7	Off	Stop	0	0/0/0/0	☑
..._s10_etile_0|1	Stopped	0	0	PRBS7	Off	Stop	0	0/0/0/0	☑
..._s10_etile_0|2	Running	2.3362E12	0	PRBS31	Off	Stop	0	0/0/0/0	☑
..._s10_etile_0|3	Running	2.3418E12	0	PRBS31	Off	Stop	0	0/0/0/0	☑
..._s10_etile_0|4	Running	2.3313E12	0	PRBS31	Off	Stop	0	0/0/0/0	☑
..._s10_etile_0|5	Running	2.3369E12	0	PRBS31	Off	Stop	0	0/0/0/0	☑
..._s10_etile_0|6	Running	2.2900E12	0	PRBS31	Off	Stop	0	0/0/0/0	☑
..._s10_etile_0|7	Running	2.3314E12	0	PRBS31	Off	Stop	0	0/0/0/0	☑
..._s10_etile_0|8	Running	2.3233E12	0	PRBS31	Off	Stop	0	0/0/0/0	☑
..._s10_etile_0|9	Running	2.3386E12	0	PRBS31	Off	Stop	0	0/0/0/0	☑

Figure 9. CDR lock-to-data status, number of bits tested and BER result

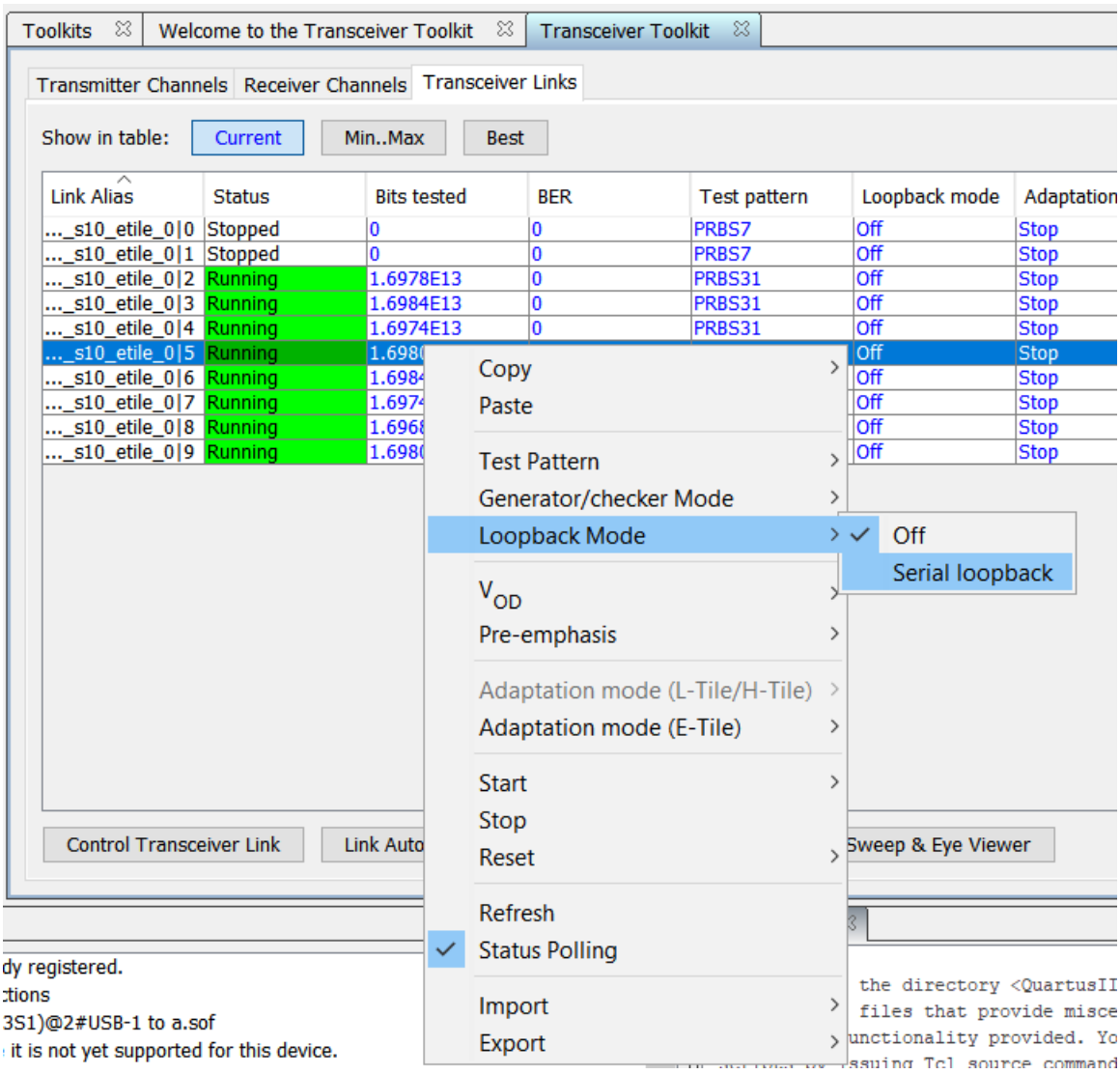

Figure 10. Enabling serial Loopback mode

Conclusion

The design example provides a reference on how to perform BER link test with Intel® Stratix® 10 TX PAM4 channels running at 51Gbps interfacing with QSFPDD 1x1 module.

References

- E-Tile Transceiver PHY User Guide
  https://www.intel.com/content/dam/www/programmable/us/en/pdfs/ug_etile_xcvr_phy.pdf

Revision History

Date	Version	Changes
June 10, 2019	1.0	Initial Release