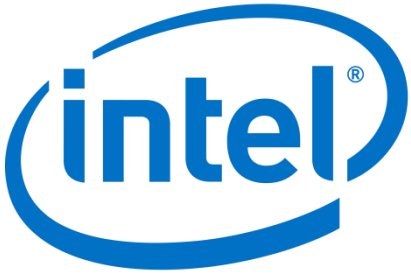


Cyclone 10 GX HDMI 4Kp60 with Video and Image Processing Pipeline Reference Design User Guide

Author: Wei Liang Lim

Date: Sept 2018

Revision: 2.0

Contents

1 Introduction

This reference design demonstrates the Intel FPGA High Definition Multimedia Interface (HDMI) 2.0 video connectivity IP core with a video processing pipeline based on IP cores from the Intel FPGA Video and Image Processing (VIP) Suite. This design is intended as a simple reference for interconnectivity between the HDMI IP core and the VIP Suite. Additionally, this design demonstrates the use of separate clocks for the RX and TX HDMI IP cores, allowing for differing RX and TX video resolutions.

The reference design targets Cyclone 10 GX devices and uses the latest 4K ready IP cores from the VIP Suite in the Intel FPGA Complete Design Suite v18.0.1Pro

1.1 Reference Design Features

- Files for targeting Cyclone 10 GX FPGA Development Kit
- Input: HDMI 2.0 connectivity supporting resolutions up to and including 2160p at 60 fps
- Output: HDMI 2.0 connectivity locked at a resolution of 2160p at 60 fps
- Input and output hot-plugging support
- Single 10-bit RGB processing pipeline with Mixer to overlay input video over a color bar background
- Triple buffer video frame buffer to provide frame rate conversion from a variable input frame rate to the fixed output rate of 60 fps

Note: This reference design does not support audio.

2 Hardware and Software Requirements

2.1 Hardware Requirements

This design requires the following hardware:

- Cyclone 10 GX FPGA Development Kit
- Bitec FMC HDMI Daughter Card (Rev 11)
- HDMI 4K capable PC/GPU
- HDMI 4K capable monitor
- Two HDMI cables

Tested GPU Models:

- Nvidia GeForce GTX1080
- Quadro M1000M
- Intel Kirbylake GT3

Tested Monitor Models:

- LG 27UD68P
- Dell P2415Qb

2.2 Software Requirements

This design requires the following software:

- Windows or Linux OS
- The Intel FPGA Complete Design Suite v18.0.1Pro that includes:

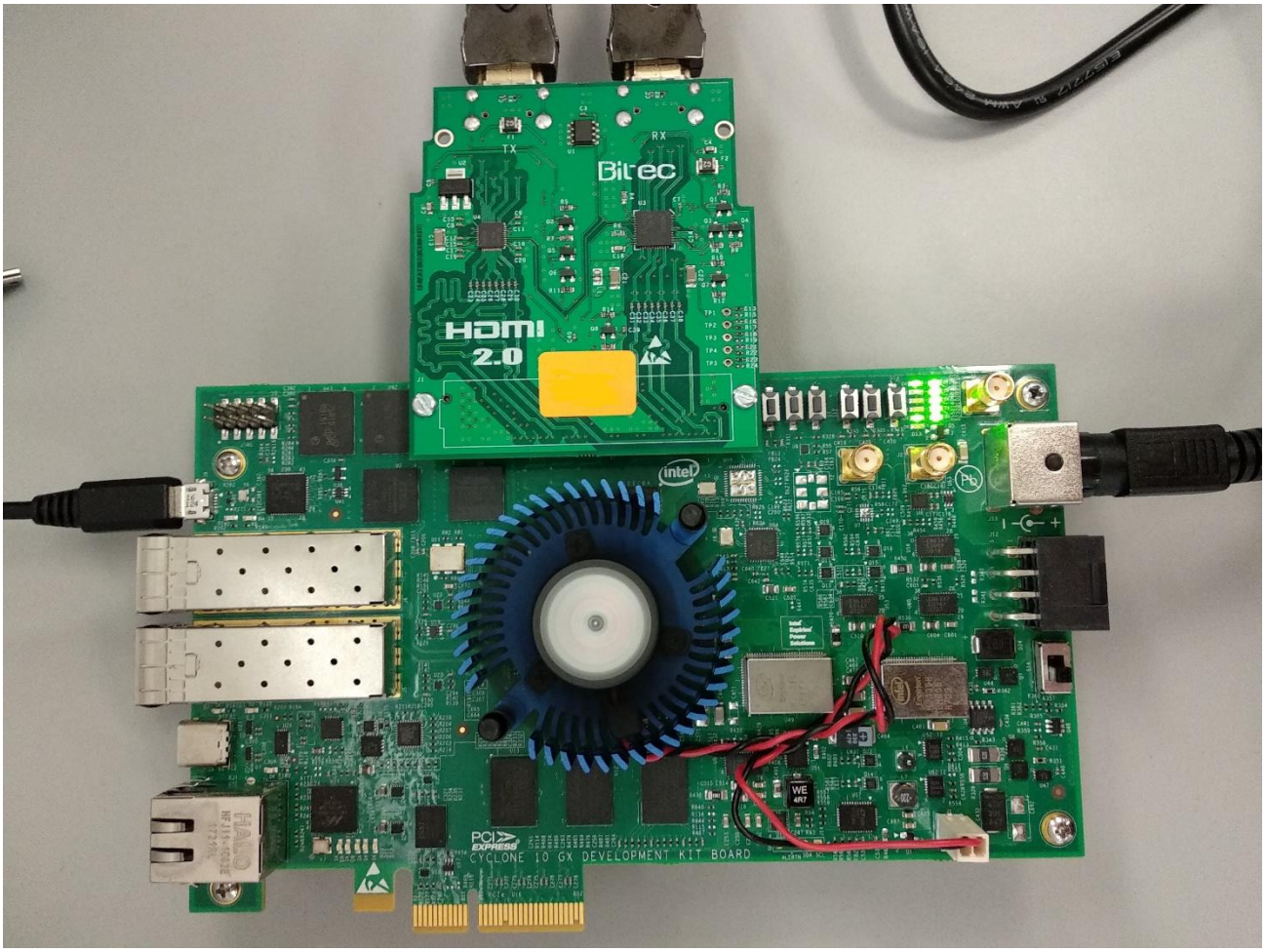
- The Quartus Prime software
- Platform Designer
- Nios II EDS
- IP Library (including the VIP Suite)

3 Reference Design Installation Files

File or Directory Name	Description
edid_ram.ip **EDID.hex** **edid_ram**	The HDMI sink's EDID table interface and contents files.
PLL_SYS.qsys	The PLL that generates the system clocks for the top-level design.
qsys_vip_pipeline.qsys	The Platform Designer system containing the video processing pipeline for the reference design along with the Nios II processor and its associated components.
qsys_vip_pipeline.sopcinfo	The information file for the qsys_vip_pipeline Platform Designer system and the Nios II software project in Eclipse.
top.qpf and top.qsf	The Quartus Prime project and settings files for the reference design.
hdmi_vip.v	The top-level HDL file for this reference design.
clock_control **edid_ram** **gxb** **hdmi_rx** **hdmi_tx** **PLL_SYS**	Directories containing the generated IP blocks that make up the reference design.
i2c_slave	Directory containing the I2C interface associated with the HDMI RX core. The I2C slave has interfaces to the EDID RAM and the SCDC interface on the HDMI Rx core.
non_acds_ip.ipx **non_acds_ip/debounce.v**	Non-IP library cores that the reference design uses. Including the debounce block for the hotplug detect signal.
master_image/hdmi_vip.sof	A pre-built .sof image of the reference design. Can be used to test the design without having to compile and build it first.
sdc/mr.sdc	The **.sdc** contraints file for the HDMI's multi-rate reconfiguration circuitry.
sdc/hdmi_vip.sdc	The **.sdc** contraints file for the top-level design. Defines the top-level clocks in the design and sets timing and false paths to and from the top-level connections.
software/vip_control_src.zip	A **.zip** file containing the software source tree.
software/vip_control/mem_init	Directory containing the pre-built RAM contents for the Nios II Processor.

4 Hardware Setup

The diagram below shows the completed hardware setup with Rev 11 Bitec HDMI 2.0 FMC card.



1. Fit the Bitec HDMI 2.0 FMC card into FMC Port on Cyclone 10 GX FPGA development board.
2. Ensure the power switch (S14) is switched off, then connect the power connector.
3. Connect a USB-Blaster II download cable from the computer to the MicroUSB Connector (J9) on the Cyclone 10 GX development board.
4. Attach an HDMI 2.0 cable between the HDMI source and the RX port of the Bitec HDMI 2.0 FMC card and ensure the source is active.
5. Attach an HDMI 2.0 cable between the HDMI display and the TX port of the Bitec HDMI 2.0 FMC card and ensure the display is active.
6. Power up the board by switching on power switch (S14).

4.1 Board Status Lights

The Cylone 10 GX FPGA Development board has four status lights, each of which contains green LED. While the reference design is running, the board's status lights display the current status of the system.

LED (GREEN)	Description
0	HDMI RX – IOPLL Locked
1	HDMI RX – IP Core Ready
2	HDMI TX – IOPLL Locked
3	HDMI TX – IP Core Ready

Note: All the four status LEDs should be light up if everything works correctly.

5 Running the Reference Design

Intel provides a precompiled **hdmi_vip.sof** file as part of the installation files in the **master_image** directory. hdmi_vip.sof includes Nios II software to run the design. If you prefer to use the precompiled file, you can skip the compilation instructions.

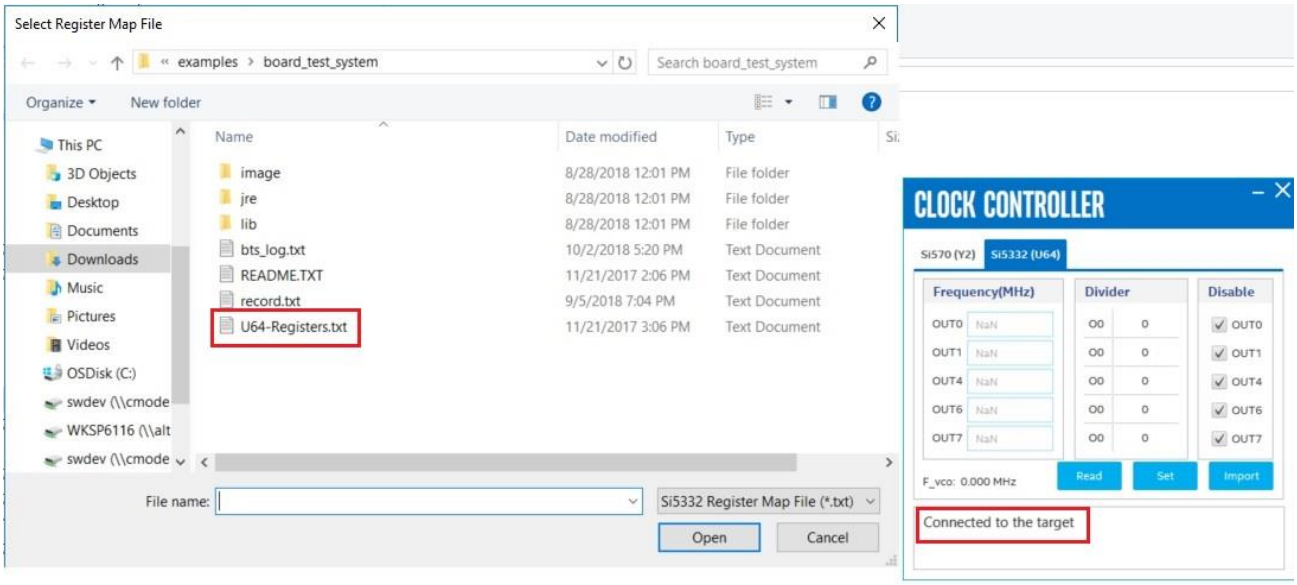
5.1 Compiling the Reference Design

1. Download and install the reference design.
2. Run command "**quartus_sh --platform -name c10gx_hdmi_vip.qar**" in Linux terminal or Nios II Command Shell to extract the project components.
3. Run "**sh compile.sh**" to compile the design.

The compilation creates the **top.sof** file in the **output_files** directory.

5.2 Running the Design on Hardware

1. Launch ClockController.exe which is in Cyclone 10 GX development kit board test system.
2. Wait for a while until JTAG connection is established. "Connected to the target" text will appear at the bottom of the GUI once the connection is established.
3. Click "Si5332 (U64)" tab and click "import" button to import default clock settings "U64-Registers.txt" for Si5332 clock controller.



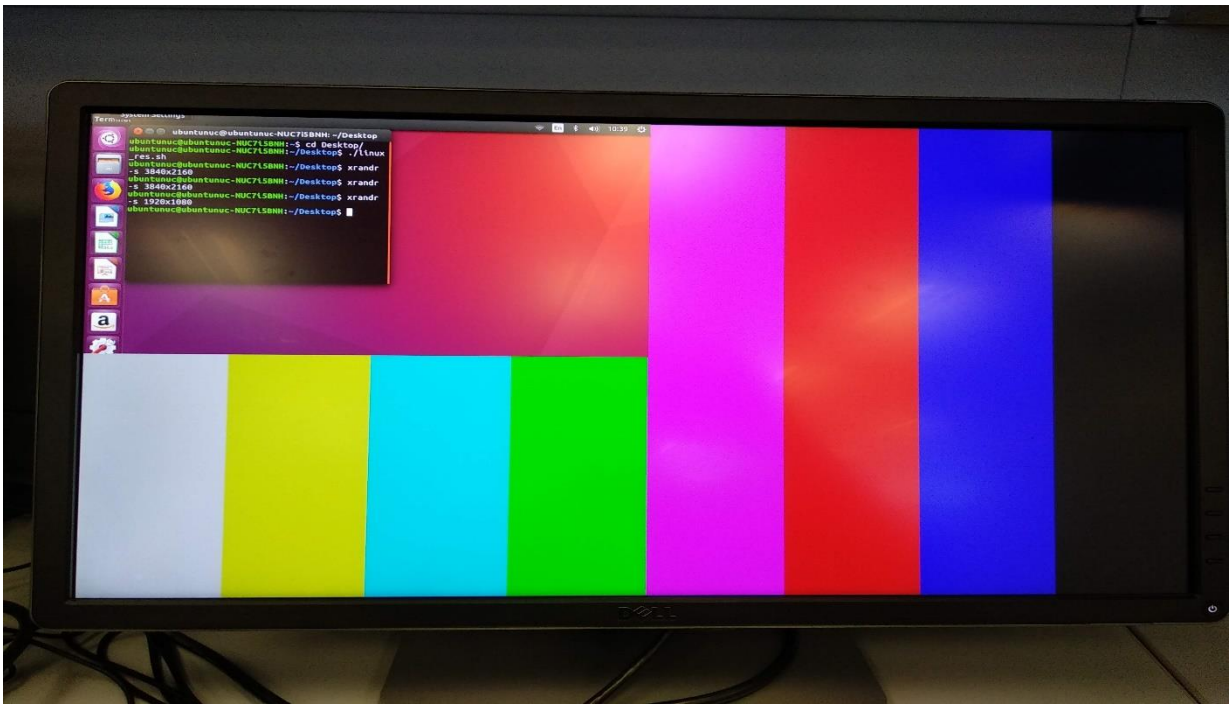
4. Set OUT1 to 250.0000, OUT2 to 21.1864 and OUT7 to 100.0000. OUT1 is reference frequency for HDMI Tx system, OUT2 is DDR3 reference clock and OUT7 is reference clock to system PLL generating clock to CPU and VIP.

5. In the Quartus Prime software, click **Tools > Programmer**.
6. In the **Programmer** window, click **Add File**, then:
    a. To use the precompiled **.sof** included with the design, select the **.sof** in the **master_image** directory.
    b. To use your compiled **.sof**, select the **.sof** in the **output_files** directory.
7. Launch **Nios II Command Shell** and enter command '***nios2-terminal***' to launch the Nios II terminal to display status messages during its operation.

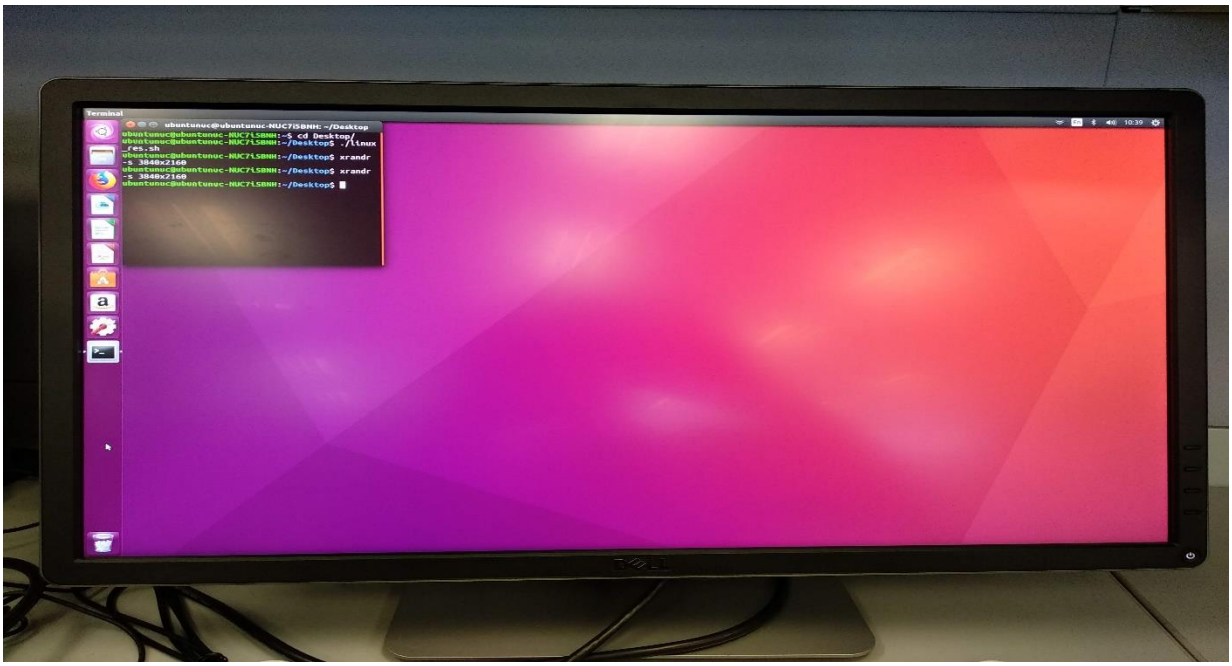
When the **.sof** is loaded into the device and the terminal program is running, examine the status lights. All the four status LEDs should be light up if everything works correctly.

Ensure that the PC/GPU HDMI source is outputting video. On the 4K HDMI compatible display, you should see the image from your PC/GPU overlaid on top of a 2160p color-bar background. Two examples are shown below for different input resolutions.

Option 1: If the input resolution is 1080p, you should see the display output from PC/GPU overlaid on top of a 2160p color-bar background as shown in the picture below:



Option 2: If the input resolution is 2160p, you should see the display output from your PC/GPU occupying the entire display, as shown in the picture below:

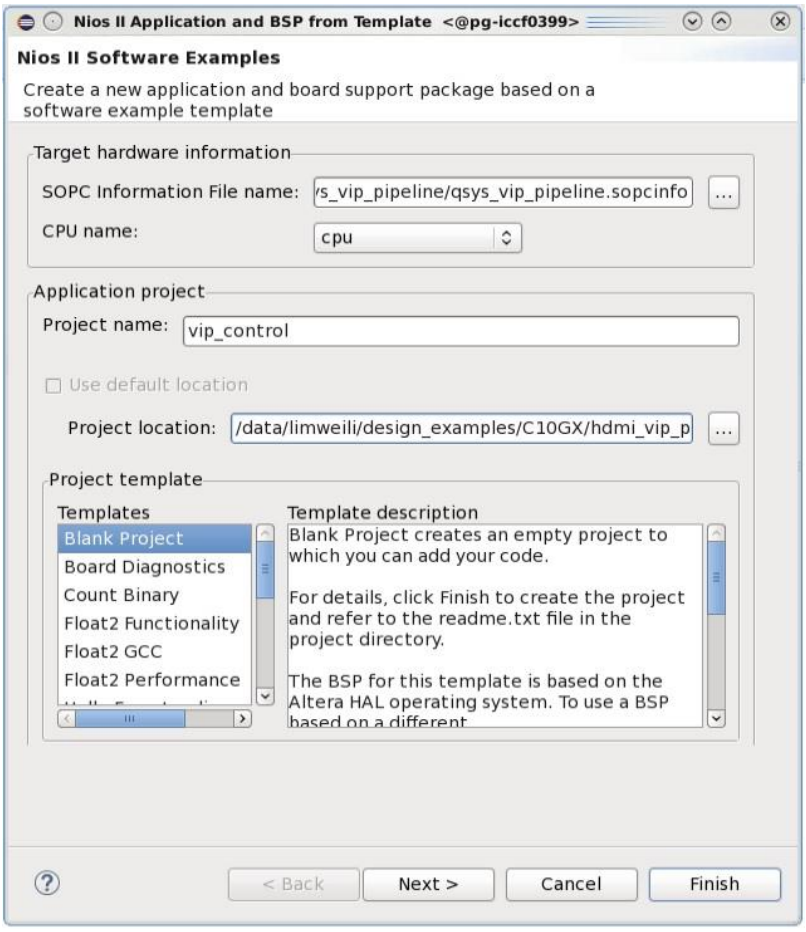


The input video resolution can be changed without reprogramming the device. The transceivers are dynamically reconfigured whenever the HDMI RX subsystem detects a change in the incoming video resolution. This design supports input resolutions up to and including 2160p.

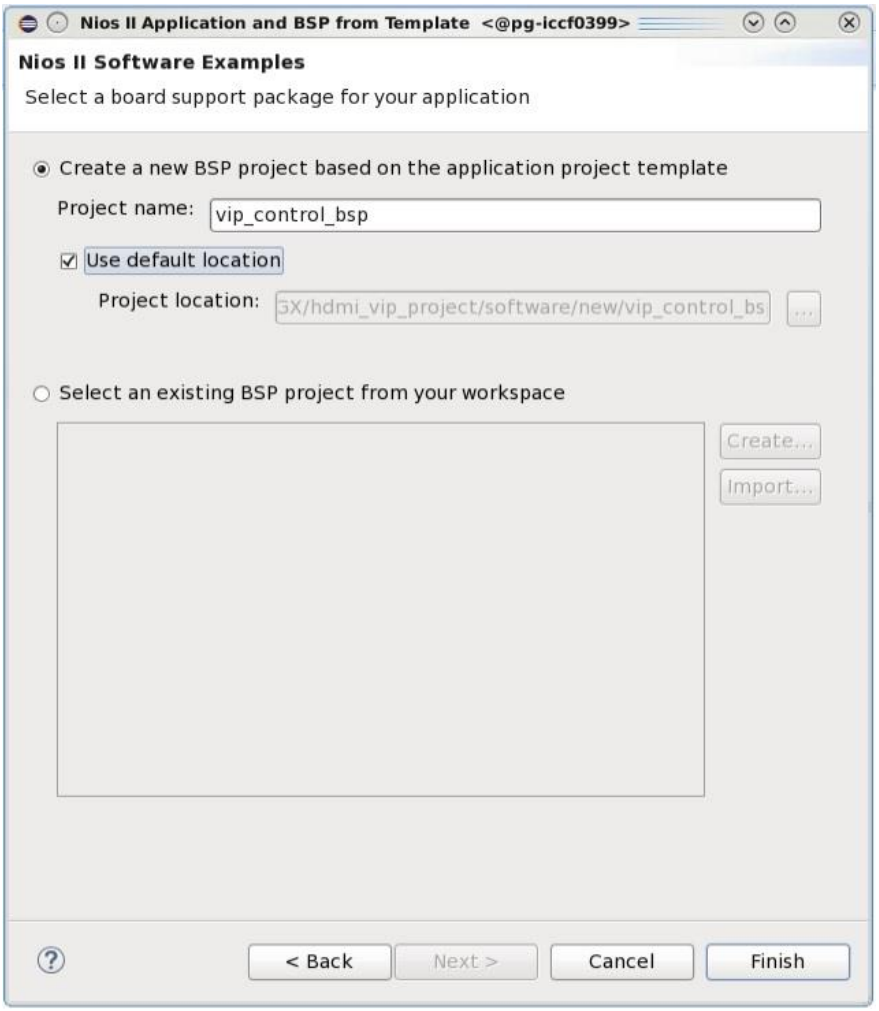
5.3 Compiling the Software

Compiling the software is only necessary if you want to make changes to the existing software running on the reference design. A precompiled version of the software is already included with the project. The source code for the design is in the **vip_control_src.zip** file in the **project/software** directory.

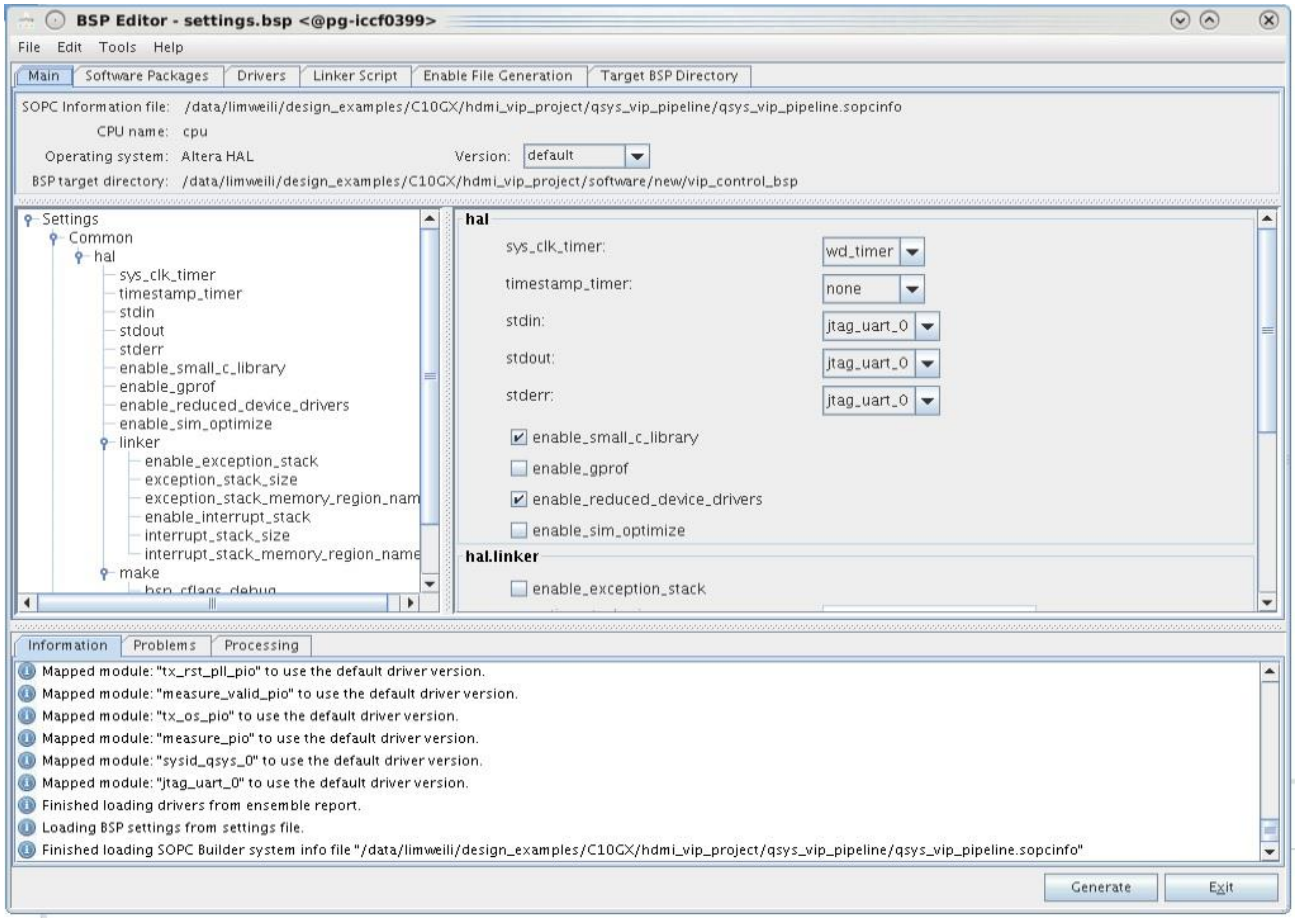
1. Ensure the **qsys_vip_pipeline.sopcinfo** file, which the software build process requires, is in the Quartus project directory.
2. Navigate to the Quartus project directory.
3. Launch Nios II software Build Tools for Eclipse: in the Quartus Prime software, click **Tools > Nios II software Build Tools for Eclipse**.
4. Select the **software** directory as the workspace folder and click **OK** to create a new workspace.
5. Click **File > New > Nios II Application and BSP from Template.** The **Nios II Application and BSP from Template** dialog box appears.



6. In the **SOPC Information File** box, select the **qsys_vip_pipeline.sopcinfo** file. The Nios II SBT for Eclipse fills in the CPU name with the processor name from the **.sopcinfo** file.
7. In the Project name box, type ***vip_control***.
8. Select **Blank Project** from the **Templates list** and then click **Next**.



9. Select **Create a new BSP project based on the application project template** with the project name **vip_control_bsp** and turn on **Use default location**.
10. Click **Finish** to create the application and the BSP based on the **.sopcinfo** file. After the BSP generates, the **vip_control** and **vip_control_bsp** projects appear in the **Project Explorer** tab.
11. In Windows Explorer, in the **software** directory, unzip the **vip_software_src.zip** file to generate a **vip_software_src** directory with all of the necessary software files.
12. Copy all these software files and the **vip** directory from the **vip_control_src** directory and in the Eclipse **Project Explorer** tab on the **vip_control** folder right-click and select **Paste**.
13. In the **Project Explorer** window, right-click **vip_control_bsp** and select **Nios II > BSP Editor**.



14. Turn on **enable_small_c_library** and **enable_reduced_device_drivers**, click **Generate** then **Exit**.
15. Select **Project > Build All** to generate the file **vip_control.elf** in the **software/vip_control** directory.
16. To build the **mem_init** file for the Quartus Prime compilation, right click on **vip_control** in the **Project Explorer** window and select **Make Targets > Build…**, then select **mem_init_generate** and click on **Build.** The Quartus Prime software generates the **qsys_vip_pipeline_cpu_ram.hex** file in the **software/vip_control/mem_init** directory.

6 Functional Description

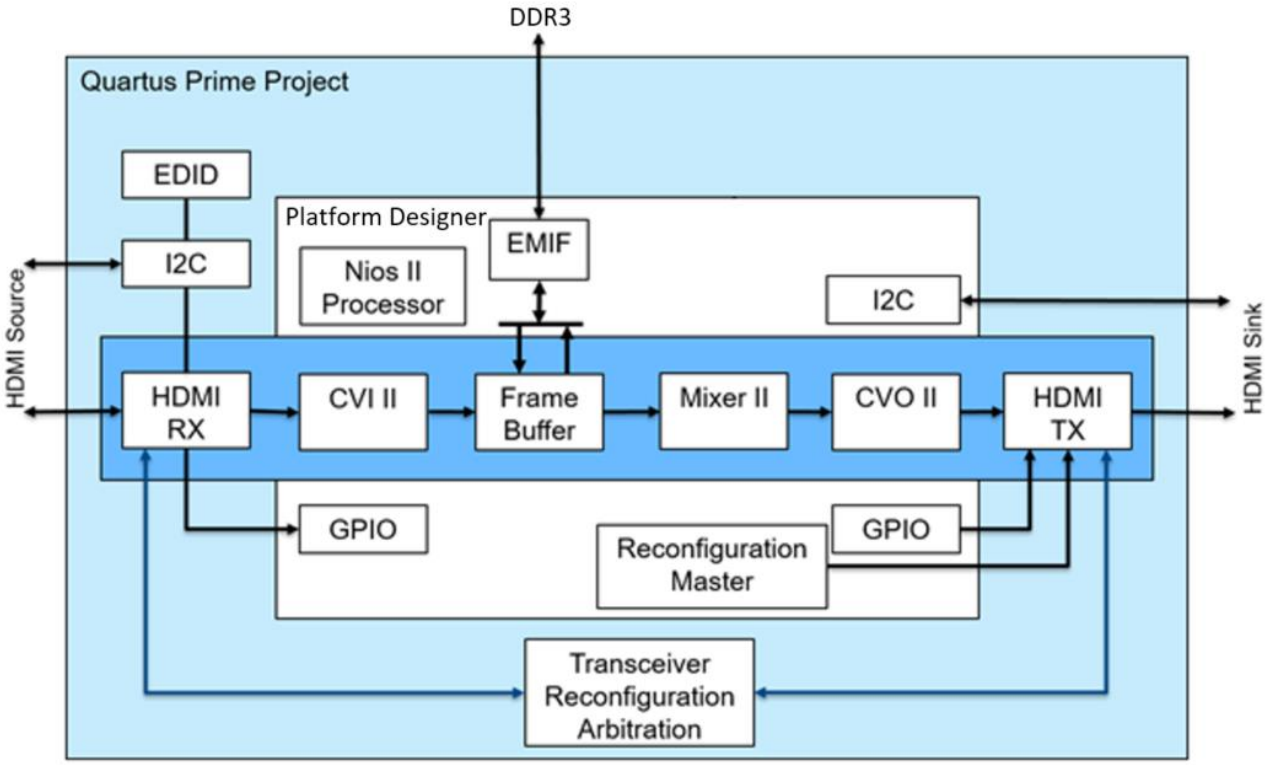
6.1 Overview

The reference design runs on Cyclone 10 GX FPGA development Kit. A Bitec FMC HDMI daughter card is used to receive video data from PC/GPU and transmit video data to a monitor. This design supports input video resolutions to the HDMI sink of 1080p or 2160p at 60 fps. The received video is converted to an Avalon-ST image stream and stored in external DDR3 memory. The buffered image is then mixed with a 3840 x 2160 color bar background, and the combined image is transmitted by the HDMI source to an HDMI 4K capable monitor. The output resolution from the HDMI source is locked at 2160p video at 60 fps.

The reference design is implemented using Intel FPGA's Platform Designer integration tool and standalone HDL modules. The design consists of the following major blocks or components:

- HDMI RX subsystem
  - HDMI sink IP core
  - HDMI sink IP core reconfiguration controller
  - Simplex RX Transceiver Native PHY IP core
  - IOPLL for HDMI IP core clocking
- HDMI TX subsystem
  - HDMI source IP core
  - Simplex TX Transceiver Native PHY IP core
  - TX fPLL
  - IOPLL for HDMI IP core clocking
- Platform Designer subsystem
  - Nios II CPU
  - Video and Image Processing pipeline
    - Clocked Video Input II (CVI)
    - Frame Buffer II
    - Mixer II
    - Clocked Video Output II (CVO)
  - DDR3 external memory interface
  - TX SCDC I2C Master
- Reconfiguration arbiter
- System PLL
- RX SCDC I2C Slave
- RX EDID I2C Slave

The diagram below shows the incoming video from the HDMI source on the left. The design processes the video through the video pipeline from left to right before passing the video out to the HDMI sink on the right.



6.2 HDMI RX Subsystem

The Bitec HDMI FMC card provides a buffer for the HDMI 2.0 signal from the HDMI source, then the HDMI RX IP core processes the signal. The HDMI RX IP processes the incoming HDMI signal without any software intervention. The HDMI RX subsystem contains a multi-rate reconfiguration controller that reconfigures the RX transceivers based on the incoming video resolution and frame rate. The resulting video signal from the HDMI RX IP is in a clocked video interface format.

The reference design configures the HDMI RX for 8-bit output. Logic between the HDMI RX and CVI bit extends each color plane to 10-bit.

6.3 Video and Image Processing

The VIP block receives video data from the HDMI RX, processes it, and outputs processed video data to the HDMI TX. Below is a brief description of each of the VIP suite IP core used in this design:

6.3.1 Clocked Video Input II

The clocked video input processes the clocked video interface signal from the HDMI RX IP core and converts it to Intel proprietary Avalon-ST Video signal format. This signal format strips all horizontal and vertical blanking information from the video leaving only active picture data. The Avalon-ST Video stream through the processing pipe is two pixels in parallel with three symbols per pixel. The clocked video input provides clock crossing for the conversion from the variable rate clocked video signal from the HDMI RX core to the fixed clock rate for the video IP pipeline

6.3.2 Frame Buffer II

The frame buffer uses the DDR3 memory to perform triple buffering that allows the video and image processing pipeline to perform frame rate conversion between the incoming and outgoing frame rates. The output frame rate is fixed at 60 fps, but the design can use any input frame rate up to 60 fps.

6.3.3 Mixer II

The mixer has one input, connected to the Frame Buffer to allow the design to show the output from the current video pipeline. The design only enables the mixer's input when it detects active, stable video at the clocked video input. Thus, the design maintains a stable output image at the output while hot-plugging at the input. The design generates a fixed size 2160p color bar image, and overlays the input image on top of the color bar background.

6.3.4 Clocked Video Output II

The clocked video output converts the Avalon-ST Video stream to the clocked video format. The design passes the clocked video format to the HDMI TX subsystem. The clocked video output adds horizontal and vertical blanking and synchronization timing information to the video. The Nios II processor programs the relevant settings in the clocked video output. The clocked video output converts the clock crossing from the fixed clock to the variable rate of the clock video output.

This reference design supports 4K resolution. The non-default parameter values of each IP core are listed in the table below:

IP Core	Parameter	Value
CVI II	Bits per pixel per color plane	10
	Number of pixels in parallel	2
	Use control port	On
Frame Buffer II	Maximum frame width	3840
	Maximum frame height	2160
	Bits per color sample	10
	Pixels in parallel	2
	Avalon-MM master(s) local ports width	512
	FIFO depth Write	512
	Av-MM burst target Write	64
	FIFO depth Read	512
	Av-MM burst target Read	64
	Frame dropping	On
	Frame repeating	On
	Drop invalid frames	On
	Run-time writer control	On
Mixer II	Maximum frame width	3840
	Maximum frame height	2160
	Bits per pixel per color plane	10
	Number of pixels in parallel	2
CVO II	Image width / Active pixels	3840
	Image height / Active lines	2160
	Bits per pixel per color plane	10
	Number of pixels in parallel	2
	Horizontal sync	88
	Horizontal front porch	176

Horizontal back porch	296
Vertical sync	10
Vertical front porch	8
Vertical back porch	72
Pixel FIFO size	3840
FIFO level at which to start output	3839
Use control port	On

6.4 HDMI TX Subsystem

The reference design configures the HDMI TX for 8-bit output. Logic between the CVO and HDMI TX removes the two LSBs from each 10-bit color plane output from the CVO.

6.5 Nios II

The software determines the current input resolution and input status automatically from the clocked video input.

The software running on the Nios II processor:

- Initializes the video IP cores
- Processes the following events:
  - HDMI transmit hot-plug
  - Stable input video availability
- Reconfigures the HDMI TX subsystem

The mixer provides a stable output image using its software programmable size background image. When the design detects a stable input stream from the clock video input block, the design enables the processing pipeline up to the mixer and the design overlays it for the mixer to show.

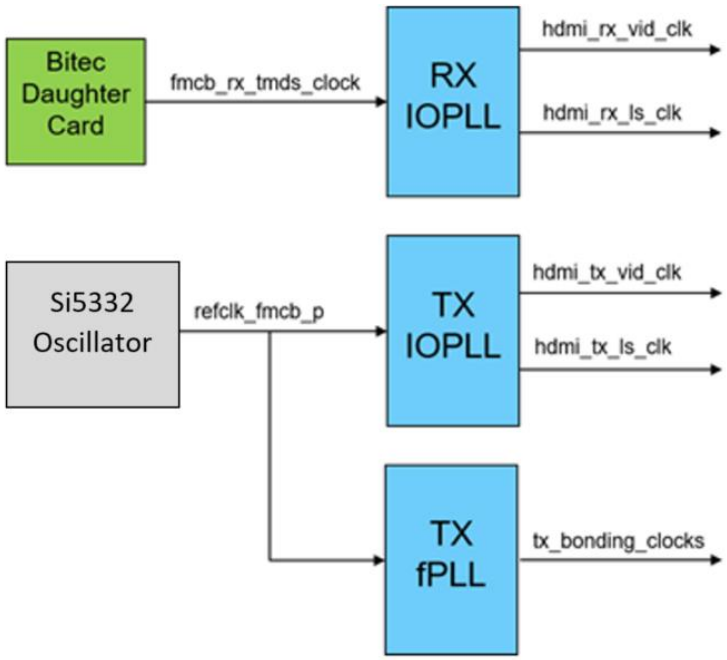
The reconfiguration master allows the Nios II processor to reconfigure the HDMI TX subsystem to the required output resolution. The software file **xcvr_gpll_rcfg.c** in the **software/vip_control_src** directory includes software routines to control the reconfiguration process. The main software source file (**main.cpp**) sets the required output resolution using the *set_output_resolution* function.

6.6 External Memory Interface

The Frame Buffer II uses the DDR3 memory to perform triple buffering that allows the video and image processing pipeline to perform frame rate conversion between the incoming and outgoing frame rates. The output frame rate is fixed at 60 fps, but the design can support multiple input frame rates up to 60 fps.

6.7 Clocking

This design demonstrates clock separation between the HDMI RX and HDMI TX subsystems. The input TMDS clock is buffered by the Bitec HDMI FMC daughter card along with the data. It is used by the HDMI RX subsystem as a reference clock to an IOPLL that generates the RX video and link clocks. The TX subsystem reference clock comes from an on-board programmable Si5332 oscillator. The TX subsystem reference clock is running at 250MHz. This clock is used as a reference clock to both an IOPLL that generates the TX video and link clocks, and an fPLL that generates the TX bonding clocks. This is illustrated in the figure below:



The table below contains a full listing of the clocks used in this design.

Signal Name	Description	Pin Number	IO Standard	Usage
clk_50	External 50MHz clock from crystal on the FPGA development kit	J23	1.8V	• Reference clock for system PLL • Clock for RX I2C slave interfaces
ddr3_pll_ref_clk	21.1864MHz clock from programmable oscillator on FPGA development kit	AA18	LVDS	• DDR3 external memory interface input reference clock
refclk_fmc_p	250MHz clock from programmable oscillator on FPGA development kit	U24	LVDS	• Reference clock for HDMI source IP core and HDMI TX subsystem
fmc_rx_tmds_clock	RX TMDS clock from Bitec FMC daughter card. Frequency depends on received video resolution.	W24	LVDS	• Reference clock and TMDS clock for HDMI sink IP core and HDMI RX subsystem
cpu_clk	Generated 100MHz clock from system PLL	N/A	N/A	• Clock for Nios II CPU and peripherals • AVMM clock for HDMI RX and TX subsystems

vip_clk	Generated 300Mhz clock from system PLL	N/A	N/A	• Clock for VIP suite pipeline Avalon-ST video datapath
hdmi_rx_vid_clk	Generated HDMI RX video clock from HDMI RX IOPLL. Frequency depends on received video resolution.	N/A	N/A	• Used internally by HDMI RX subsystem • Clock for interface between HDMI sink IP core and CVI
hdmi_rx_ls_clk	Generated HDMI RX link clock from HDMI RX IOPLL. Frequency depends on received video resolution.	N/A	N/A	• Used internally by HDMI RX subsystem
hdmi_tx_vid_clk	Generated 300MHz HDMI TX video clock from HDMI TX IOPLL	N/A	N/A	• Used internally by HDMI TX subsystem • Clock for interface between CVO and HDMI source IP core
hdmi_tx_ls_clk	Generated 300MHz HDMI TX link clock from HDMI TX IOPLL	N/A	N/A	• Used internally by HDMI TX subsystem • Used to synchronize General Control Packet (GCP), Auxiliary Video Information (AVI), and Vendor Specific InfoFrame (VSI) information

7 Revision History

Date	Version	Changes
June 2018	1.0	Initial Release
Sept 2018	2.0	Updated to Quartus Pro 18.0.1