

**1G/2.5G Ethernet Design Example for Stratix 10 Devices**

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# **Introduction**

This document describes design example that demonstrate the 1G/2.5G Ethernet operations for Stratix 10 device. The design example consists of Intel Stratix 10 Low Latency Ethernet 10G Media Access Controller (MAC) and Intel Stratix 10 1G/2.5G/5G/10G Multi-rate Ethernet PHY IP core in MBASE-T mode on Stratix 10 GX Transceiver Signal Integrity Development Kit.

# **Features**

This design offers the following features:

* Dual-speed Ethernet operations—1G and 2.5G.
* Support for two channels.
* Sequential random bursts tests. Users are able to configure the number of packets, payload data type, and payload size for each burst.
* Packet monitoring system is provided on the transmit and receive paths.
* Packet statistic will be reported for Ethernet MAC transmitter (TX) and Ethernet MAC receiver(RX)
* Testbench and simulation script.
* Tested with the Spirent TestCenter

# **Hardware and Software Requirements**

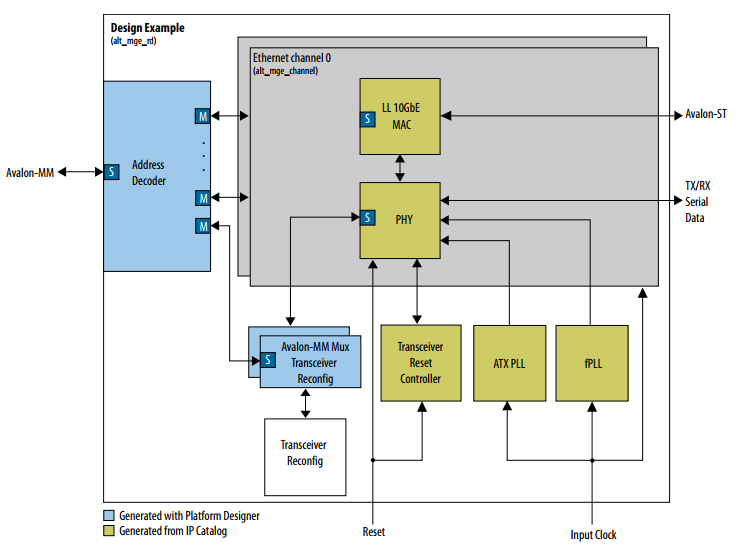
Intel uses the following hardware and software to test the design example in a Linux system:

* Intel Quartus® Prime Pro Edition version 17.1 software
* System Console
* ModelSim-AE and ModelSim-SE
* For hardware testing:
  + Intel Stratix 10 GX Signal Integrity (SI) Development Board (1SG280LU3F50E2VGS1)
  + Cables: Fiber optic cable and fiber optic loopback cable
  + Small form factor pluggable plus(SFP+) optical transceiver module
  + External generator (Spirent Tester)

# **Functional Description**

There are various components in this design example. The following block diagram shows the design components and the top-level signals of the design example.

**Figure 1. Block Diagram – 1G/2.5G Ethernet Design Example**



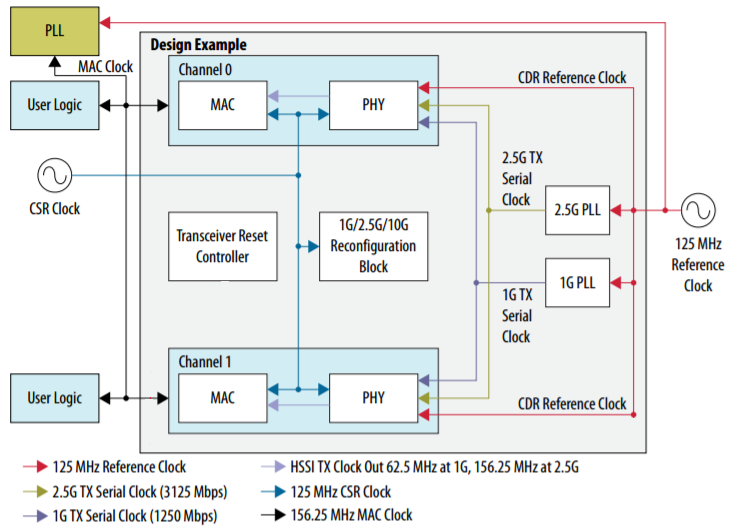
# **Design Components**

**Table 1. Design components**

|  |  |
| --- | --- |
| **Components** | **Description** |
| Low Latency 10G MAC IP | LL10G MAC IP core is generated with the following settings:   * Speed: 1G/2.5G * Data path options: TX & RX * Enable ECC on memory blocks: No * Enable supplementary address: Yes * Enable statistic collection: Yes * Statistic counters: Memory-based * Enable time stamping: No * All Legacy Ethernet 10G MAC Interfaces options: No |
| Multi-rate Ethernet PHY IP | 1G/2.5G Multi-rate Ethernet PHY IP (MBASE-T mode) |
| Transceiver Reset Controller | Altera Transceiver PHY Reset Controller IP core, used to perform digital/analog reset to the transceiver when dynamic reconfiguration is performed/PLL is out of lock. |
| Avalon-MM Mux Transceiver Reconfiguration | Provide system console(jtag) access to transceiver reconfig block through Avalon-MM interface |
| Transceiver Reconfiguration Block | Reconfigures the transceiver channel speed from 2.5Gbps to 1Gbps or vice versa. The transceiver channel is powered on with 2.5 Gbps. |
| ATX PLL | Generates a TX serial clock for the Stratix 10 2.5G transceiver |
| fPLL | One fPLL is to generate a TX serial clock for the Stratix 10 1G transceiver and another one is to generate MAC TX & RX clocks. |

# **Clocking Scheme**

**Figure 2. Clocking Scheme for the 1G/2.5G Ethernet Design Example**

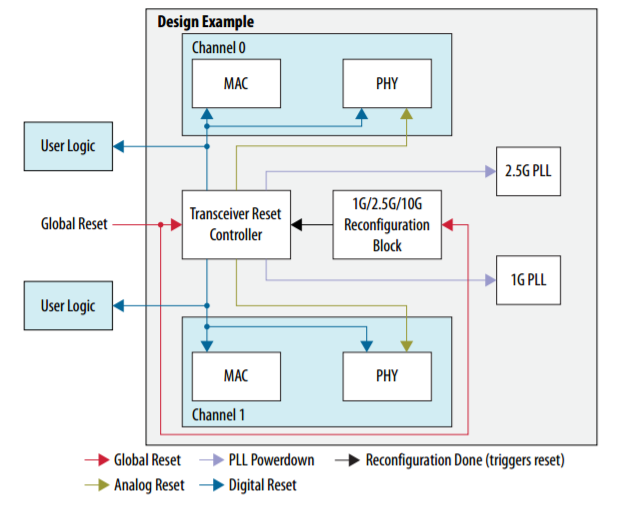


# **Reset Scheme**

The global reset signal of this design example is asynchronous and active – low.

Asserting this signal reset all channels and their components. Upon power-up, reset the  
 design example.

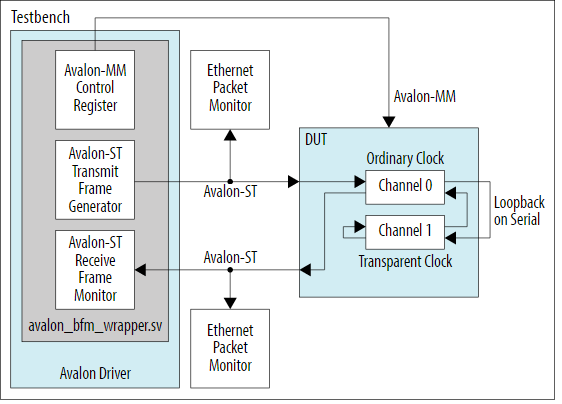
**Figure 3. Reset Scheme**

****

# **Simulation**

**Testbench**

**Figure 4. Block Diagram of Testbench**



**Table 2. Testbench components**

|  |  |
| --- | --- |
| **Component** | **Description** |
| Device Under Test (DUT) | Components of the design example |
| Avalon Driver | Consists of Avalon-ST master bus functional models (BFMs). This driver forms the Avalon-ST TX & RX paths and also provides access to the Avalon-MM interface of DUT |
| Ethernet Packet Monitors | Monitor TX & RX paths and display the monitored frames in simulator console |

**Using the Simulator**

Follow the steps below to simulate the design example using ModelSim simulator:

1. Download and restore the example design files from Design Store.
2. Ensure that the **QUARTUS\_ROOTDIR** environment variable points to the Quartus installation path.
3. Launch the Quartus Prime Pro edition software and open the project file (**top.qpf**).
4. Before running the design compilation, go to **Assignments > Settings.** Under **IP Settings** category, tick the checkbox for “**Generate IP simulation when generating IP**”.
5. Compile the design by clicking **Processing > Start Compilation**.
6. Launch the **ModelSim** simulator.
7. Change the working directory to *<project\_directory>/simulation/ed\_sim/mentor.*
8. Run the following command to set up the required libraries, compile the functional simulation model, and exercise the simulation model with the provided testbench:

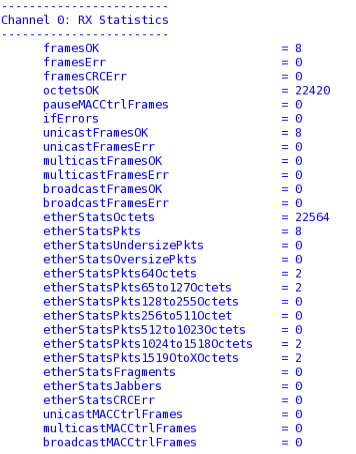
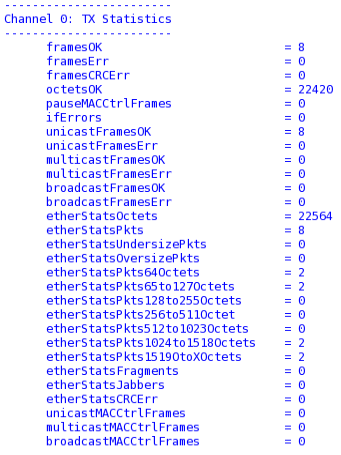
**do tb\_run.tcl**

**Simulation Test Case**

The simulation test case will perform the following steps:

1. Starts up the example design with an operating speed of 2.5G.
2. Configures the MAC, PHY and FIFO buffer for channel 0 and channel 1.
3. Sends the following packets:
   * 55 bytes packet
   * 100 bytes packet
   * 1518 bytes packet
   * 9600 bytes packet (Jumbo packet)
4. Repeats steps 2 to 4 for 1G speed mode.
5. At the end of simulation, MAC statistic counters will be displayed in the transcript window. The transcript window also will show simulation PASSED if the RX Avalon-ST received all packets successfully, no error in MAC statistics counters and the RX MAC statistics counters equal to the TX MAC statistics counters.

**Figure 5. Sample Simulation Output**



# **Hardware Testing**

**Test Case – External Loopback Test**

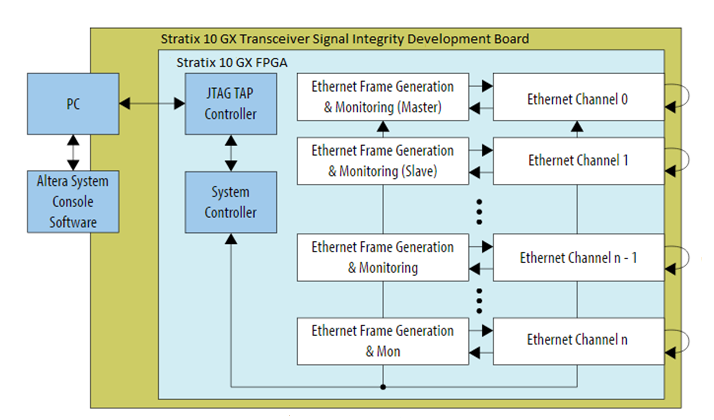
Follow the steps below to compile and test the design in the supported Intel development kit:

1. Download and restore the example design files from Design Store.
2. Launch the Quartus Prime Pro edition software and open the project file (**top.qpf**).
3. Compile the design by clicking **Processing > Start Compilation**.
4. After the design is compiled successfully, a programming file(**top.sof**) will be generated and located in the *project\_directory/output\_files* directory.
5. Set up the development board with the following steps:
   1. Attach SFP optical transceiver module with optical fiber loopback cable on channel 0 or channel 1.
   2. Connect the programming cable to the JTAG connection port (J14)
   3. Connect the power adaptor to the power supply input (J107)
6. In the Intel Quartus Prime software, select **Tools > Programmer** to launch the programmer.
7. Launch the Clock Control tool **(stratix10GX\_1sg280uf50\_si\_revc\_ltile\_V17.1b240v1.1\examples\board\_test\_system\ClockController.exe)** and change the frequency of Y1 to 125 MHz. (Refer to Figure 7 on page 11)
8. Download the generated programming file (**altera\_eth\_top.sof**) to the development board using the **Programmer** application.
9. Reset the system by pressing the PB0 push button.

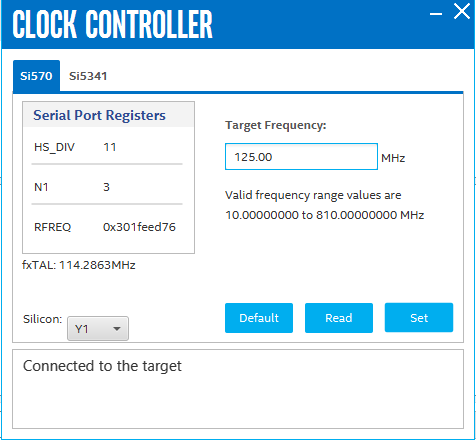
*Note: The design must be reset whenever you begin a new test.*

1. In the Quartus Prime Pro edition software, launch the System Console (**Tools > System Debugging Tools > System Console**).
2. In the System Console command shell, change the working directory to *<project\_directory>\hwtesting \system\_console*.
3. Initialize the design command list by running the following command:  
   **source main.tcl**
4. Run the following command in the system console to start the external loopback test.   
   **TEST\_EXT\_LB <channel> <speed> <burst\_size>**  
   *Example: TEST\_EXT\_LB 0 1G 100000000  
   Note: For more information about of the command parameters, please refer to* ***Test Commands*** *topic**on page 16.*
5. As shown in figure 7, figure 8 and figure 9, test results will be displayed at the end of the test which shows that the packet monitor block receives the same number of packets generated without error and the TX and RX statistics counters have the same number of packets transmitted/received without error.

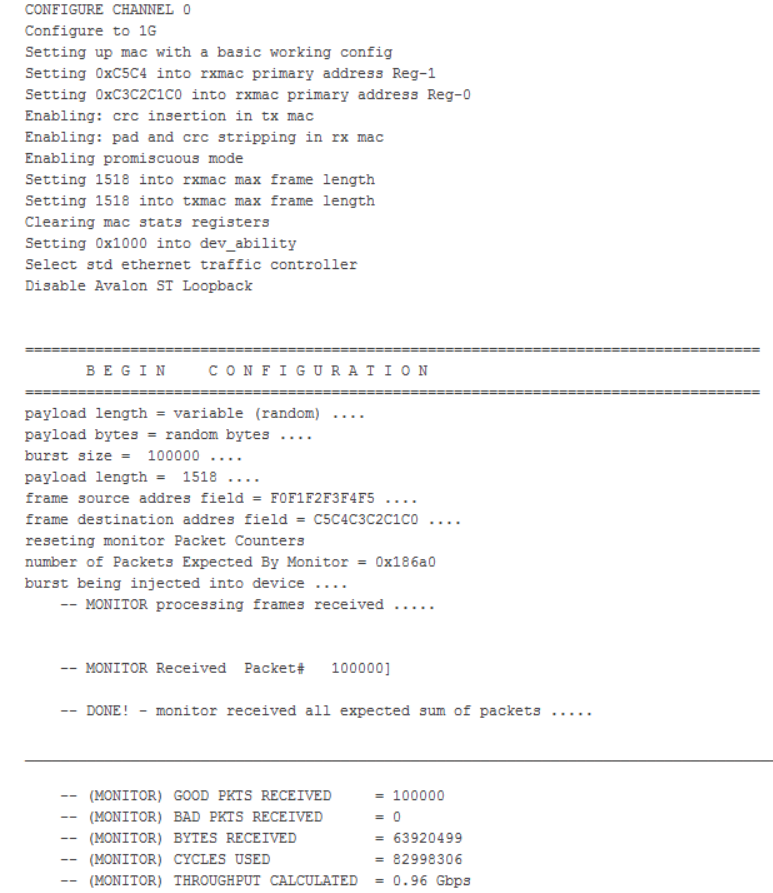
**Figure 6. Hardware Setup for External Loopback Test**



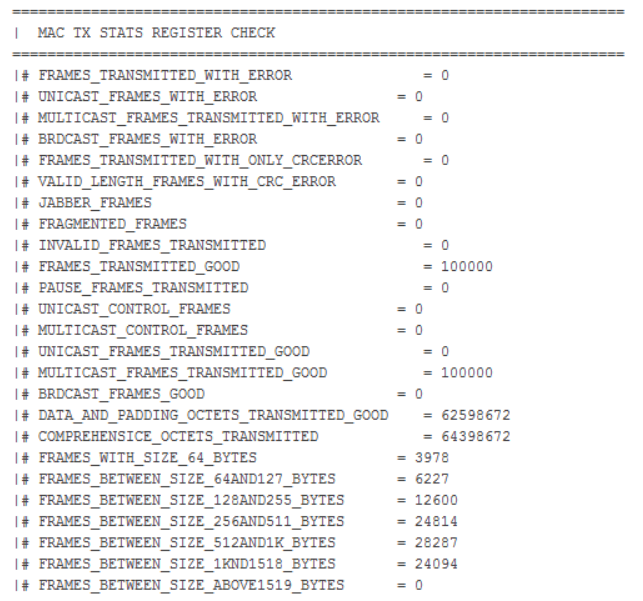
**Figure 7. Configuration of Y1 Frequency in Clock Controller**



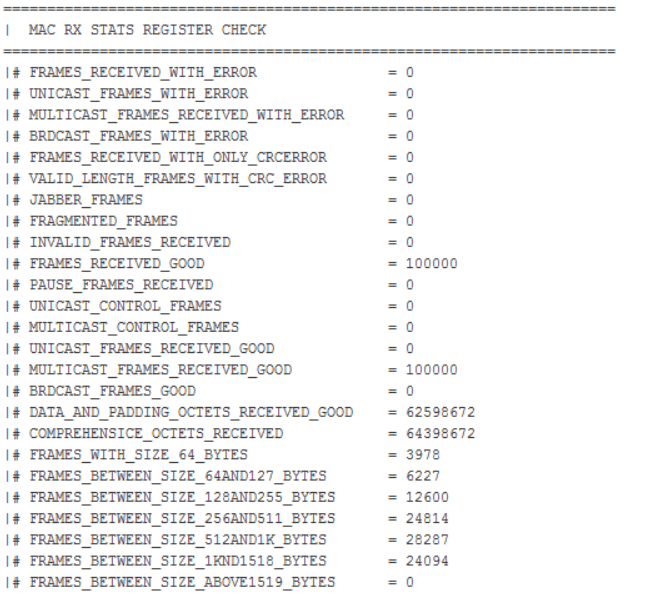
**Figure 8. Sample Output – Packet Monitor**



**Figure 9. Sample Output – TX Statistic Counter**



**Figure 10. Sample Output – RX Statistic Counter**

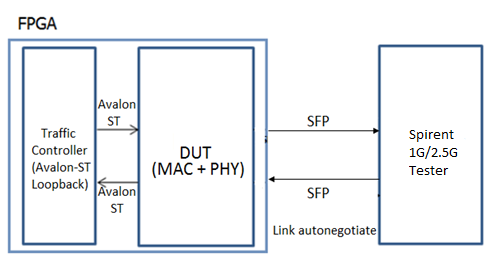


**Test Case – Avalon-ST RX-TX Loopback Test With External Tester**

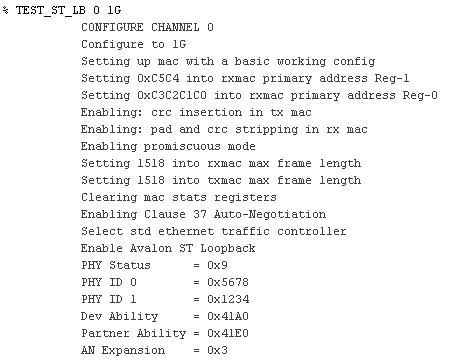
Follow the steps below to compile and test the design in the supported Intel development kit:

1. Download and restore the example design files from Design Store.
2. Launch the Quartus Prime Pro edition software and open the project file (**top.qpf**).
3. Compile the design by clicking **Processing > Start Compilation**.
4. After the design is compiled successfully, a programming file(**top.sof**) will be generated and located in the *project\_directory/output\_files* directory.
5. Set up the development board with the following steps:
   1. Attach SFP optical transceiver module to channel 0 or channel 1 and connect this module to an external tester through optical fiber cable.
   2. Connect the programming cable to the JTAG connection port (J14).
   3. Connect the power adaptor to the power supply input (J107).
6. In the Intel Quartus Prime software, select **Tools > Programmer** to launch the programmer.
7. Launch the Clock Control tool **(stratix10GX\_1sg280uf50\_si\_revc\_ltile\_V17.1b240v1.1\examples\board\_test\_system\ClockController.exe)** and change the frequency of Y1 to 125 MHz.
8. Download the generated programming file (**altera\_eth\_top.sof**) to the development board using the **Programmer** application.
9. Reset the system by pressing the PB0 push button.
10. *Note: The design must be reset whenever you begin a new test.*
11. In the Quartus Prime Pro edition software, launch the System Console (**Tools > System Debugging Tools > System Console**).
12. In the System Console command shell, change the working directory to *<project\_directory>\hwtesting \system\_console*.
13. Initialize the design command list by running the following command:  
    **source main.tcl**
14. Run the following command in the system console to configure the low latency 10G MAC and Multi-rate PHY and start the Avalon-ST loopback test.  
    **TEST\_ST\_LB <channel> <speed>**   
    *Example: TEST\_ST\_LB 0 1G  
    Note: For more information about of the command parameters, please refer to* ***Test Commands*** *topic**on page 16.*
15. Start transmitting the Ethernet packets from the external packet tester to the SI development board and verify the number of packets that successfully loopback to the external packet tester.
16. Run the following command to view the transmitter (TX) and receiver (RX) MAC statistic counters.  
    **CHKMAC\_TXSTATS  
    CHKMAC\_RXSTATS**

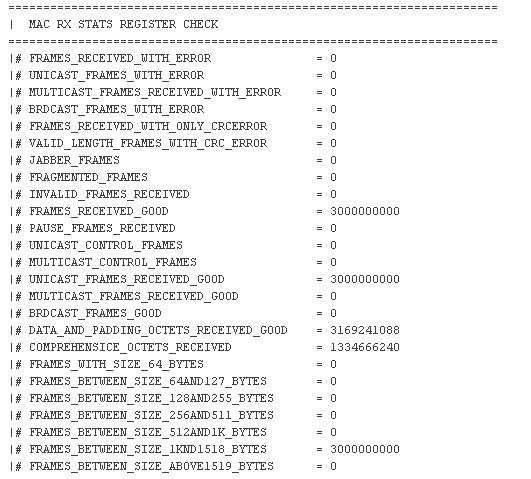
**Figure 11. Hardware Setup for Avalon-ST RX-TX Loopback Test**



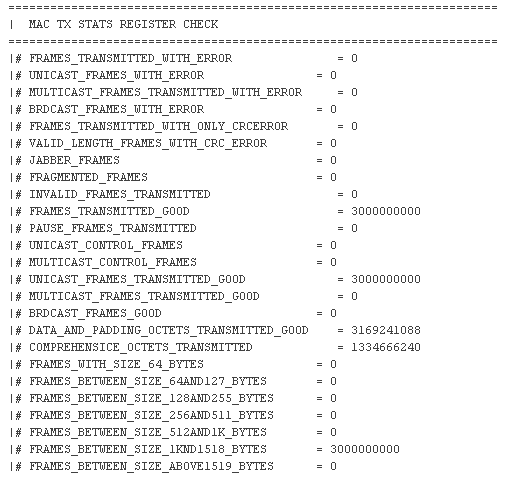
**Figure 12. Sample Output – MAC and PHY Configurations Summary**



**Figure 13. Sample Output – TX Statistic Counter**



**Figure 14. Sample Output – RX Statistic Counter**



# **Test Commands**

This design example provides various TCL commands to test the Stratix 10 1G/2.5G Multi-rate Ethernet design in different loopback modes.

**Table 3. Command Parameters for External Loopback Test**

Format for the TCL command test is **TEST\_EXT\_LB <channel> <speed> <burst\_size>**

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Valid Values** | **Description** |
| channel | 0, 1 | Channel number to be tested |
| speed | 1G, 2.5G | PHY speed mode |
| burst\_size | An integer value | Number of packets to be generated for the test |

**Table 4. Command Parameters for Avalon-ST Loopback Test**

Format for the TCL command test is **TEST\_ST\_LB <channel> <speed>**

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Valid Values** | **Description** |
| channel | 0, 1 | Channel number to be tested |
| speed | 1G, 2.5G | PHY speed mode |

# **Configuration Registers**

Users can access the 32 bits configuration registers of the design components through Avalon-MM interface.

**Table 5. System Register Map**

|  |  |
| --- | --- |
| **Base Address** | **Block** |
| 0x000000 | Transceiver Reconfiguration Block |
| 0x100000 | Traffic Controller |
| 0x010000 | MAC – Channel 0 |
| 0x018000 | PHY – Channel 0 |
| 0x01A000 | Native PHY Reconfiguration – Channel 0 |
| 0x020000 | MAC – Channel 1 |
| 0x028000 | PHY – Channel 1 |
| 0x02A000 | Native PHY Reconfiguration – Channel 1 |
| 0x004000 | Reserved |

# **Transceiver Reconfiguration**

**Table 6. Transceiver Reconfiguration Register Map**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Word Offset | Name | Bits | Description | Access | HW reset Value |
| 0x00 | logical\_channel\_ number | [9:0] | The logical number of the reconfiguration block. | RW | 0x000 |
| [31:10] | Reserved | - | - |
| 0x01 | control | [1:0] | Specify the new operating speed:   * 00: 1 Gbps * 01: 2.5Gbps * 10: Reserved * 11: 10Gbps | RW | 0x00 |
| [15:2] | Reserved | - | 0x000 |
| [16] | Writing 1 to this bit when it is 0 to start the reconfiguration process. The bit clears itself when the process it completed. | RW | 0x00 |
| [31:17] | Reserved | - | 0x000000 |
| 0x02 | status | [0] | When this bit is set to 1, indicates the reconfiguration process is in progress. | RO | 0x00 |
| [31:1] | Reserved | - | - |

# **Related Links**

1. Stratix 10 GX Transceiver Signal Integrity Development Kit Downloadable Content

* <https://www.altera.com/products/boards_and_kits/dev-kits/altera/kit-s10-transceiver-si.html>
* Download the Stratix 10 GX SI L-tile Package (ES Edition)

1. Intel FPGA Low Latency Ethernet 10G MAC User Guide

* <https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/ug/ug_32b_10g_ethernet_mac.pdf>
* Contain the MAC registers’ settings and definitions

1. Intel Stratix 10 1G/2.5G/5G/10G Multi-rate Ethernet PHY IP Core User Guide
   * <https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/ug/ug-s10-mre-phy.pdf>
   * Contain the PHY registers’ settings and definitions
2. Intel FPGA Low Latency Ethernet 10G MAC Design Example User Guide for Intel Stratix 10 Devices
   * <https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/ug/ug-20073.pdf>
   * Describe the interface signals and configuration registers that related to this design (Section 7 and Section 8)