

Simple PWM(Pulse Width Modulation) Using MAX 10 FPGA Evaluation Kit

©2014 Altera Corporation. All rights reserved. ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS and STRATIX words and logos are trademarks of Altera Corporation and registered in the U.S. Patent and Trademark Office and in other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders as described at www.altera.com/common/legal.html. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

This design example demonstrates the working of a simple PWM using the Max 10 Evaluation Kit. The brightness of an LED is used to demonstrate this feature. Instead of varying an analog voltage to the LED, the width of a pulse with voltage rails at 0 and 2.5V can be used to vary the intensity of the LED brightness by supplying the LED with a pulse width modulated signal.

Working of the Design:

This Design example takes the input from the user using two Keys and displays the corresponding count value and the PWM output on the LED's.

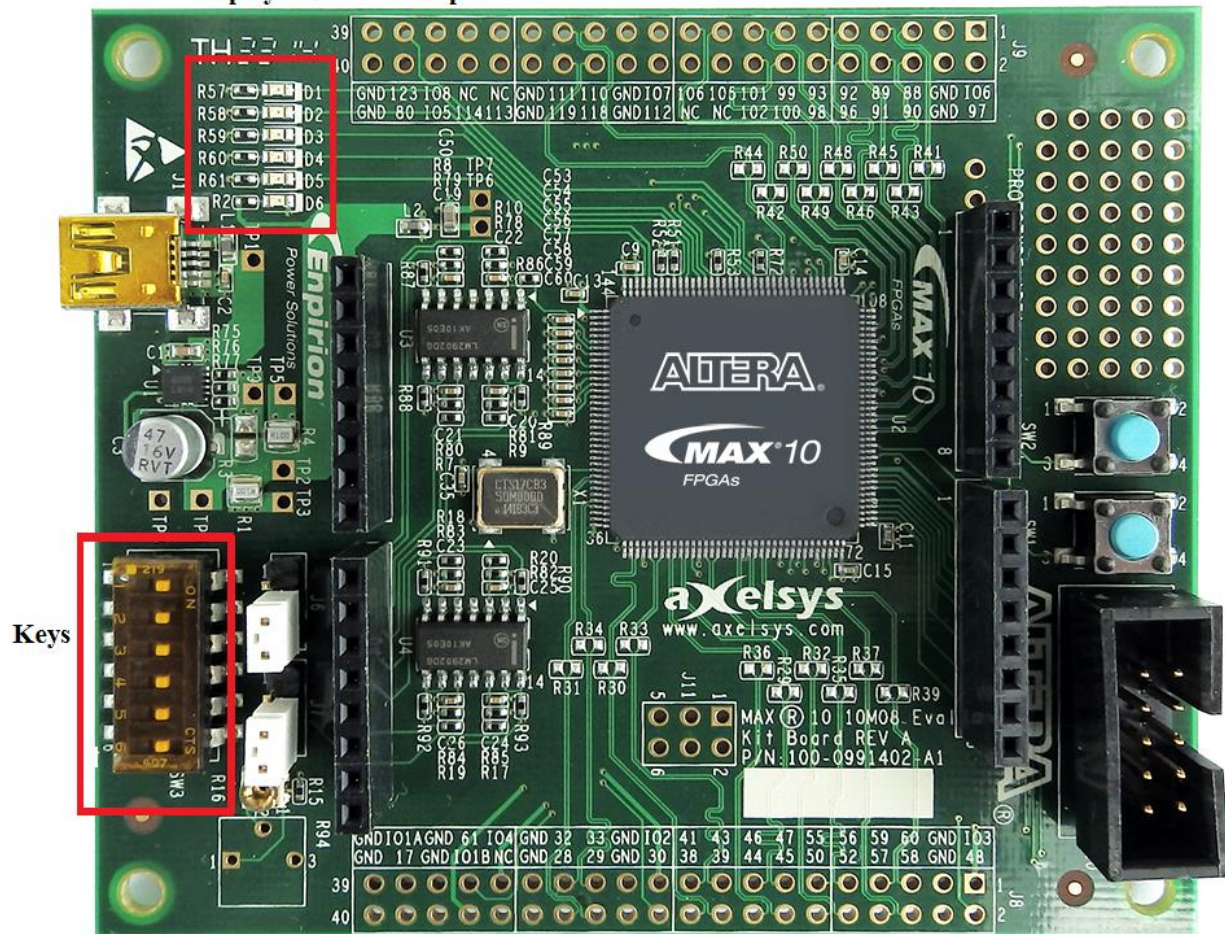
The two Keys, Key1 and Key2 are the inputs for the design. Key1 corresponds to incrementing the value of the counter and Key2 corresponds to decrementing the value of the counter.

The outputs are 5 LEDs from LED1- LED5 (D1 to D5 on the board). LED5 displays the brightness(the PWM output) and LED 1-4 display the count value.

Initially all the LEDs are off indicating a count value of 0. The user can start by pressing the up or down key. Pushing the up Key once will cause the count value to increment by 1 and hence the LED1 will glow and LED 2- 4 are off. (Binary representation 0001 is displayed with LED4 being the MSB and LED1 being the LSB). The LED5 is dimly lit for this count. The user can keep pushing the 1st Key and correspondingly see the count on the LEDs incrementing from 0 - 15. As the count reaches its maximum value the LED5 is brightly lit.

The user can try a variety of combinations of the up and down Keys and verify the count increment /decrement and the LED5 being brightly/dimly lit accordingly.

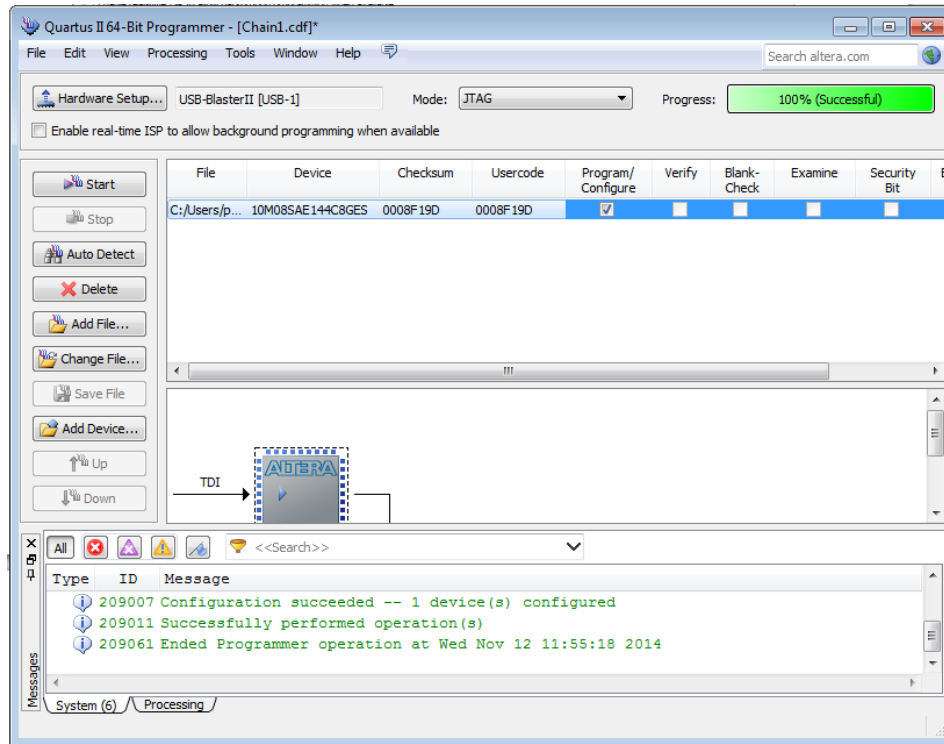
LED's D1 to D4 display the count and D5 displays the PWM output



The Steps to run the simple PWM design on the MAX 10 Evaluation kit are:

1. Download the pwm_led_eval.par from the design store.
2. Use command `quartus_sh --platform_install -package <directory-path>/pwm_led_eval.par`
3. Once the process completes use the command:
use the command:
`"quartus_sh --platform -name pwm_led_eval"`
to obtain all the files in the pwm_led .qar. All the files will be unarchived and stored.
Use the command "quartus top" to launch quartus and open the project.
4. Compile the design.
5. To program the eval kit go to:
 - i) Go to Tools→Programmer.
 - ii) Click on Hardware Setup. A hardware Setup dialog box will open.
 - iii) Select USB Blaster under currently selected hardware. Click on close.
 - iv) Use the Add file tab to navigate to the master/images folder and select the top.sof file.

- v) Select the checkbox Program/Configure and Verify.
- vi) Click on start. This starts the downloading of the .sof file on to the Eval Kit.

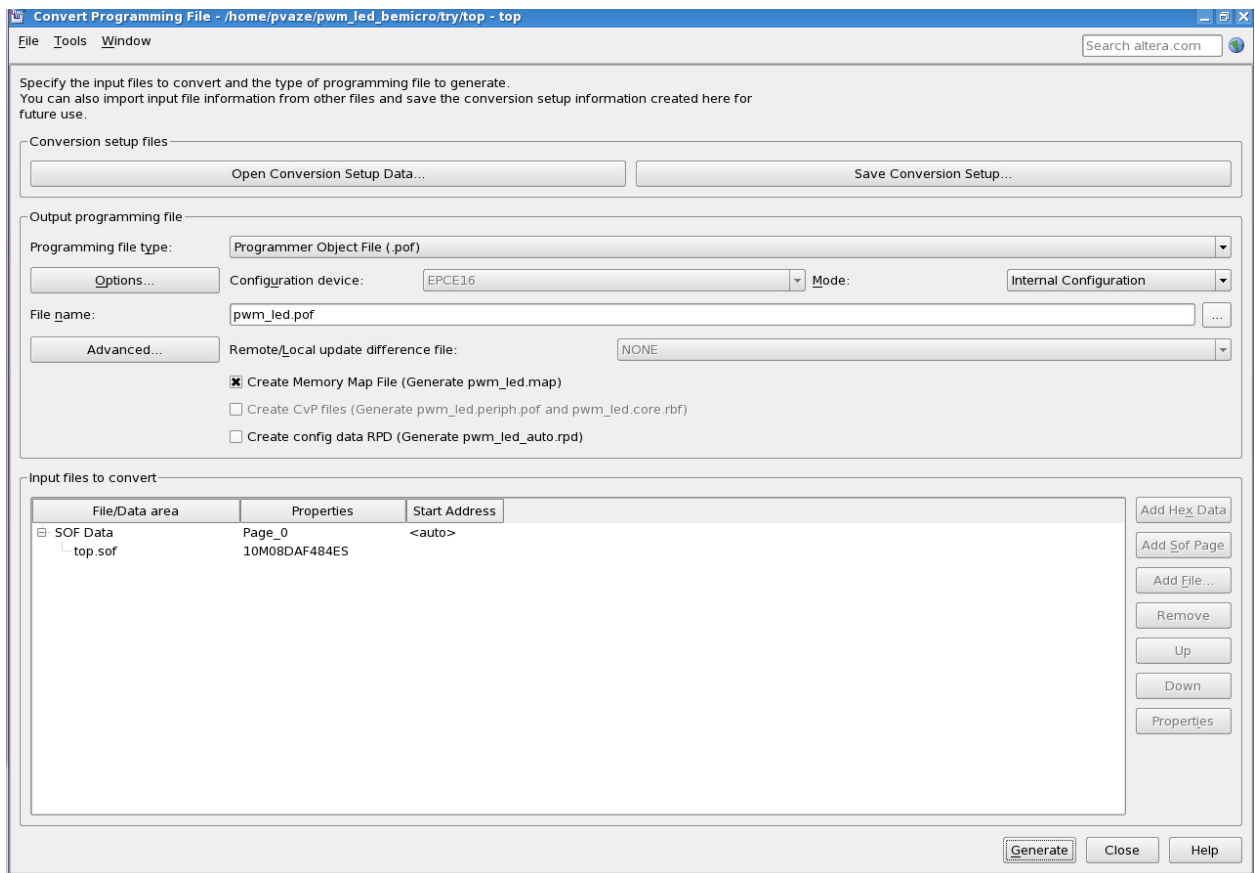


6. Once the top.sof file is downloaded to the kit, the user can try several inputs and test the design.

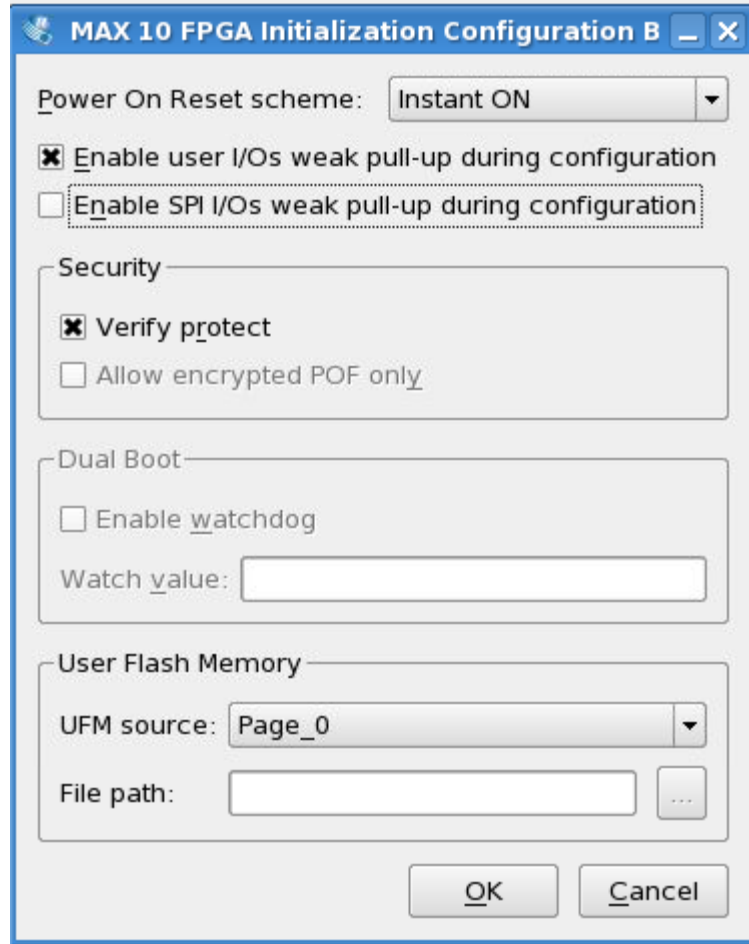
The two most common formats for downloading the image into the MAX10 FPGA is the .sof and .pof files. The .sof file gets downloaded directly in the FPGA configuration SRAM and will lose contents upon power cycling. The .pof file is loaded into the configuration flash memory and will be stored in the MAX 10 FPGA and preserved during a power cycle.

To generate the .pof file for the design follow the below steps:

- 1) On the File menu, click Convert Programming Files.
- 2) Under Output programming file, select Programmer Object File (.pof) in the Programming file type list.



- 3) In the Mode list, select Internal Configuration.
- 4) To set the ICB settings, click Options button. An ICB setting dialog box will appear.



Set the following in the ICB setting dialog box:

Power on Reset Scheme: Instant On

Check - Enable user IOs week pull up during configuration check box.

Check - Enable the JTAG Security check box.

Check - Verify Protect check box.

In this example, No Watchdog is used, since the configuration reverts once the Watchdog times out.

NOTE: It is always recommended to enable the Watch Dog Timer.

Click OK.

- 5) In the Convert Programming File window(previous image) specify the file name for the programming file you want to generate.
- 6) Click Generate to create the file.

Acknowledgment

This design is based on [Simple PWM Tutorial](#) for Be Micro MAX 10 FPGA Evaluation Kit produced by Arrow Electronics.

Document Revision History

Date	Version	Changes
November 2014	2014.11.13	Initial Release