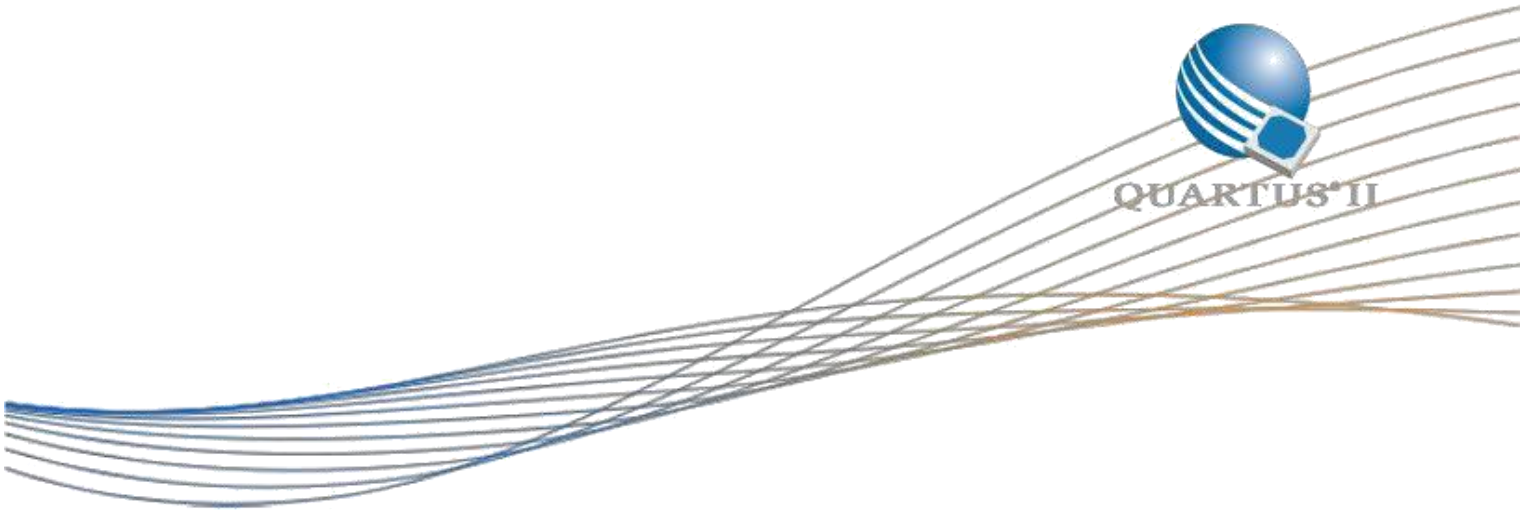

Board Update Portal based on NIOS II Processor Using the MAX 10 FPGA Development Kit

Revision history

Version	Author	Date	Changes	Reason
1.0	Martin Chen	6/1/2015	Initial release	

Table of Contents

Overview

This example design is a web-server based board update portal (BUP) design which contains a Nios® II processor, a Triple Speed Ethernet media access control (MAC) MegaCore® and a DDR3 MegaCore®. It allows you to remotely update a FPGA system over Ethernet, for an example, it can be used to update the firmware of an embedded FPGA system. The design is based on Ethernet A port on MAX 10 FPGA development kit, please download and install the BTS installer for more details about BUP design.

The following external parts are needed to demonstrate the design example:

1. MAX10 10M50DA FPGA Development kit
2. Mini-USB cable for programming MAX 10 device
3. Quartus v15.0 or later
   - Recompile the design example
   - Recompile the software build
   - Use NIOS command shell to download SOF and ELF file and get IP address info
   - Quartus v15.0.0/145 or later is required for this design example. Please refer to the Altera Download Center for information on updates
4. **IMPORTANT**: only use the 12V, 2A AC adapter that came with this kit. Do not use other power supplies from other Altera kits

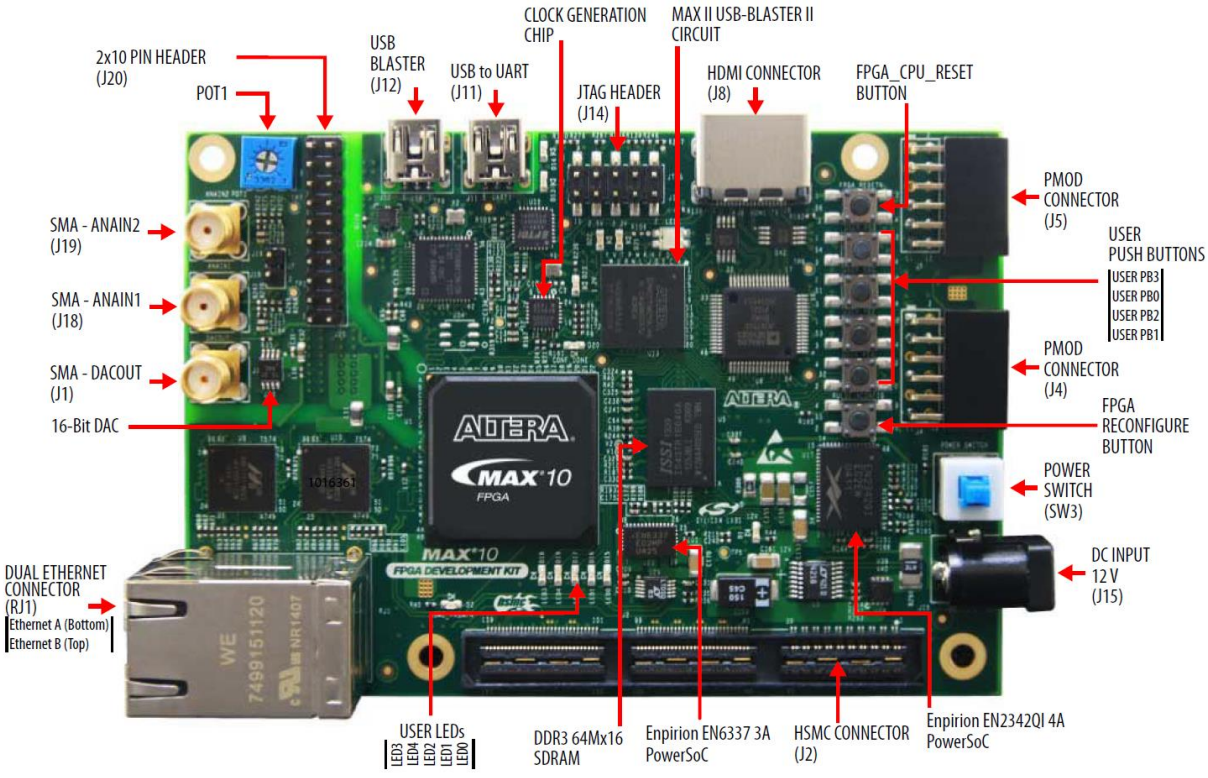

Figure 1: Max10 FPGA Development Kit

Theory of Operation

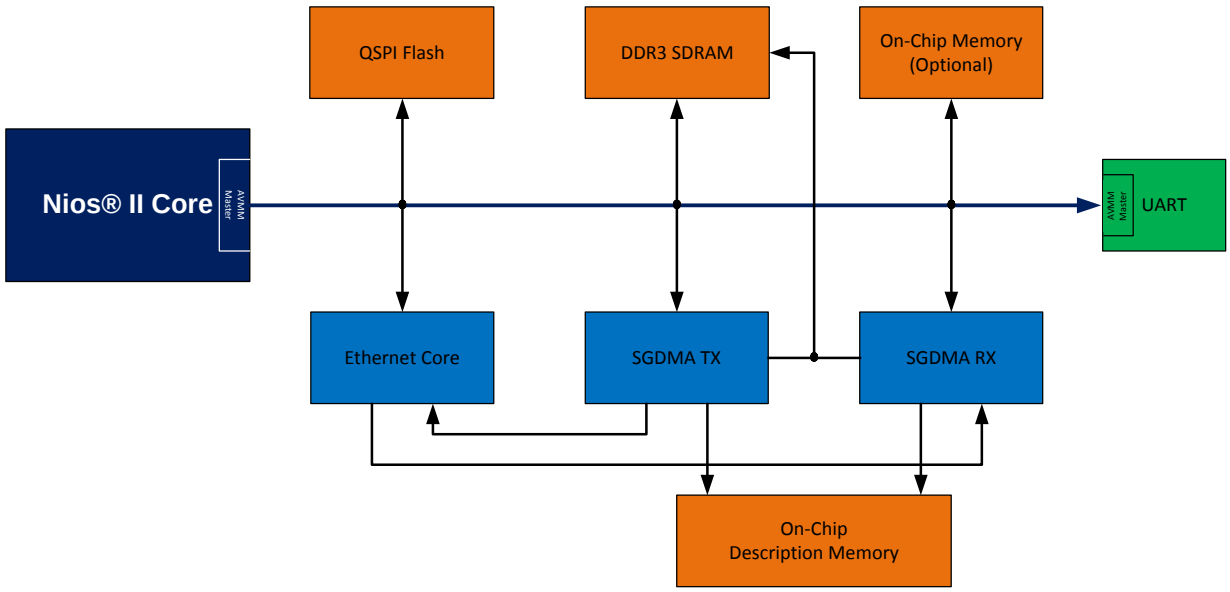

Figure 2: BUP design example block diagram

The Nios® II processor is used to implement a web server in MAX 10 FPGA device. Please see application note AN429: Remote Configuration Over Ethernet with the Nios® II Processor (PDF) to learn more about remote update. Also, more information about Embedded Peripheral IP can be found at IP Peripheral User Guide.

Simple Demo Setup

1. Connect the power cord to the power plug of the kit
2. Connect a mini USB from your PC/laptop to the J12 USB connector (labeled as USB 1 on the silkscreen) on the top left of the kit
3. Connect Ethernet cable to Ethernet port A (the bottom one)

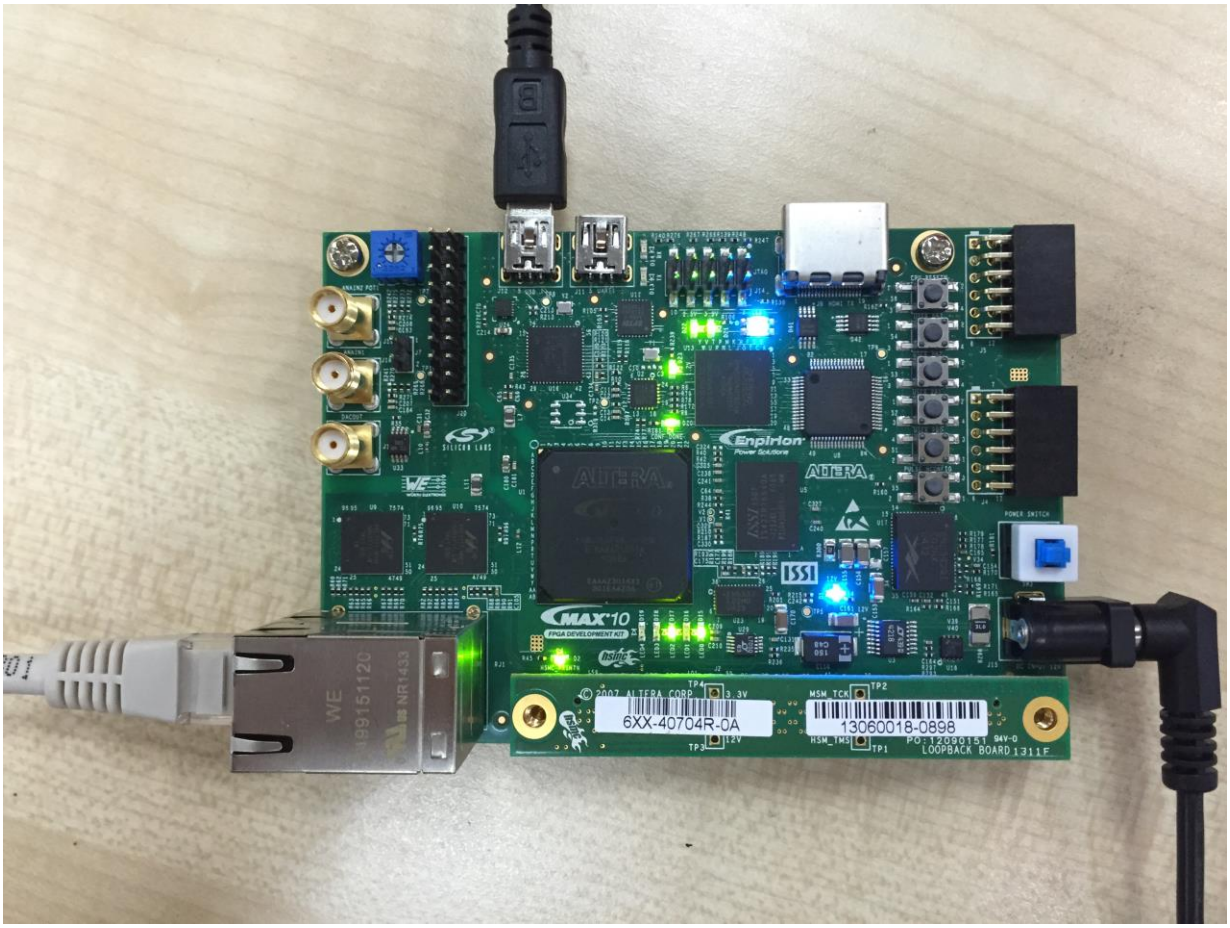

Figure 3: BUP test platform

4. Open NIOS command shell and change to project root directory
5. Type "**nios2-configure-sof --cable 1 --device 1 master_image/m10_rgmii.sof;sleep 5;nios2-download -g –r software_examples/factory_image/web_server.elf;nios2-terminal;**"
6. Check whether it gets corresponding IP address as expected

```
nios2-terminal: connected to hardware target using JTAG UART on cable
nios2-terminal: "USB-BlasterII [USB-1]", device 1, instance 0
nios2-terminal: (Use the IDE stop button or Ctrl-C to terminate)

InterNiche Portable TCP/IP, v3.1

Copyright 1996-2008 by InterNiche Technologies. All rights reserved.
prep_tse_mac 0

Your Ethernet MAC address is 00:07:ed:2a:02:3a
prepped 1 interface, initializing...
[tse_mac_init]
INFO    : TSE MAC 0 found at address 0x00201000
INFO    : PHY Marvell 88E1111 found at PHY address 0x00 of MAC Group[0]
INFO    : PHY[0.0] - Automatically mapped to tse_mac_device[0]
INFO    : PHY[0.0] - Restart Auto-Negotiation, checking PHY link...
INFO    : PHY[0.0] - Auto-Negotiation PASSED
MARVELL : Mode changed to RGMII/Modified MII to Copper mode
MARVELL : Enable RGMII Timing Control
MARVELL : PHY reset
INFO    : PHY Marvell 88E1111 found at PHY address 0x01 of MAC Group[0]
WARNING : PHY[0.X] - Mapping of PHY to MAC failed! Make sure the PHY address is defined correctly in tse_mac_device[] structure
WARNING : MAC Group[0] - Number of PHY connected is not equal to the number of channel, Number of PHY : 2, Channel : 1
INFO    : PHY[0.0] - Checking link...
INFO    : PHY[0.0] - Link not yet established, restart auto-negotiation...
INFO    : PHY[0.0] - Restart Auto-Negotiation, checking PHY link...
INFO    : PHY[0.0] - Auto-Negotiation PASSED
INFO    : PHY[0.0] - Link established
INFO    : PHY[0.0] - Speed = 100, Duplex = Full
OK, x=0, CMD_CONFIG=0x00000000

MAC post-initialization: CMD_CONFIG=0x04000203
[tse_sgdma_read_init] RX descriptor chain desc (1 depth) created
mctest init called
IP address of et1 : 0.0.0.0
Created "Inet main" task (Prio: 2)
Created "clock tick" task (Prio: 3)
Acquired IP address via DHCP client for interface: et1
IP address : 192.168.1.100
Subnet Mask: 255.255.255.0
Gateway    : 192.168.1.1


nios2-terminal: exiting due to ^D on remote
```

Figure 4: Link establishment and IP address acquirement

How to recompile the hardware build

Please follow the steps on the Design Store web page to extract and install the m10_rgmii platform file. The following steps describe how to setup a project in Quartus II software in order to configure the MAX10 FPGA device with the m10_rgmii (BUP) demo design.

1. Launch Quartus II software and open the project top.qpf using **File->Open Project**
2. Compile the project by clicking the  button
3. Launch the Quartus II programmer from the Tools menu or alternatively by clicking the  button
4. Download the .sof file output_files/top.sof and program the device using the programmer as previously described

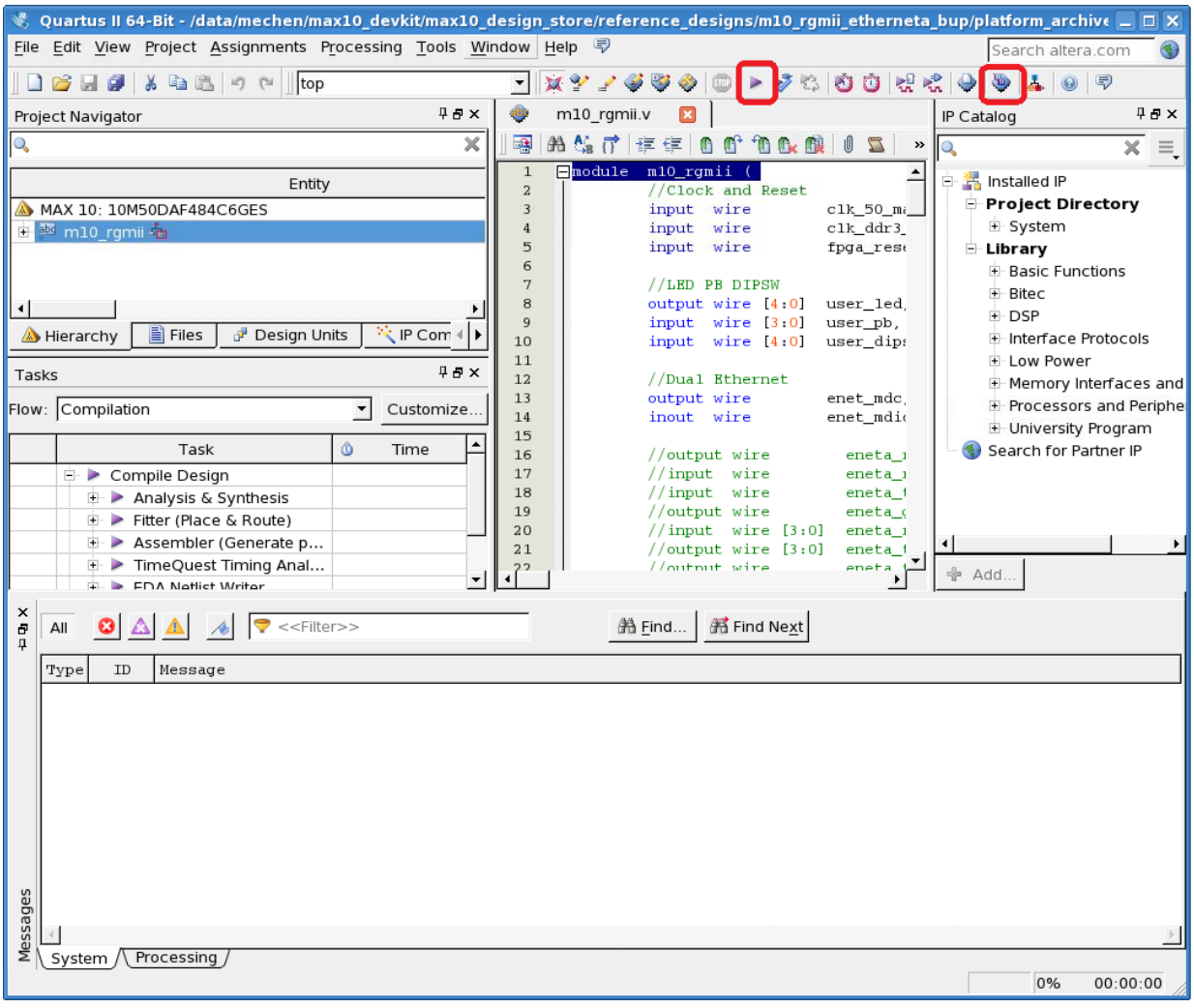

Figure 5: Link establishment and IP address acquirement

Convert SOF file to POF file

Please follow the steps on how to convert SOF file to POF file for MAX 10 FPGA internal configuration solution. For dual configuration feature, please turn to the "Selecting the Internal Configuration Scheme" section of the User Guide for more details.

1. Launch Quartus II software and open the **Convert Programming File tool**
2. Select **Internal Configuration mode**
3. Add Sof Page
4. Add file
5. Generate POF file for output_files/top.sof

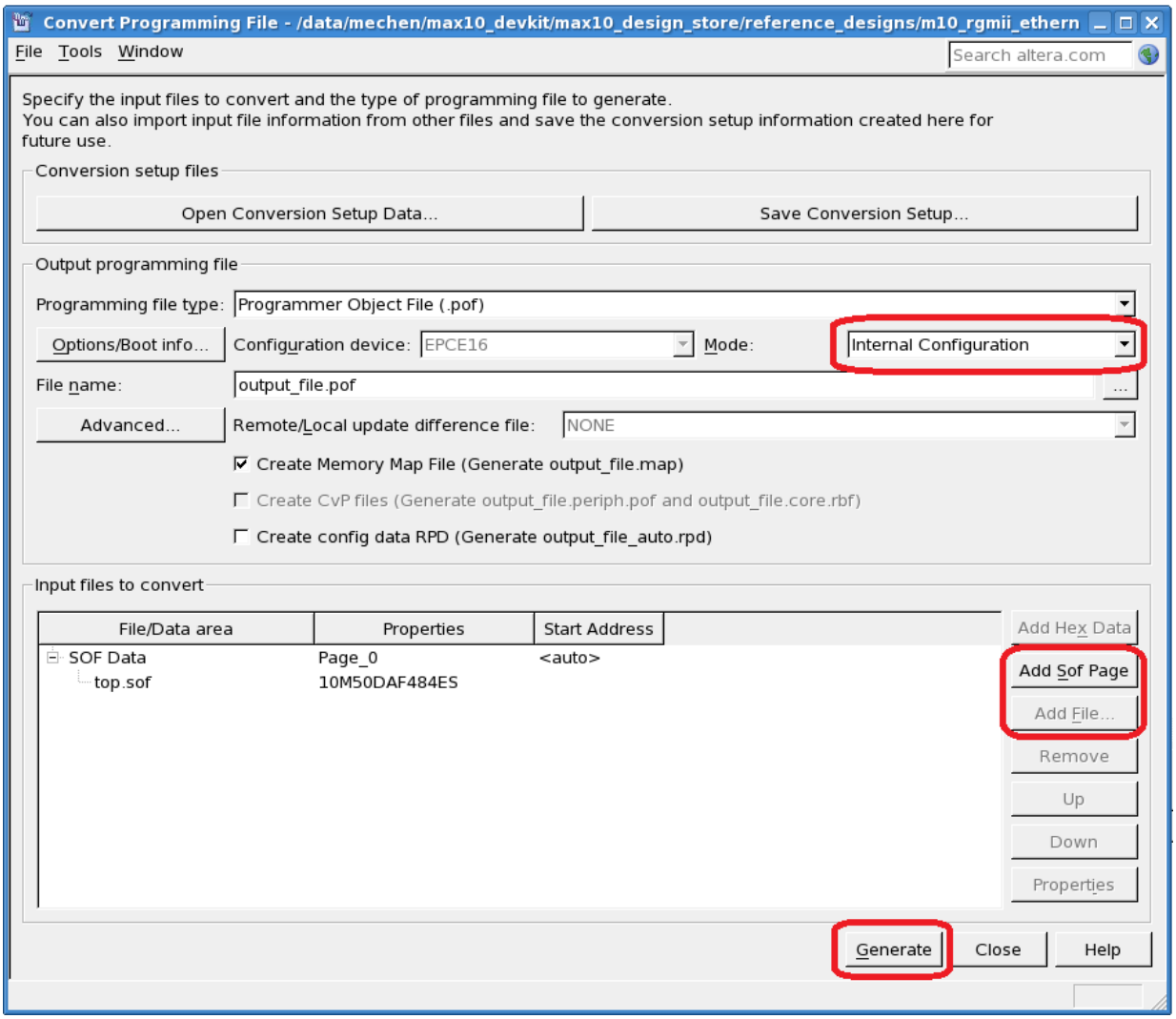

Figure 6: Link establishment and IP address acquirement

How to recompile the software build

Please follow the steps on how to recompile the software build under different conditions.

1. **Compile the software build without any modifications**
   a) Open NIOS command shell (v15.0.0/145 or later) and change to the directory: <BUP Root Directory> \software_examples\app
   b) Type in the command "**./create-this-app**"
   c) The compilation will take you a few minutes (it depends on your PC performance), and generate an output file named web_server.elf

2. **Recompile the software build with some modifications of BSP file**
   a) Open NIOS command shell (v15.0.0/145 or later) and change to the BSP directory: <BUP Root Directory> \software_examples\bsp
   b) Type in the command "**make**"
   c) Change to the directory <BUP Root Directory> \software_examples\app after BSP recompilation
   d) Type in the command "**make**"
   e) The compilation will take you a few minutes (it depends on your PC performance), and generate an output file named web_server.elf

3. **Recompile the software build with some modifications of APP files**
   a) Open NIOS command shell (v15.0.0/145 or later) and change to the directory <BUP Root Directory> \software_examples\app
   b) Type in the command "**make**"
   c) The compilation will take you a few minutes (it depends on your PC performance), and generate an output file named web_server.elf

Convert NIOS executable file to .flash file

You should convert executable file to .flash file so that you can program it into QSPI flash with BUP build, you should use the elf2flash utility to create the flash image:

1. Open NIOS command shell (v15.0.0/145 or later)
2. Type in the command "**elf2flash --base=0x24000000 --end=0x27FFFFFF --reset=0x24430000 --input=[ELF_FILE_LOCATION] --output=[FLASH_FILE] --boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_loader_cfi.srec**"

Note:

1) Base offset address and end offset address are the QSPI flash addresses assigned in the BUP Qsys component
2) Reset offset address stand for Flash memory base address (0x2400_0000) + Reset Vector Offset (0x0043_0000)
3) Reset Vector Offset address (0x4300_0000) is assigned to factory software block by default, please refer the User Guide for more info about flash memory mapping

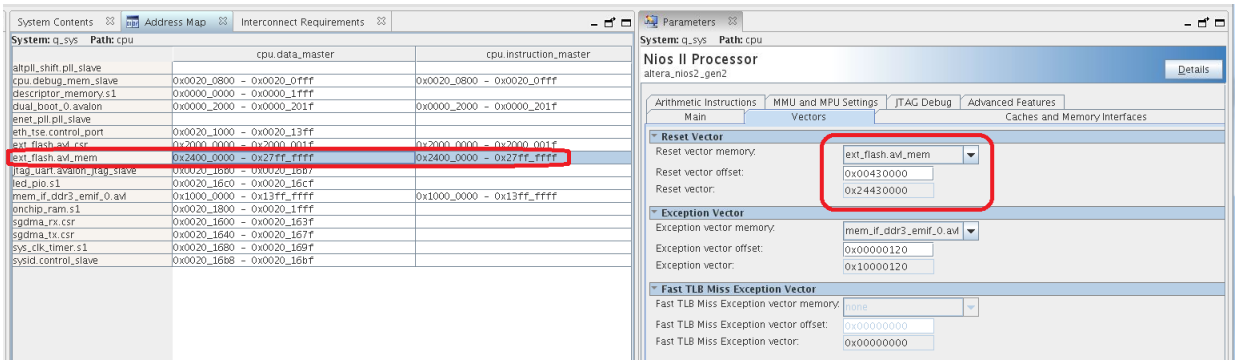

Figure 7: BUP Qsys component offset address info

Program images into On-chip CFM flash and external QSPI flash

The following steps describe how to program FPGA image into MAX 10 FPGA On-chip CFM flash for internal configuration and software image(s) into on-board QSPI flash.

How to program the factory images into MAX 10 FPGA device and Quad SPI flash:

1. Program *\software_examples\factory_images\dual_boot_image.pof into Configuration Flash Memory (CFMs) via programmer
2. Change SW2 switch 2 to the ON position (0)
3. Make sure Ethernet cable is connected to port A (the bottom one)
4. Power cycle the board or push S5 button to boot up from BUP build (BUP A)
5. Open NIOS command shell at *\altera\15.0\nios2eds\, e.g. double click "Nios II Command Shell.bat"
6. Change directory to *\software_examples\factory_images\
7. Type "**nios2-download --cable n* --device 1 -g -r ./web_server.elf; nios2-terminal;**"
8. Check whether it gets corresponding IP address
9. Launch IE and type the IP address got from step #g in the address bar (e.g. http://192.168.1.100, Change Proxy Server setting if needed)
10. If it turns out be the MAX 10 FPGA development kit Webpage, please click the bottom-right "Factory Restore" link to restore factory build, otherwise, it should be the raw page for factory build programming

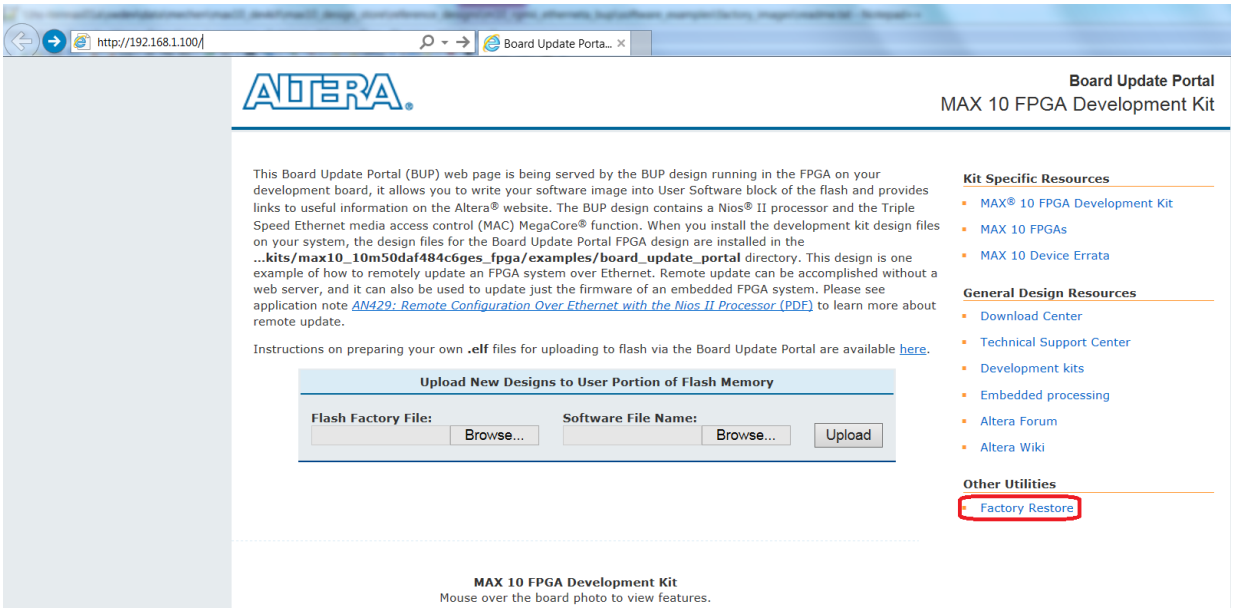

Figure 8: MAX 10 FPGA development kit Webpage

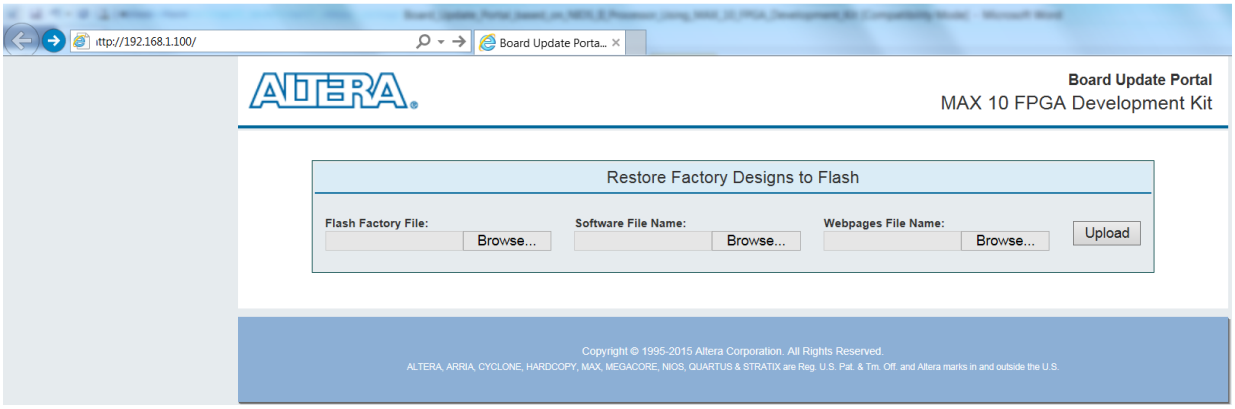

Figure 9: Factory build restoration page

11. Load "*\software_examples\factory_images\m10_fpga_html.zip" in "Webpages File Name" column and "*\software_examples\factory_images\ext_flash.flash" in "Software File Name" column and then upload them

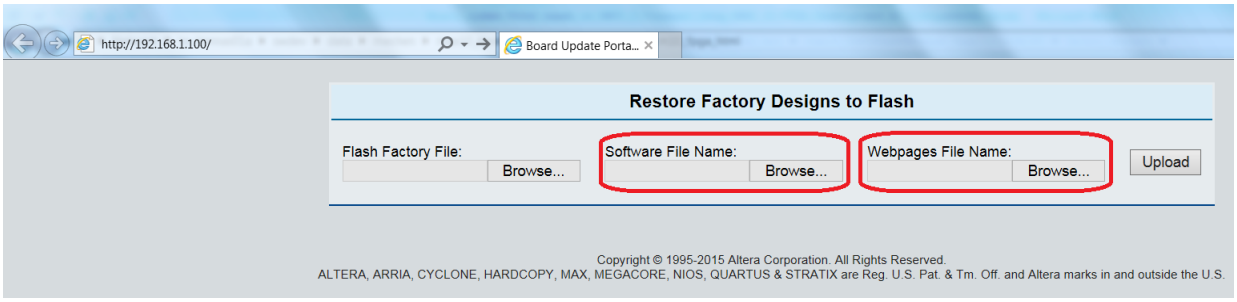

Figure 10: Raw page for factory recovery

12. Check whether it uploads successfully or not
13. Power cycle the board again
14. Type "nios2-terminal;" in NIOS command shell again to check whether it can get IP address as expected
15. Launch IE and type its IP address in the address bar to see whether the webpage is working or not

Note:

1) n* stands for USB cable number, e.g. "cable 1"
2) Dual-boot images:
   - Dual compressed image #0: BUP A build
   - Dual compressed image #1: GPIO (bts_config) build which is also available on Design Store
   - Please turn to the "Selecting the Internal Configuration Scheme" section of the User Guide for Dual Configuration feature
3) Ethernet Port A is used by the factory BUP build by default