

Arria 10 JESD204B AD9144-AD9625 Interoperability Reference Design User Guide

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Overview

This reference design is targeted on Arria 10 GX FPGA Development Kit. It showcases Altera JESD204B IP core interoperates with Analog Devices Inc. AD9144 digital-to-analog converter (DAC) and AD9625 analog-to-digital converter (ADC). The FPGA generates the sine wave using the Altera NCO IP core and transmits the data to the DAC through the JESD204B link. When the JESD204B link is established, you can view the 2.4576MHz sine wave by connecting a SMA cable from the oscilloscope to one of the four analog output channels SMA on the AD9144 evaluation module (EVM). The AD9625 interface is not hardware tested yet and is currently disabled in the NIOS II software; this interface will be tested once the AD9625 EVM is available before the future release of this reference design. You can use this design as a reference for your design with Altera JESD204B IP core to interoperate Arria 10 with AD9625.

Theory of Operation

The architecture of this reference design is derived from the AN729: Implementing JESD204B IP Core System Reference Design with NIOS II Processor as Control Unit. The link to the application note is

- https://www.altera.com/en_US/pdfs/literature/an/an729.pdf

Enhancements are made to the reference design in AN729. The following key features are available in this reference design for the TX interface:

- A simplex TX IP core with Native PHY standard PCS interoperates with AD9144 at FMC port A at 9.8304Gbps. The JESD204B parameters of this interface are L=8, M=4, F=1, S=1, N=N'=16, K=32, HD=1, SCR=1, CS=CF=0. The ATX PLL drives the bonded PMA through the master CGB.
- Dedicated device clock for TX IP core link layer is sourced from on-board clock generator X3. This 245.76MHz reference clock is used for the IO PLL; OUTCLK0 produces 245.76MHz link clock for the link layer, transport layer and is exported to the CLKOUT SMA. The AD9516 clock generator on the AD9144 evaluation module (EVM) sources the reference clock from this CLKOUT through a SMA cable; OUTCLK1 produces 245.76MHz frame clock for the transport layer and user logic such as the pattern generator.
- A dedicated ATX PLL reference clock at 245.76MHz is supplied from the AD9516 clock generator on the AD9144 EVM through FMC port A. This clock generator also supplies 245.76MHz device clock to the DAC. The internal DAC PLL generates 983.04MHz sampling clock for the analog channels. The AD9516 operates in clock distribution mode; the on-chip PLL is bypassed.
- The SYSREF pulses for FPGA and DAC are generated by the AD9516 clock generator.
- The TX transport layer (assembler) and pattern generator are integrated into QSYS inside the jesd204b_subsystem_0 along with the JESD204B TX IP core.
- SPI programming sequences for AD9516 clock generator and AD9144 DAC are coded in main.c in the NIOS II SW project.

- A DAC status monitoring subroutine is coded in main.c in the NIOS II SW project.

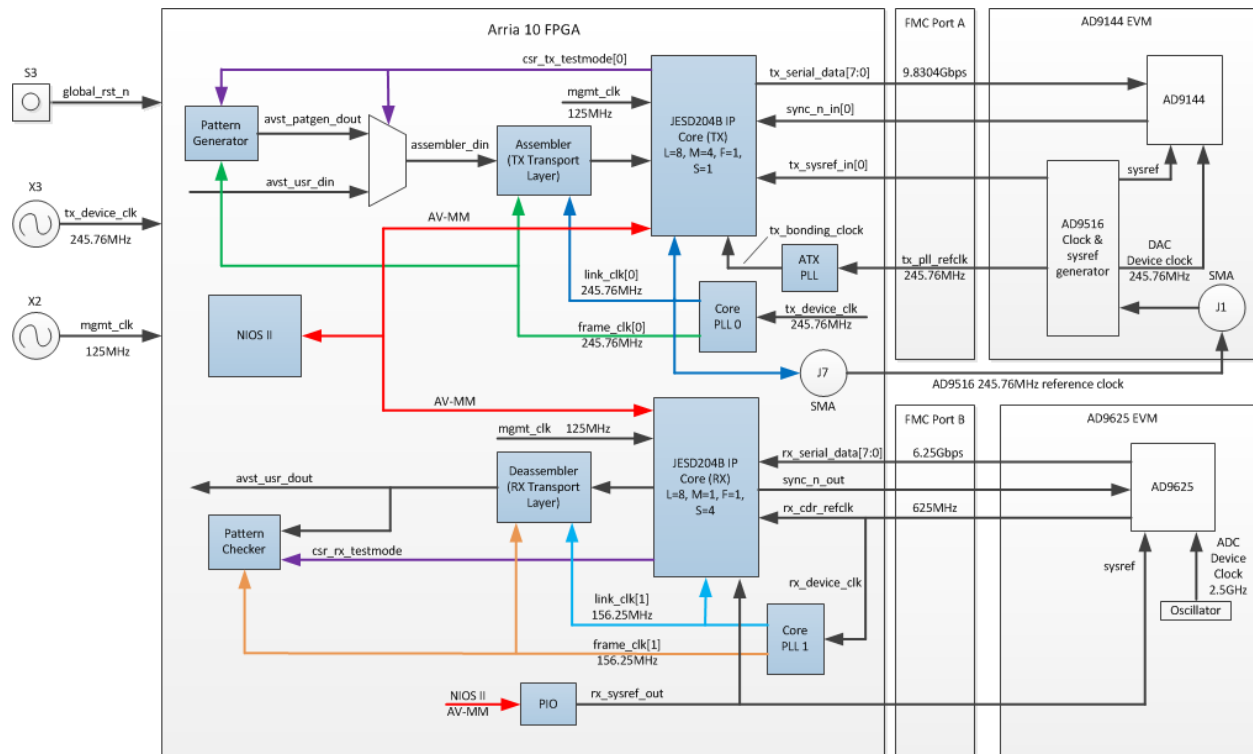
The following key features are available in this reference design for the RX interface:

- A simplex RX IP core with Native PHY standard PCS interoperates with AD9625 at FMC port B at 6.25Gbps. The JESD204B parameters of this interface are L=8, M=1, F=1, S=4, N=12, N'=16, K=32, HD=1, SCR=1, CS=CF=0.
- The AD9625 generates 625MHz device clock and CDR reference clock for the RX IP core. This clock is transmitted through the FMC port B to the dedicated transceiver reference clock pins. The AD9625 EVM has an on-chip 2.5GHz oscillator which provides device clock for the AD9625.
- The FPGA generates SYSREF pulse for the RX IP core as well as the AD9625.
- A 3-wire to 4-wire SPI conversion circuit that has the Altera GPIO Megafunction is instantiated. This circuit controls the SPI data direction of the bidirectional IO buffer.
- The RX transport layer (de-assembler) and pattern checker are integrated into QSYS inside the jesd204b_subsystem_1 along with the JESD204B RX IP core.
- SPI programming sequence for AD9625 ADC is coded in main.c in the NIOS II SW project.

The following key features are common to both TX and RX interfaces:

- An enhanced NIOS II SW project that supports that supports multi-link design with different TX and RX JESD204B parameters.
- Top level Verilog `define directive can be used to enable/disable logic generation for TX and RX interfaces independently.
- PHY debug features such as transceiver dynamic reconfiguration, Altera Debug Master Endpoint, Capability Registers, Control and Status Registers and PRBS Soft Accumulators are enabled.
- A SignalTap II file is included for further debug assistance. Optionally, you can enable the SignalTap II in the Quartus II project setting and recompile the design.
- Frequency checkers are instantiated to report the operating frequencies of the on-board programmable oscillator X3 (tx_device_clk), AD9516 clock generator on AD9144 EVM (tx_pll_refclk) and AD9625 DIVCLK pins (rx_cdr_refclk).

Figure 1: Reference Design Simplified Block Diagram



Software Requirements

In order to run the reference design, the following software is needed at your PC:

- Altera Complete Design Suite (ACDS). Refer to the version indicated at the Quartus II version field of this reference design in the Design Store.
- Altera Arria 10 GX FPGA Development Kit Installer

The Clock Control GUI which is part of the FPGA development kit installer is used to configure the X3 on-board VCXO clock frequency. You can download the kit installer from

https://www.altera.com/products/boards_and_kits/dev-kits/altera/kit-a10-gx-fpga.html

Hardware Setup

In order to run the reference design, you need to the following hardware:

- Arria 10 GX FPGA Development Kit
- AD9144-FMC-EBZ evaluation module
- AD-FMCADC2-EBZ evaluation module ⁽¹⁾
- 1x SMA cable
- Micro-USB cable ⁽²⁾
- Development kit power adaptor (2)

The following hardware is optional:

- 1x SMA cable
- Low bandwidth oscilloscope (500MHz)

Note:

- (1) The AD9625 evaluation module is not needed if you want to run the TX-only interface with AD9144 DAC.
- (2) The micro-USB cable and power adaptor are part of the development kit accessories.

Before you power up the FPGA development kit, perform the following actions to operate the TX only interface with AD9144 DAC:

- Apply a jumper at pin 5-6 of J11 to set the FMC port A adjustable voltage to 1.8V. Refer to Figure 2 for the jumper setting.
- Apply a jumper at pin 5-6 of XP1 programming header on the AD9144 EVM to disable the XU1 micro-controller on the EVM.
- Short the JP3 pads on the AD9144 EVM to enable the U10 voltage translator for the SPI interface.
- Install the AD9144 EVM at the FMC port A (left) of the FPGA development kit. This EVM derives power from FPGA development kit, so no power adaptor for the EVM is needed.
- Connect the SMA cable between J7 CLKOUT SMA on the FPGA development kit and J1 SMA on the AD9144 EVM to transmit the 245.76MHz clock from the IO PLL to AD9516 clock generator reference clock input.

Perform the following actions to operate the TX and RX interfaces with AD9144 DAC and AD9625 ADC in addition to the actions above:

- Apply a jumper at pin 5-6 of J8 to set the FMC port B adjustable voltage to 1.8V. Refer to Figure 2 for the jumper setting.
- We recommend you to remove the R379 termination resistor on the FPGA development kit because this termination resistor couples the SCLK pulses to SDIO data pin at the SPI interface to AD9625 EVM.
- Install the AD9625 EVM at the FMC port B (right) of the FPGA development kit.

Note that the current revision of the reference design has disabled the RX interface in the NIOS II software. This interface will be enabled in the future release when the RX interface is validated with AD9625 EVM.

Figure 3 shows the complete hardware setup for TX-only interface operation with AD9144 EVM. Figure 4 shows the complete hardware setup for TX and RX interfaces operation with AD9144 and AD9625 EVM. The RX-only interface operation is not supported in the NIOS II software project.

After you have performed the setup as indicated above, connect the micro-USB cable to your PC and power up the FPGA development kit. Before you load the design to the FPGA,

configure the X3 VCXO on the FPGA development kit to output 245.76MHz clock using the Clock Control GUI. In the Clock Control GUI Si570 (X3) tab, enter 245.76 at the **Target Frequency** text box and click the **Set** button as shown in the Figure 5.

Figure 2: FMC port A and B adjustable voltage jumper settings

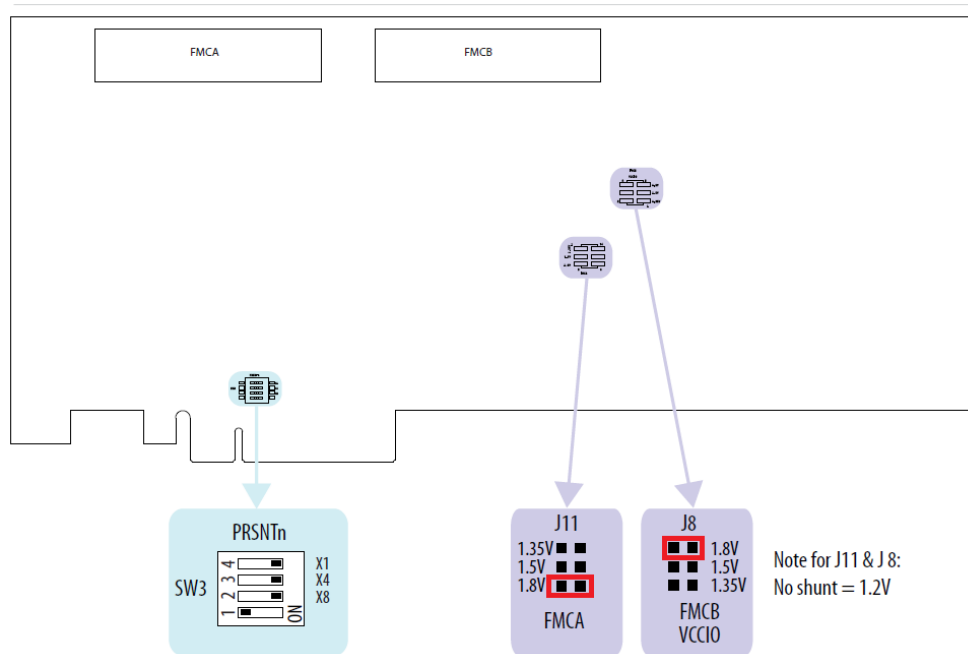


Figure 3: Hardware setup for TX-only operation with AD9144 EVM

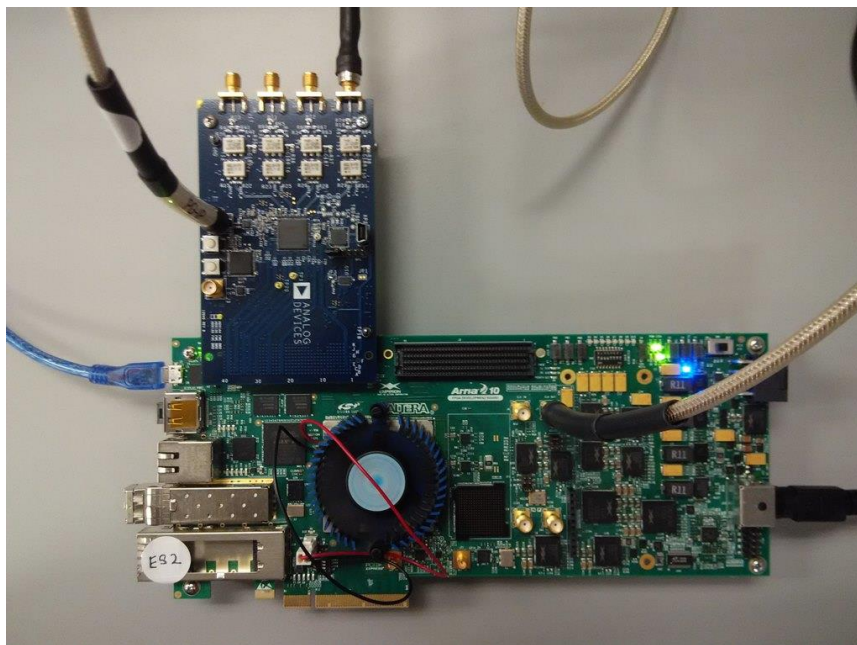


Figure 4: Hardware setup for TX and RX operation with AD9144 and AD9625 EVM

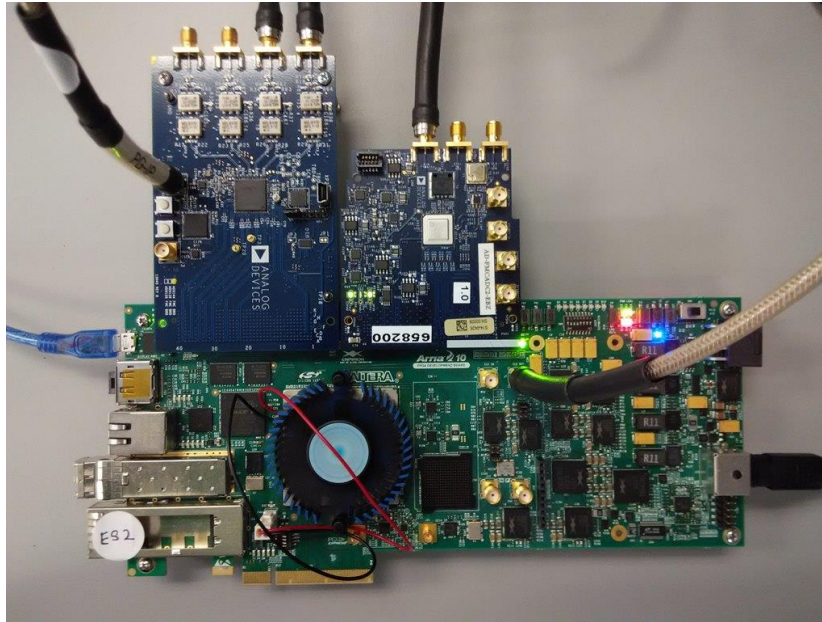
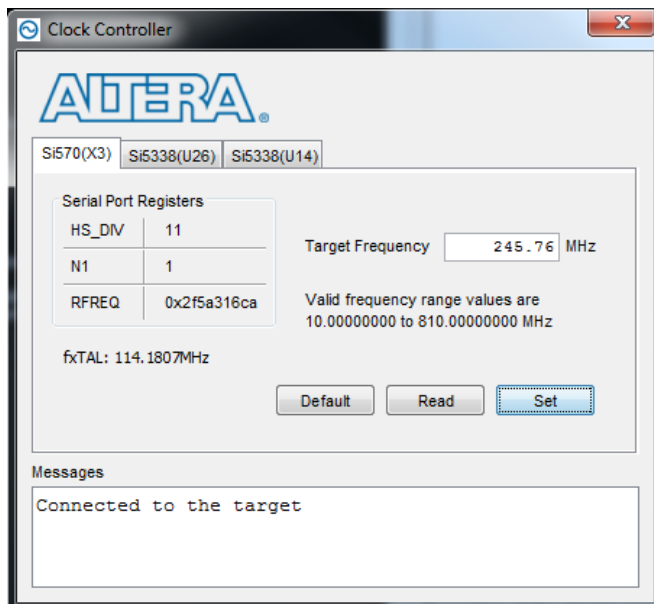


Figure 5: X3 clock source setup



Quick Start Guide

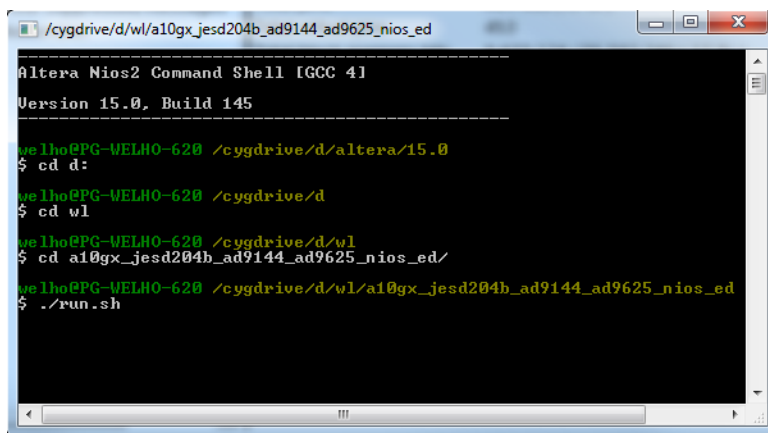
Follow the following steps to run the reference design:

- Extract the reference design to your PC.
- Launch the NIOS II command shell. Navigate to the reference design project folder.
- Type `./run.sh` at the command prompt. Refer to Figure 6.

Note: If you have more than 1 JTAG cable attached to your PC (i.e. more than one Altera development kit), identify the targeted Arria 10 FPGA development kit by typing **jtagconfig** at the Windows command prompt. The JTAG cable number is identified in **[USB-<JTAG cable number>]** as shown in Figure 7. Type **./run.sh <JTAG cable number>** at the NIOS II command shell.

- If you have an oscilloscope, connect a SMA cable from any analog output channel at the AD9144 EVM to the oscilloscope input channel. Observe the sine waveform as shown in Figure 8.
- Observed the message printed at the NIOS II command shell. Refer to Figure 9.

Figure 6: Run the reference design from NIOS II command shell



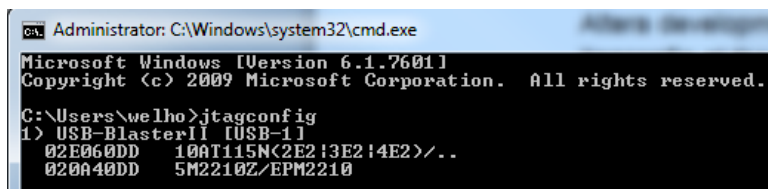
```

/cygdrive/d/wl/a10gx_jesd204b_ad9144_ad9625_nios_ed
Altera Nios2 Command Shell IGCC 41
Version 15.0. Build 145

welho@PG-WELHO-620 /cygdrive/d/altera/15.0
$ cd d:
welho@PG-WELHO-620 /cygdrive/d
$ cd wl
welho@PG-WELHO-620 /cygdrive/d/wl
$ cd a10gx_jesd204b_ad9144_ad9625_nios_ed/
welho@PG-WELHO-620 /cygdrive/d/wl/a10gx_jesd204b_ad9144_ad9625_nios_ed
$ ./run.sh

```

Figure 7: Identify JTAG cable number from Windows command prompt



```

Administrator: C:\Windows\system32\cmd.exe
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

C:\Users\welho>jtagconfig
1) USB-BlasterII [USB-1]
   02E060DD 10A1115N<2E213E214E2>/..
   020A40DD 5M2210Z/EPM2210

```

The **run.sh** shell script loads the SOF and ELF images into the FPGA. Once the ELF images are loaded, the NIOS II terminal displays the tasks performed by the NIOS II to bring up the JESD204B link:

- Configure the AD9516 clock generator on the AD9144 EVM through the SPI interface to output the targeted clock and SYSREF frequencies for the AD9144 DAC and TX IP core. Refer to the Theory of Operation for details.
- After the correct ATX PLL reference clock is received, the transceiver user calibration is performed for the ATX PLL and each TX channel.
- Assert reset sequence for the transceiver and IP core according to the sequence defined in the Altera reset sequencer IP in jesd204b_subsystem_0 QSYS.
- Configure the TX IP core csr_test_mode register so that the pattern generator outputs sine wave test pattern to AD9144

- Configure AD9144 DAC through the SPI interface
- Once the DAC is configured, the DAC initializes the JESD204B link by de-asserting the sync_n signal. This action transitions the link from code group synchronization phase (CGS) to initial lane alignment sequence phase (ILAS). The TX IP core transmits the JESD204B link parameters in the second ILAS multi-frame. These parameters are captured by the DAC. After 4 multi-frames are being transmitted, the DAC performs lane alignment. If alignment is achieved and there is no link error detected by the DAC, the sine wave test pattern data is converted to analog waveform and output through the DAC analog channels.
- After 10 seconds of data streaming, the TX link status is checked by reading the TX IP core status 0 register.
- Various DAC registers are read to check the RX link status through the SPI interface. These include reading the IRQ register (address 0x47A), the JESD204B configuration mismatch error register (address 0x47B) and the JESD204 parameters capture register (address 0x030).

After the link is up and running, the JESD204B prompt is displayed to acquire user input. Refer to AN729 for a list of commands supported by the NIOS II software. This reference design doesn't support dynamic reconfiguration.

Known issues:

- The ACDS 15.0 NIOS II terminal doesn't accept user input. This problem is scheduled to be fixed in the future release of the ACDS software.

Figure 8: Observing sine wave at oscilloscope

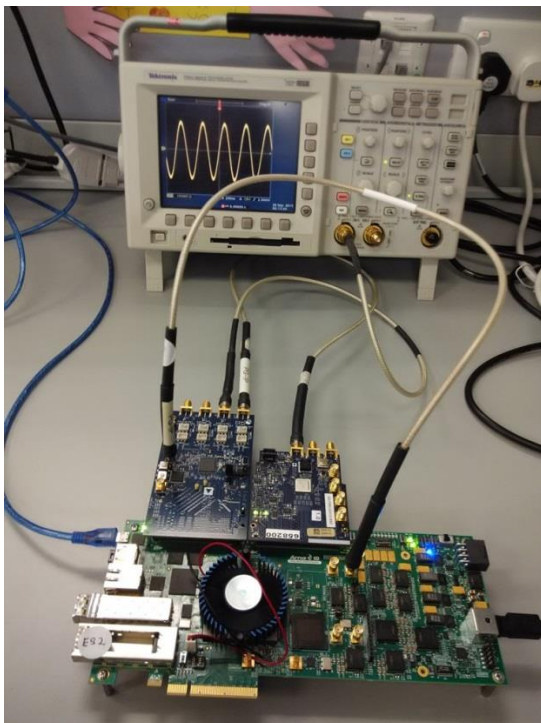


Figure 9: Messages printed at the NIOS II command shell

The screenshot shows a NIOS II command shell window with the following messages and callouts:

- Configure AD9516:** Points to the message "Configuring external clock generator..."
- Transceiver user calibration:** Points to the messages "Reset transceiver, link and frame for link 0 ...", "Perform transceiver user calibration for link 0 ...", and the list of TX termination and VOD calibration passes for channels 0 through 7.
- Assert reset sequence:** Points to the message "Calibrate ATX PLL..."
- Configure IP core:** Points to the message "Asserting complete reset sequencing for each link..."
- Configure AD9144:** Points to the messages "DAC PLL is locked", "SERDES PLL is locked", "SERDES PLL calibration is successful", "SERDES PLL operates correctly", and "LMFC SYNC machine has properly locked".
- Link initialization and data streaming:** Points to the messages "Pulse sysref...", "Wait for 10 seconds...", "Reporting link status...", and "TX status 0 register for link 0: 0x00000005".
- Check TX IP core status:** Points to the message "Initialization successful!"
- Check DAC status:** Points to the "Polling DAC status ..." section, which includes a list of error checks (No bad disparity error, No not in table error, No unexpected control character error, No initial lane sync error, No bad checksum error, No frame sync error, No code group sync error) and a list of received DAC parameters (L, M, F, S, K, N, N', HD, SCR, CS, CF, checksum).

The terminal output ends with the prompt: "Please enter command at the prompt: [Press 'q' to exit terminal or 'h' for menu of available commands] JESD204B>"

Design Regeneration

The reference design needs to be regenerated if you modify the design. One scenario where the design is modified and regenerated is when the data rate is changed, for example to 10Gbps. Perform the following steps to modify and re-generate the design in Quartus II software to operate at 10Gbps:

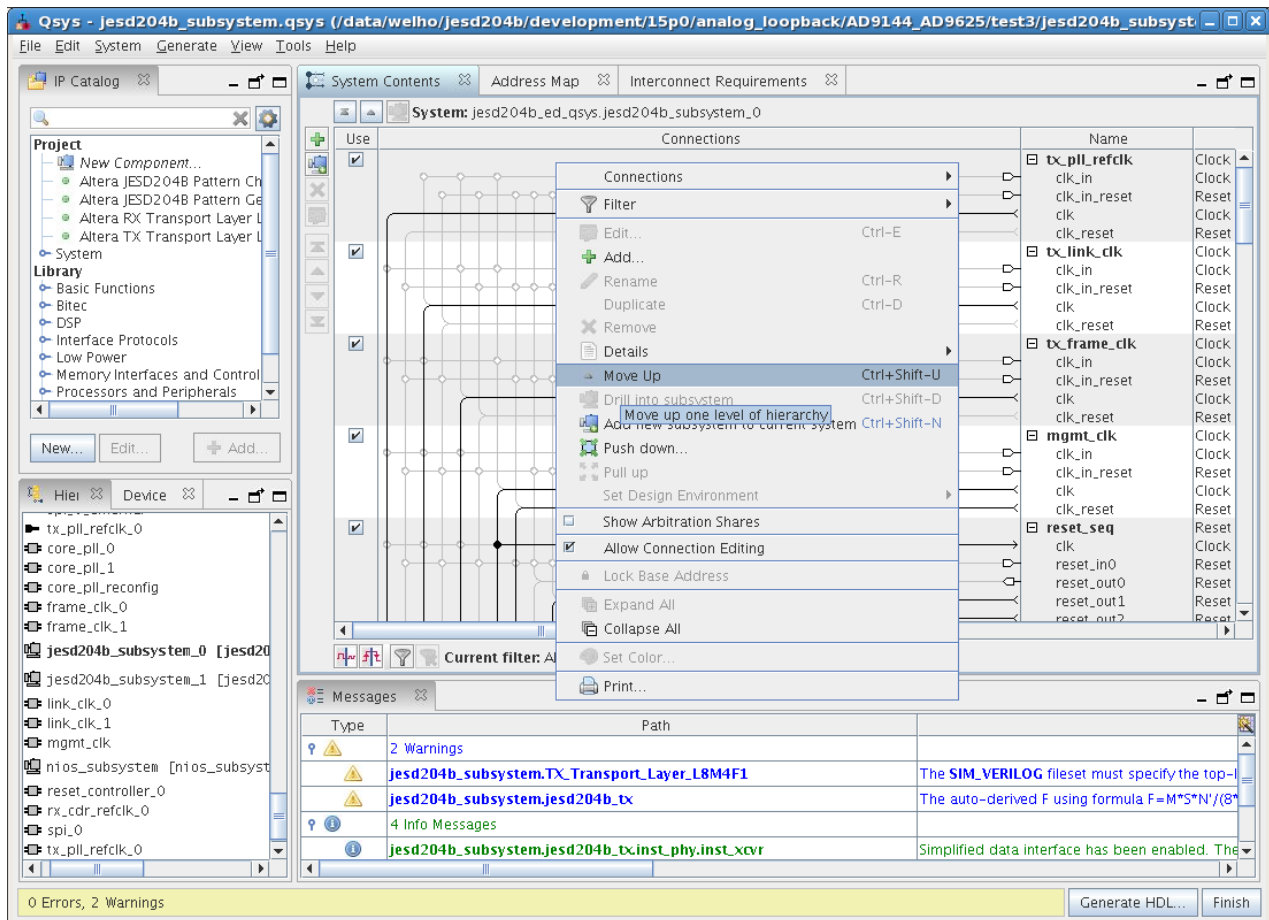
- Launch QSYS and open **sine_wave_gen_16.qsys**.
- At the **Frequency** tab, change the **Clock Rate** to 250.00MHz. Change the **Desired Output Frequency** to 2.5000MHz.
- Click **Generate HDL...** button to re-generate the NCO IP. Click **Finish** after the re-generation finishes.
- Open the **jesd204b_ed.qsys.qsys** file.
- Change the **tx_pll_refclk_0**, **link_clk_0** and **frame_clk_0** clock sources frequencies to 250MHz.
- Change the **core_pll_0** reference clock frequency to 250MHz. Change the output frequencies for TX link and frame clock to 250MHz.
- Select **jesd204b_subsystem_0**, right click and select **Drill into subsystem**.
- In the **jesd204b_subsystem_0**, change the **tx_pll_refclk**, **tx_link_clk** and **tx_frame_clk** frequency to 250MHz.
- Change the **jesd204b_tx** instance data rate to 10000Mbps.
- At the **xcvr_atx_pll_a10_0** instance, change the **PLL output frequency** to 5000.0MHz. Select 250MHz from the **PLL integer reference clock frequency** dropdown list.
- Right click at any space below the **Connections** title bar in the **System Contents** tab. Select **Move Up** to go back to the top QSYS hierarchy.
- Click **Generate HDL...** button to re-generate the entire QSYS system. The re-generation process takes several minutes. Click **Finish** after the re-generation finishes.
- At the **jesd204b_ed.sdc** file, change the **tx_device_clk** and **tx_pll_refclk** period to 4.00.
- Perform full compilation in Quartus II software and make sure the compilation is successful.

The NIOS II software needs to be re-built because the **jesd204b_ed.qsys.sopcinfo** file has been updated. To re-build the NIOS II software through Eclipse, perform the following steps:

- Launch the **NIOS II Software Build Tools for Eclipse**.
- Click **Browse** button when **Workspace Launcher** window appears. Navigate to the **software** folder in this reference design project folder and click **OK**.
- To import the software project from the **jesd204_nios_ed.zip** file, right click at the **Project Explorer** pane and select **Import**.
- Under the **General** icon, select **Existing Projects into Workspace** and click **Next**.
- Click on the **Select archive file** radio button. Click **Browse** to navigate and select **jesd204_nios_ed.zip** file. Click **OK** and followed by **Finish**. The software project will be setup in your workspace.
- Right click at the **jesd204_nios_ed_bsp** folder under the **Project Explorer** pane. Select **NIOS II** and then select **Generate BSP** to re-generate the BSP.

- Right click at the **jесd204_nios_ed** folder under the **Project Explorer** pane. Select **Clean Project** to delete the old ELF image and then select **Build Project** to generate the new ELF image. The original ELF image is stored at the **master_image** folder in reference design project folder.

Figure 10: Move up the QSYS hierarchy



Before you run the reference design at 10Gbps, perform the following steps:

- Set the X3 on-board VCXO frequency to 250.0MHz using the Clock Control GUI.
- Backup the original SOF and ELF images in the **master_image** folder.
- Copy the generated SOF file from the **output_files** folder to **master_image** folder.
- Copy the generated ELF file from **software/jesd204_nios_ed** folder to **master_image** folder.
- At the reference design folder, type **.run.sh** in the NIOS II command shell.

Revision History

Date	Version	Changes
2015 October	1.0	Initial release