Intel® Stratix® 10 Programmable Acceleration Card (PAC) 4-Channel DDR4 RDIMM Design Manual

2019.01.22

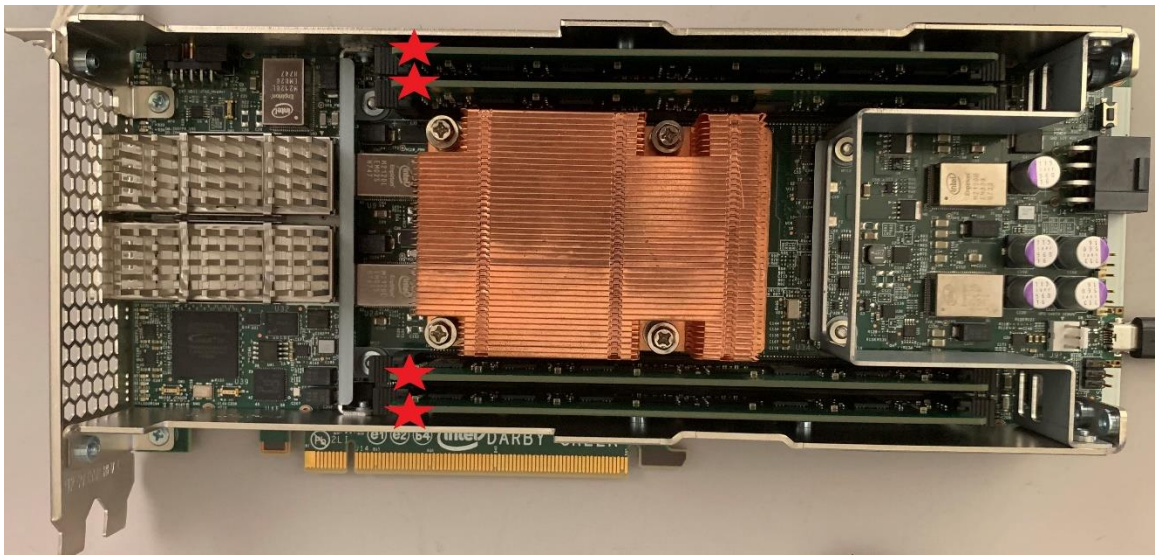
Contents

1. Introduction

1.1. Introduction

This document describes a reference design that uses 4 channels of DDR4 RDIMM memory on an Intel® Stratix® 10 PAC. This reference design leverages the out-of-the box Intel® Stratix® 10 EMIF IP available in Quartus Pro to interface with the four, independent RDIMM memory devices on the Stratix® 10 PAC. This design may be used as an example of how to interface with the 4 channels of DDR4 DIMM available on the Stratix® 10 PAC, simultaneously, using Quartus EMIF IP.

Figure 1 **Intel® Stratix® 10 PAC w/ DDR4 RDIMM Devices Identified**



Related Information

External Memory Interfaces Intel® Stratix® 10 FPGA IP User Guide

1.2. Design Specifications

Table 1 **General Specifications**

Specification Name	Specification Value
Board Name	Intel® Stratix® 10 Programmable Acceleration Card
FPGA P/N	1SX280HN2F43E2VGS3

# External Memory Devices	4
fMAX	300 MHz
Memory Clock Frequency	1200 MHz
Quartus Version	Pro 18.1.0

Table 2 Memory Device Specifications

Specification Name	Specification Value
Part No.	Micron MTA9ASF1G72PZ
Rated Speed Grade	DDR4-2666
Memory Format	RDIMM
Density	8 GB
# of DQ Pins	64
# of DQ Groups	8
Row Address Width	16 bits
Column Address Width	10 bits
Bank Address Width	2 bits
Bank Group Width	2 bit

1.3. Design Requirements

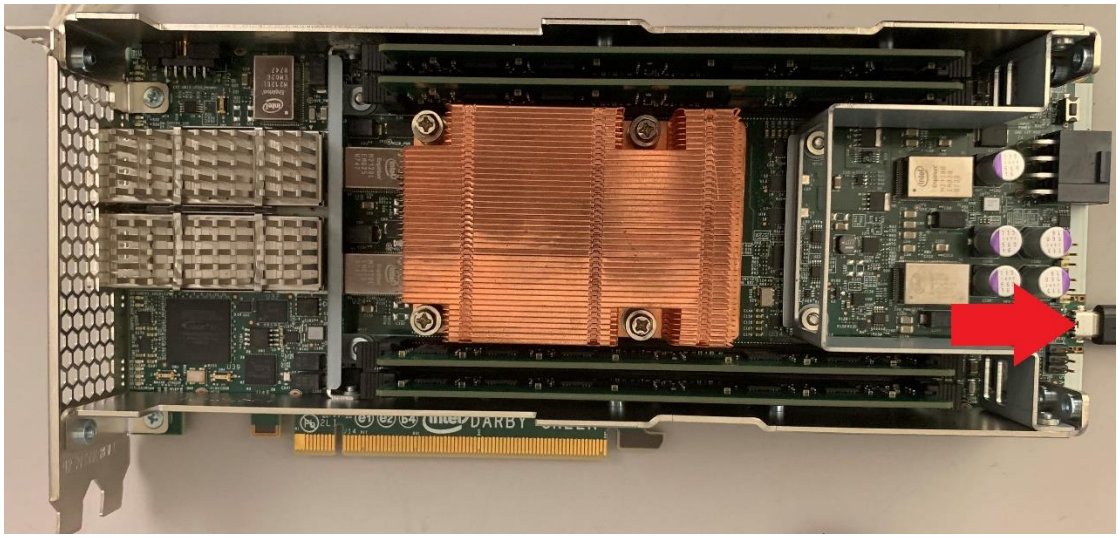
This reference design requires the following:

- Intel® Stratix® 10 Programmable Acceleration Card (PAC) rev-c or newer. This PAC contains a 1SX280HN2F43E2VGS3 Intel® Stratix® 10 SX FPGA
- A computer with the Intel® Quartus® Prime Pro Edition software version 18.1 installed. The computer downloads the FPGA SRAM Object File (.sof) to the FPGA on the PAC.

1.4. Running the Reference Design on Hardware

1. Place the Intel® Stratix® 10 PAC on an ESD protected surface.
2. Turn on the fans and/or other cooling mechanisms. The PAC doesn't contain any active cooling. Therefore, it **must** have an external cooling mechanism.
3. Connect a micro-USB cable between the computer and the PAC. The location of the micro-USB connector on the PAC is identified in Figure 2 following.

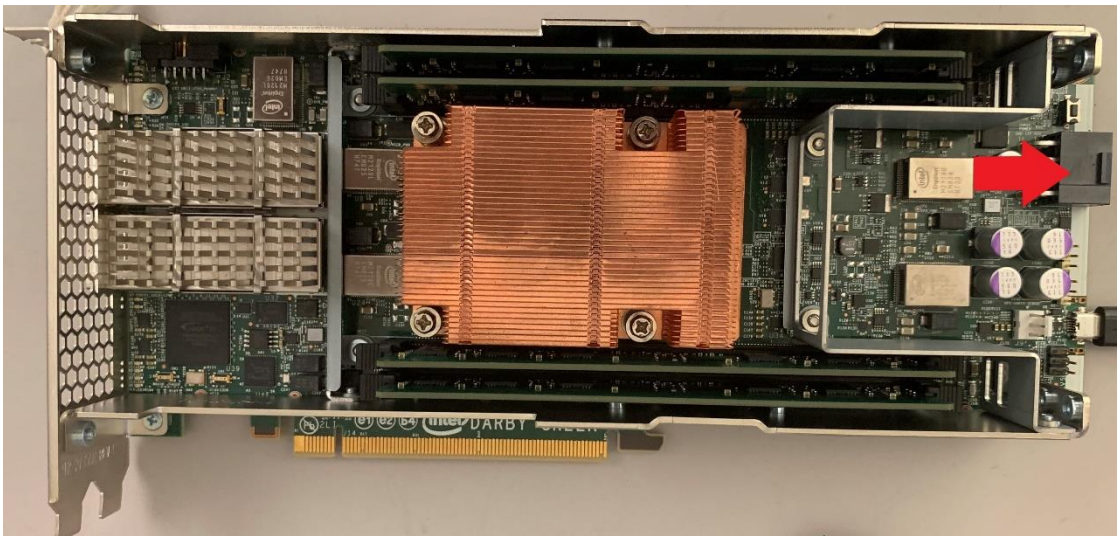
Figure 2 **Intel® Stratix® 10 PAC Micro-USB Connector**



4. **IMPORTANT -** Once power is applied to the PAC it will turn on.

   At this time, connect the power supply to PAC. The location of the power connector on the PAC is identified in Figure 3 below.

Figure 3 **Intel® Stratix® 10 PAC Power Connector**



5. On the computer, use the Quartus® Prime 18.1 Programmer to load the .sof file onto the PAC. The .sof file is located in the *<ROOT_PROJECT_DIRECTORY>/output_files* directory.

   After successfully programming the .sof, the reference design will be running on the PAC. Please see Section 3 for information on how to verify the design is functioning

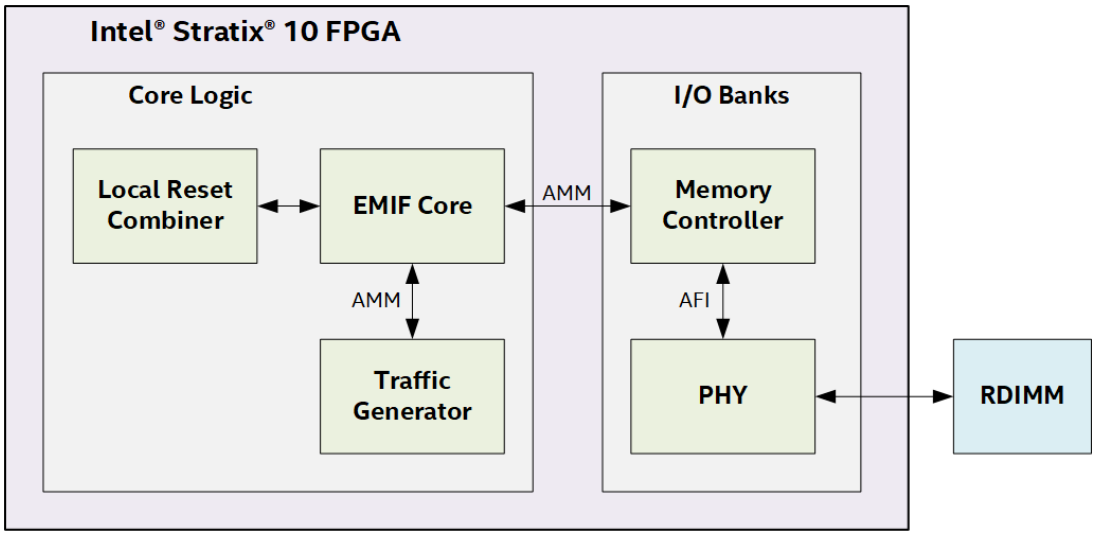
2. Reference Design Description

2.1. Introduction

This reference design uses out-of-the-box IP available in Quartus® Prime Pro 18.1. Three different IP's are used: EMIF, Traffic Generator, and Local Reset Combiner as is illustrated in Figure 4 following. A description of each IP is presented below. All three IP's were generated as part of the example design generation process for the *External Memory Interfaces Intel® Stratix® 10 FPGA IP* available in Quartus® Prime Pro 18.1.

- *EMIF* - This IP is used to interface with the external memory device. Four instances of the EMIF IP are present in this design, once for each memory device. The EMIF IP contains a small core-logic portion that exposes an Avalon Memory-Mapped (AMM) interface to the Hardened Memory Controller (HMC). The HMC communicates with the PHY using the Altera PHY Interface (AFI). Lastly, the PHY interfaces with the I/O lanes connected to the RDIMM device. For information on the EMIF IP architecture please refer to the EMIF Stratix® 10 FPGA IP User Guide.
- *Traffic Generator* – This IP generates a PRBS31 pattern using linear-feedback shift register's (LFSR's) to emulate memory traffic. This pattern is written to the memory device, read from the memory and checked for bit errors. This test is referred to as the traffic generation test. In this design four independent traffic generators are used simultaneously, one for each memory device.
- *Local Reset Combiner* – This IP is used to accept multiple user-requested resets for the memory device.

Figure 4 Reference Design Block Diagram



Related Information

External Memory Interfaces Intel® Stratix® 10 FPGA IP User Guide

2.2. I/O Column Usage for RDIMM Devices

On the Intel® Stratix® 10 PAC two I/O columns are utilized for interfacing with the four DDR4 RDIMM devices; two RDIMM devices interface to each I/O column. The I/O column usage for external memory interfaces must be taken into account when creating debug strategies. In particular when the EMIF Toolkit is used, the memory interfaces need to be configured such that the EMIF Toolkit debug interface is daisy-chained between memory devices on the same I/O column. More information on this configuration will be discussed in Section 2.6. Debugging this reference design using the EMIF toolkit will be discussed in section 3.3.

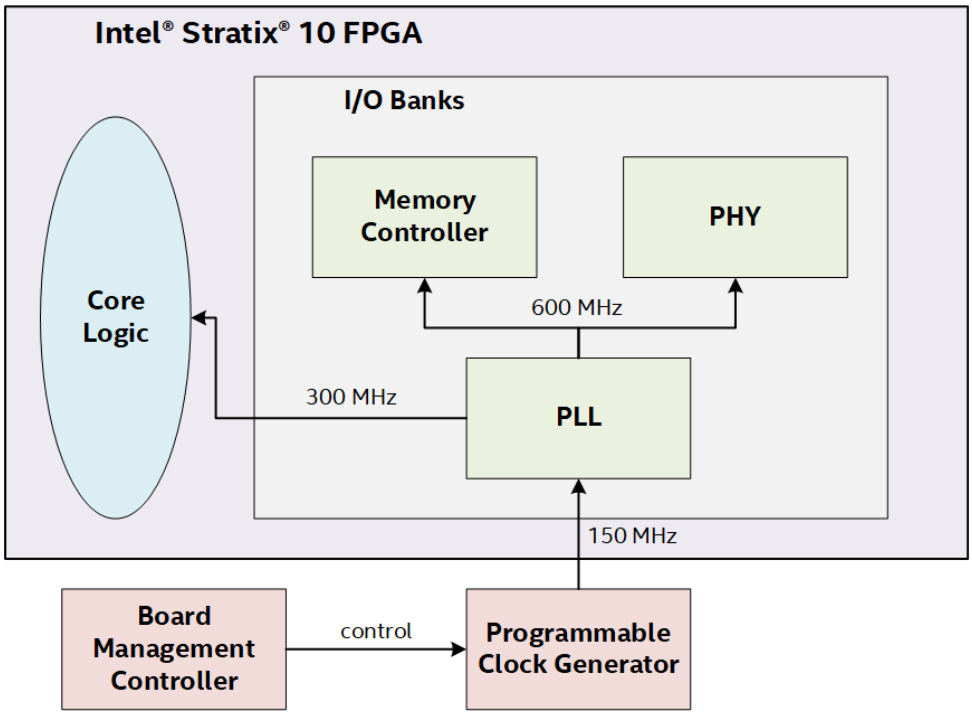
2.3. Clocking Scheme

In this reference design, each RDIMM operates at 1200 MHz. A simplified diagram of the clocking scheme used in this reference design is shown in Figure 5 following.

- A reference input clock is applied to the input of the FPGA I/O PLL. This clock is generated by a programmable clock generator on the PAC (U16 on the schematic). This frequency of this reference clock is controlled by the board management controller (BMC) and is set to be 150 MHz by default. The frequency of this clock should match the *PLL reference clock frequency* setting in the EMIF IP. Please note that the PLL M and N values are determined by these settings in the EMIF IP, regardless of what the PLL input clock frequency actually is.

- A quarter-rate (300 MHz) and half-rate (600 MHz) clock are generated by the I/O PLL's. The quarter rate clock drives the core logic while the half-rate drives the Hardened Memory Controller (HMC) and PHY.

Figure 5 **Reference Design Clocking Scheme Diagram**



Related Information

External Memory Interfaces Intel® Stratix® 10 FPGA IP User Guide

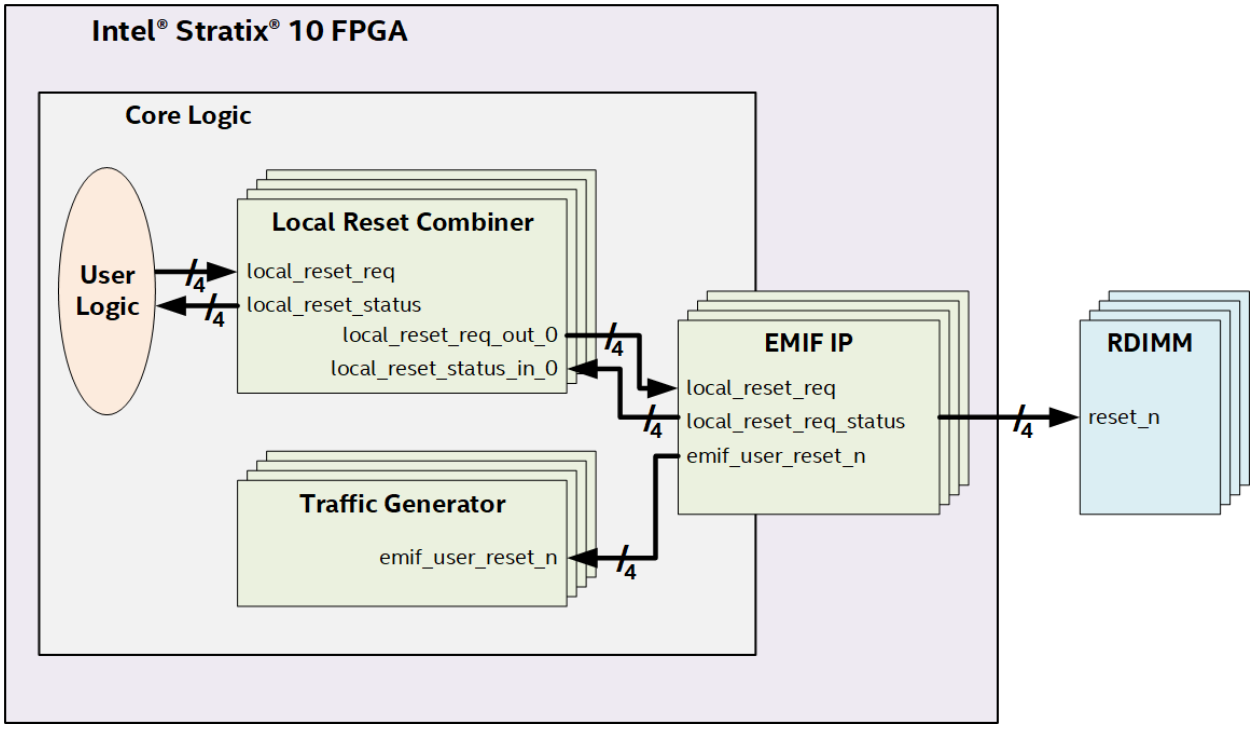
2.4. User-requested Reset Scheme

The user-requested reset scheme available in this example design is illustrated in Figure 6 following. A user-requested reset is commonly performed to put the memory interface(s) in the known power-up state. This scheme works as follows:

1. User logic asynchronously asserts local_reset_req of the local reset combiner for the memory interface to reset.
2. The local reset combiner assets local_reset_req of the EMIF IP. The local reset combiner will follow the EMIF IP reset procedure described in the EMIF Intel® Stratix® 10 FPGA IP User Guide.
3. The EMIF IP asserts the emif_usr_reset_n port connected to the traffic generator

4. The EMIF IP resets the hard-memory controller and PHY.
5. The EMIF IP de-asserts the emif_user_reset_n port
6. The EMIF IP resets the external memory devices via the reset_n signal
7. Calibration is performed on the external memory devices
8. The EMIF IP asserts local_reset_done contained within the local_reset_status conduit indicating the reset has completed to the local reset combiner
9. The local reset combiner asserts local_reset_done contained within the local_reset_status conduit indicating the reset has completed to the user logic

Figure 6 **Reference Design Reset Scheme Diagram**



Related Information

External Memory Interfaces Intel® Stratix® 10 FPGA IP User Guide

2.5. Project Hierarchy

This reference design has the directory structure shown in Figure 7 following. A description of each item in the directory structure is provided in Table 3 and Table 4 following.

Figure 7 Reference Design Directory Structure

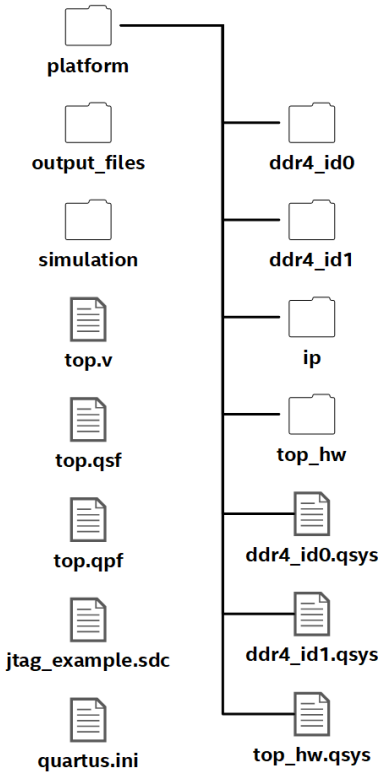


Table 3 Root Reference Directory Item Descriptions

Item Name	Description
platform directory	Contains the IP for this reference design. Please see Table 4 following
output_files directory	Contains the project output files this includes Report files (.rpt), equation files (.eqt) and the SRAM object file (.sof)
simulation directory	Contains files such as post-synthesis netlist(s) that may be used to perform gate-level simulation and power estimation
top.v	The top level entity (e.g. Verilog file) in the reference design
top.qsf	The Quartus® Settings File (.qsf) for the reference design. This file stores project information like Quartus® Version, device information, pin-outs and settings
top.qpf	The Quartus® Prime Pro 18.1 project file for the reference design
jtag_example.sdc	The Synopsis Design Constraint (.sdc) file for this project. This file is generated by the EMIF Stratix® 10 IP.
quartus.ini	Contains configuration settings that are no exposed in the Quartus® Graphical User Interface (GUI)

Table 4 Platform Directory Item Description

Item Name	Description
ddr4_id0 directory	Contains the generated IP files for the DDR4 RDIMM that *exports* the debug interface
ddr4_id1 directory	Contains the generated IP files for the DDR4 RDIMM that *imports* the debug interface
ip directory	Contains the following .IP files: • *ed_synth_emif_s10_0_id0.ip* – The IP file for the EMIF core which exports the debug interface • *ed_synth_emif_s10_0_id1.ip* – The IP file for the EMIF core which imports the debug interface • *ed_synth_local_reset_combiner.ip* – The IP file for the local reset combiners • *ed_synth_tg.ip* – The IP file for the traffic generators
top_hw directory	Contains the generated IP files for the top-level Platform Designer system in this reference design
ddr4_id0.qsys	The Platform Designer sub-system for the DDR4 RDIMM that *exports* the debug interface
ddr4_id1.qsys	The Platform Designer sub-system for the DDR4 RDIMM that *imports* the debug interface
top_hw.qsys	The top-level Platform Designer system in the reference design

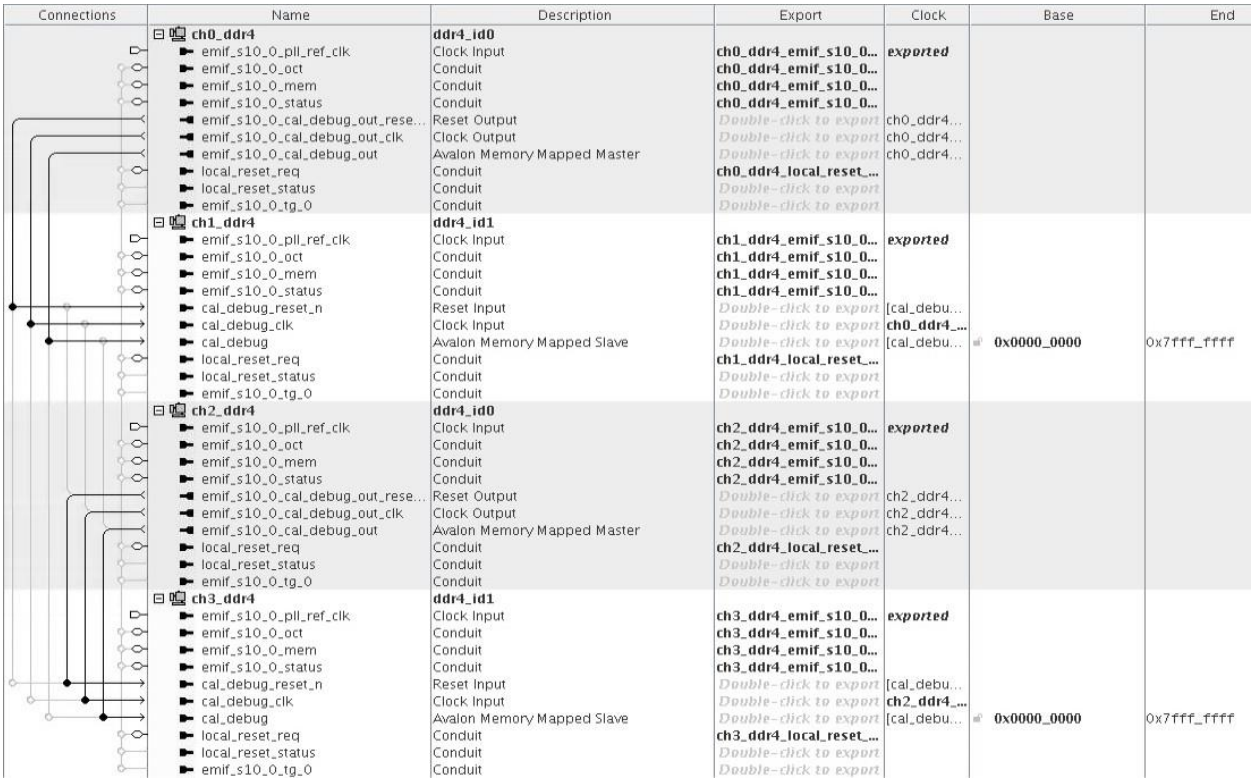
2.6. Platform Designer System

The root Platform Designer system used in this reference design is shown in Figure 8 following. This system is represented by the top_hw.qsys file in the *<ROOT_PROJECT_DIRECTORY>/platform* directory. This root Platform Designer system contains four Platform Designer sub-systems, one for each DDR4 RDIMM interface.

As mentioned in Section 2.2, memory devices that interface to the same I/O column must have daisy chained debug interfaces. Therefore, in this reference design, *ch0_ddr4*'s debug interface is exported to *ch1_ddr4*. Likewise, the *ch2_ddr4*'s debug interface is export to *ch3_ddr4*. In this Platform Designer system *ddr4_id0* represents the IP set for the memory interface that exports the debug interface while *ddr4_id1* represents the IP set for the memory interface that imports the debug interface.

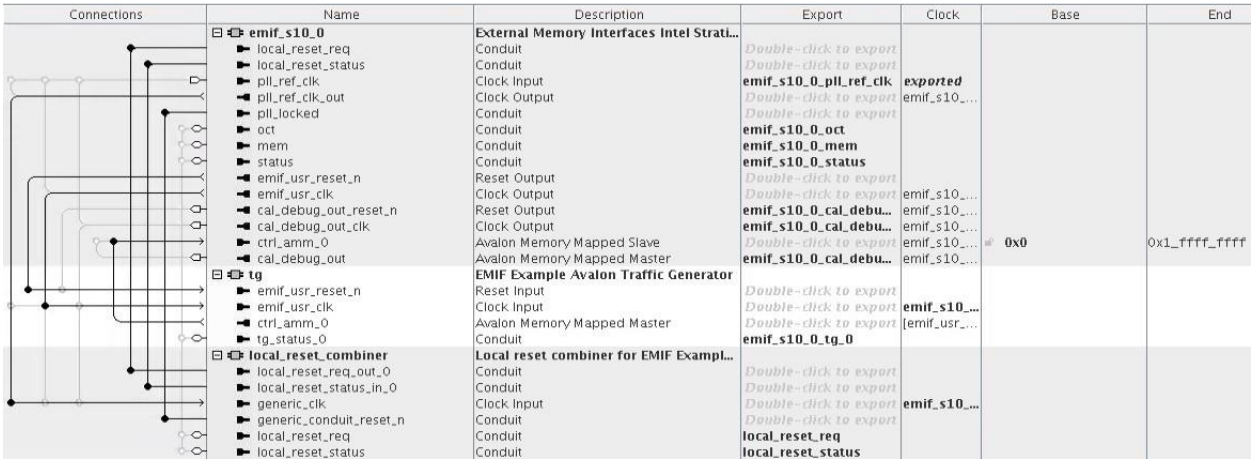
The Platform Designer sub-system for the memory interfaces that export a debug interface in shown in Figure 9 following. The Platform Designer sub-system for the memory interfaces that import a debug interface is show in Figure 10 following.

Figure 8 Reference Design Top Level Platform Designer System



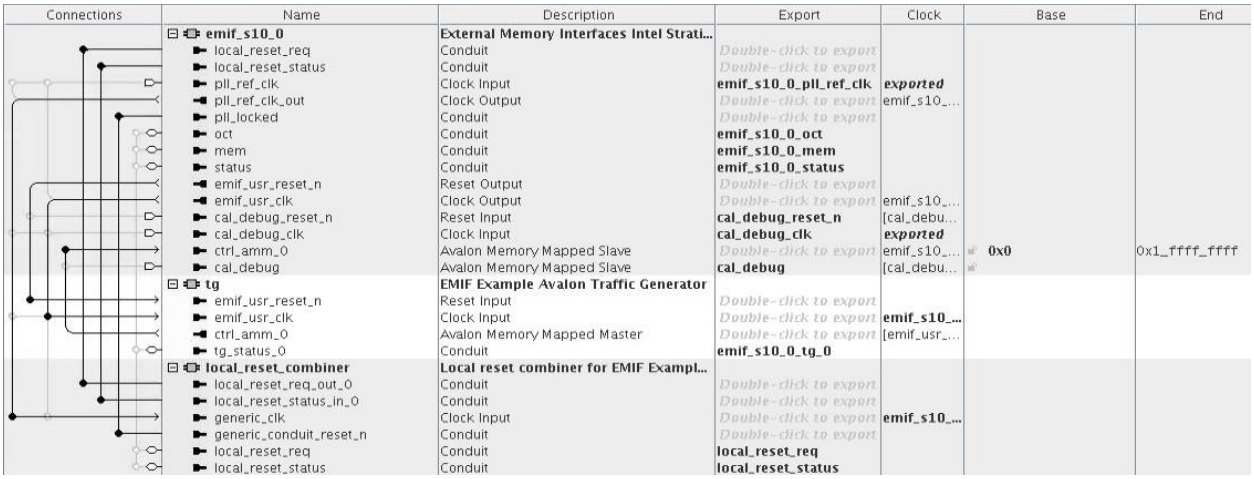
Connections	Name	Description	Export	Clock	Base	End
	ch0_ddr4	ddr4_id0				
	emif_s10_0_pll_ref_clk	Clock Input	ch0_ddr4_emif_s10_0...	exported		
	emif_s10_0_oct	Conduit	ch0_ddr4_emif_s10_0...			
	emif_s10_0_mem	Conduit	ch0_ddr4_emif_s10_0...			
	emif_s10_0_status	Conduit	ch0_ddr4_emif_s10_0...			
	emif_s10_0_cal_debug_out_rese...	Reset Output	Double-click to export	ch0_ddr4...		
	emif_s10_0_cal_debug_out_clk	Clock Output	Double-click to export	ch0_ddr4...		
	emif_s10_0_cal_debug_out	Avalon Memory Mapped Master	Double-click to export	ch0_ddr4...		
	local_reset_req	Conduit	ch0_ddr4_local_reset_...			
	local_reset_status	Conduit	Double-click to export			
	emif_s10_0_tg_0	Conduit	Double-click to export			
	ch1_ddr4	ddr4_id1				
	emif_s10_0_pll_ref_clk	Clock Input	ch1_ddr4_emif_s10_0...	exported		
	emif_s10_0_oct	Conduit	ch1_ddr4_emif_s10_0...			
	emif_s10_0_mem	Conduit	ch1_ddr4_emif_s10_0...			
	emif_s10_0_status	Conduit	ch1_ddr4_emif_s10_0...			
	cal_debug_reset_n	Reset Input	Double-click to export	[cal_debu...		
	cal_debug_clk	Clock Input	Double-click to export	ch0_ddr4_...		
	cal_debug	Avalon Memory Mapped Slave	Double-click to export	[cal_debu...	0x0000_0000	0x7fff_ffff
	local_reset_req	Conduit	ch1_ddr4_local_reset_...			
	local_reset_status	Conduit	Double-click to export			
	emif_s10_0_tg_0	Conduit	Double-click to export			
	ch2_ddr4	ddr4_id0				
	emif_s10_0_pll_ref_clk	Clock Input	ch2_ddr4_emif_s10_0...	exported		
	emif_s10_0_oct	Conduit	ch2_ddr4_emif_s10_0...			
	emif_s10_0_mem	Conduit	ch2_ddr4_emif_s10_0...			
	emif_s10_0_status	Conduit	ch2_ddr4_emif_s10_0...			
	emif_s10_0_cal_debug_out_rese...	Reset Output	Double-click to export	ch2_ddr4...		
	emif_s10_0_cal_debug_out_clk	Clock Output	Double-click to export	ch2_ddr4...		
	emif_s10_0_cal_debug_out	Avalon Memory Mapped Master	Double-click to export	ch2_ddr4...		
	local_reset_req	Conduit	ch2_ddr4_local_reset_...			
	local_reset_status	Conduit	Double-click to export			
	emif_s10_0_tg_0	Conduit	Double-click to export			
	ch3_ddr4	ddr4_id1				
	emif_s10_0_pll_ref_clk	Clock Input	ch3_ddr4_emif_s10_0...	exported		
	emif_s10_0_oct	Conduit	ch3_ddr4_emif_s10_0...			
	emif_s10_0_mem	Conduit	ch3_ddr4_emif_s10_0...			
	emif_s10_0_status	Conduit	ch3_ddr4_emif_s10_0...			
	cal_debug_reset_n	Reset Input	Double-click to export	[cal_debu...		
	cal_debug_clk	Clock Input	Double-click to export	ch2_ddr4_...		
	cal_debug	Avalon Memory Mapped Slave	Double-click to export	[cal_debu...	0x0000_0000	0x7fff_ffff
	local_reset_req	Conduit	ch3_ddr4_local_reset_...			
	local_reset_status	Conduit	Double-click to export			
	emif_s10_0_tg_0	Conduit	Double-click to export			

Figure 9 Platform Designer Sub-system, External Memory Interface w/ Debug Interface Export



Connections	Name	Description	Export	Clock	Base	End
	emif_s10_0	External Memory Interfaces Intel Strati...				
	local_reset_req	Conduit	Double-click to export			
	local_reset_status	Conduit	Double-click to export			
	pll_ref_clk	Clock Input	emif_s10_0_pll_ref_clk	exported		
	pll_ref_clk_out	Clock Output	Double-click to export	emif_s10_...		
	pll_locked	Conduit	Double-click to export			
	oct	Conduit	emif_s10_0_oct			
	mem	Conduit	emif_s10_0_mem			
	status	Conduit	emif_s10_0_status			
	emif_usr_reset_n	Reset Output	Double-click to export			
	emif_usr_clk	Clock Output	Double-click to export	emif_s10_...		
	cal_debug_out_reset_n	Reset Output	emif_s10_0_cal_debu...	emif_s10_...		
	cal_debug_out_clk	Clock Output	emif_s10_0_cal_debu...	emif_s10_...		
	ctrl_amm_0	Avalon Memory Mapped Slave	Double-click to export	emif_s10_...	0x0	0x1_ffff_ffff
	cal_debug_out	Avalon Memory Mapped Master	emif_s10_0_cal_debu...	emif_s10_...		
	tg	EMIF Example Avalon Traffic Generator				
	emif_usr_reset_n	Reset Input	Double-click to export			
	emif_usr_clk	Clock Input	Double-click to export	emif_s10_...		
	ctrl_amm_0	Avalon Memory Mapped Master	Double-click to export	[emif_usr_...		
	tg_status_0	Conduit	emif_s10_0_tg_0			
	local_reset_combiner	Local reset combiner for EMIF Exampl...				
	local_reset_req_out_0	Conduit	Double-click to export			
	local_reset_status_in_0	Conduit	Double-click to export			
	generic_clk	Clock Input	Double-click to export	emif_s10_...		
	generic_conduit_reset_n	Conduit	Double-click to export			
	local_reset_req	Conduit	local_reset_req			
	local_reset_status	Conduit	local_reset_status			

Figure 10 Platform Designer Sub-system, External Memory Interface w/ Debug Interface Import



3. Debugging the Reference Design

3.1. Introduction

To verify the reference design is functioning ISSP or the EMIF Toolkit may be used. In general, this verification process involves verifying that the memory device calibration and traffic generation (e.g. driver margining) test passed. More information on both of these can be found in the External Memory Interface Intel® Stratix® 10 FPGA IP User Guide.

Related Information

External Memory Interfaces Intel® Stratix® 10 FPGA IP User Guide

3.2. In-System Sources and Probes (ISSP)

To verify the design using ISSP, read the values of the probes listed in Table 5 below. Please note, there will be four sets of these probes, one for each DDR4 RDIMM devices. Thus, verify all four CALP and TGP probes have a high logic value.

Table 5 Reference Design ISSP Probe Descriptions

Probe Name	Description
PLLL	A logic high indicates the PLL has locked to the input reference clock
CALP	A logic high indicates that calibration has passed
CALF	A logic high indicates that calibration has failed
TGP	A logic high indicates that the traffic generation test has passed
TGF	A logic high indicates that the traffic generation test has failed
TGT	A logic high indicates that the traffic generation test has timed-out

3.3. External Memory Interfaces (EMIF) Toolkit

The EMIF Toolkit provides the ability to analyze EMIF's in detail. Usage of the EMIF Toolkit is covered in depth in the External Memory Interface Intel® Stratix® 10 FPGA IP User Guide. The general process applicable to this reference design is summarized below.

1. Open the reference design in Quartus Prime Pro 18.1.
2. Program the PAC with this reference design's .sof file (*output_files/top.sof*).

3. Open the EMIF Toolkit by selecting **Tools ➤ System Debugging Tools ➤ EMIF Toolkit**
4. Once the EMIF Toolkit opens, create a connection to the PAC:
    a. Double-click **Tasks ➤ Connection Setup ➤ Initialize connections**
    b. Double-click **Tasks ➤ Connection Setup ➤ Link Project to Device...**
    c. Select the PAC device and this reference's design *top.sof* and press **OK**
5. Create a connection to the memory interface to analyze:
    a. Double-click **Tasks ➤ Connections ➤ Create Memory Interface Connection...**
    b. Ensure the PAC and Stratix 10 FPGA are selected for the *Hardware* and *Device* inputs
    c. For the *Memory interface* drop down, select the I/O column to use. There will be two options as in this reference design two DDR4 RDIMM devices interface to two different I/O columns. As will be seen, you'll be able to switch between memory devices on the same I/O column
    d. Press **OK**
    e. Optionally repeat steps a-d for the other I/O column. You can then switch between connections in the remaining steps to test all four memory devices.
6. Select the memory interface to analyze
    a. Double-click **Tasks ➤ Memory Interface ➤ Settings ➤ Select Active Interface**
    b. For the **Interface** dropdown select *Interface 0* for the ch0 or ch2 DDR4 RDIMM devices and *Interface 1* for ch1 or ch3 DDR4 RDIMM devices
    c. Press **OK**
7. Double-click on **Tasks ➤ Memory Interface ➤ Commands ➤ Rerun Calibration**
8. Navigate to Reports **DDR4 ➤ <MEMORY CONNECTION> ➤ Calibration Report.** The following information is available in the calibration report:
    - Calibration Status Per Group table: Lists the pass/fail status per group.
    - DQ Pin Margins Observed During Calibration table: Lists the DQ read/write margins and calibrated delay settings. These are the expected margins after calibration, based on calibration data patterns. This table also contains DM/DBI margins, if applicable.
    - DQS Pin Margins Observed During Calibration table: Lists the DQS margins observed during calibration.
    - FIFO Settings table: Lists the VFIFO and LFIFO settings made during calibration.
    - Latency Observed During Calibration table: Lists the calibrated read/write latency.
    - Address/Command Margins Observed During Calibration table: Lists the margins on calibrated A/C pins, for protocols that support Address/Command calibration.

    To verify calibration passed for a particular external memory interface:
    a. Click on **DDR4 ➤ <MEMORY CONNECTION> ➤ Summary**
    b. The *Calibration* line item will show the calibration result

9. To verify the results of traffic generation test (e.g. driver margining)
    a. Double click on **Tasks ➤ Memory Interface ➤ Commands ➤ Driver Margining.**
    b. In the pop-up window that appears, select the corresponding ISSP probes and leave the other setting at their default value.
    c. Press **OK** to run the
    d. Navigate to Reports **DDR4 ➤ <MEMORY CONNECTION> ➤ Margin Report**
    e. In the tables contained with the Margin Report verify all margins are greater than zero.