ADC Convertor Using the
MAX 10 FPGA Development Kit
1. **Description**

10M50DA device has two analog-to-digital converters (ADC) which can be used to monitor the internal temperature of the die and support external analog signal conversion. So this design example is used to check out FPGA embedded ADC components alongside with external DAC and potentiometer on the board. Please download the installer of MAX 10 FPGA development kit and use BTS GUI to try it out.

![Max10 FPGA Development Kit](image)

2. **Operation of the Design:**

This design example demonstrates the working of two analog-to-digital convertors (ADC) in MAX 10 FPGA device on the Max 10 Development Kit. The ADC solution provides the built-in capability to translate analog quantities to digital data for information processing, computing, data transmission, and control system. It has a 12-bit successive approximation register for each ADC channel which represents the analog signal being observed with 1MSPs sample rate. Please refer to MAX 10 handbook for more info about embedded ADC component.

3. **Reconstruct the Design:**

This design example has a system Qsys component which includes ADC cores and JTAG-Avalon MM interface, so that you can access and monitor the design via system-console. Qsys platform is pretty easy to use and facilitate you to reconstruct the design to meet your design requirements.
4. How to run the ADC design example on the MAX 10 Development kit

1) Download the adc.par from the design store.
2) Use the command "quartus_sh --platform_install -package <directory-path>/adc.par" to install the design template
3) Use the command "quartus_sh --platform -name adc" to unarchive the project and get all the design files.
4) Recompile the design or directly use SOF image at master_image folder
5) Power off the kit and connect external analog input(s) (Threshold: 2.5V) to ADC channel(s) if possible
6) Power on the kit and configure SOF to MAX 10 FPGA
7) Double click “BoardTestSystem” at “\examples\board_test_system\" to open BTS GUI to test this design.
Note:

DAC output is another option to drive ADCs, however, it is not enabled in BTS GUI by default, so please try to use register configuration way to generate whatever pattern you want.

Acknowledgment
This design is based on ADC for MAX 10 FPGA Development Kit produced by Altera Corporation.

Document Revision History

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<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
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<tbody>
<tr>
<td>May 2015</td>
<td>V1.0</td>
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