Interlaken MegaCore Function Parameter Selection Worksheet

For Throughput and User Clock Frequency Calculation

Introduction

This application note describes the Altera® Interlaken MegaCore® function parameter selection calculator for the specific performance requirements. It is a Microsoft Excel-based tool. The calculator helps user to find throughput for selected line rate and traffic pattern. It also provides reference minimum user clock frequency to meet throughput requirement.

The Interlaken protocol is a high-speed, scalable, channelized interface for chip-to-chip packet transfers. It is designed for 10 Gbits/s to 100 Gbits/s inter-chip connectivity. This wide bandwidth range makes it suitable for many applications and allows generations of devices to be backward-compatible. Sample applications include OC-768 SONET framers to network processor interface, next-generation 100 Gbits/s Ethernet MAC to packet processor interface, line card to switch fabric interface, etc. Figure 1 gives an example of 40G Packet over SONET line card architecture. The Interlaken interface can be used in three places in Figure 1 line card architecture:

1. The interconnect between STS-768 framer and NPU
2. The interconnect between NPU and traffic manager
3. The interconnect between Traffic manager and switch fabric interface

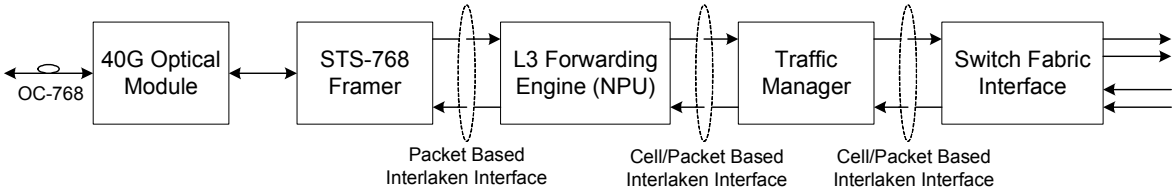


Figure 1. Single Port OC-768 Packet over SONET Line Card

The interface between STS-768 framer and NPU is packet based that the packet size varies. Interlaken is ideal to handle variable size packets. Interlaken divides the packets into smaller bursts, delineated by a header. The bursts are striped as words, round robin, across the SerDes lanes. The connection between NPU and Traffic Manager, or between Traffic Manager and Switch Fabric can be either cell based or packet based.

The Interlaken MegaCore Function Parameter Selection worksheet is designed to help user handle parameters for both cells based design and packet based design. It has three sections:

1. Parameter configuration and throughput calculation section.
2. Parameter configuration for cell based/fixed size packet design
3. Parameter configuration for variable size packets with random weighted distribution

In compliance with the Interlaken Protocol Definition Revision 1.2 specification, Altera® Interlaken MegaCore® function allows user to implement both transmitter and receiver functions.

The Calculator Color Code

The calculator is color-coded to indicate their use. The color code is listed on upper right of "MegaCore & Transceiver Settings" worksheet as shown below:

Entry Color Code:	Calculator Input
	Calculator Output
	Fixed Value in Calculation

Pink-shaded fields with black text are input boxes for user to fill in. Blue-shaded fields contain information returned by the calculator. Green-shaded fields with black text are fixed value used by calculator and not user configurable. Nothing prevents user from modifying the blue fields (the results returned by the calculator). However, modifying the blue fields may lead to incorrect calculation results.

Using the Calculator

This section describes the calculator, briefly describing each field or result, and explains how to use it. The calculator begins when user enter the expected Interlaken MegaCore Settings and Transceiver Lane Settings. And then guides user through the selection of various packet pattern affecting clock rates. This application note and the accompanying calculator make the following assumptions that user:

- Familiar with the Interlaken Protocol Specification http://www.interlakenalliance.com/Interlaken_Protocol_Definition_v1.2.pdf
- Familiar with Interlaken MegaCore Function User Guide http://www.altera.com/literature/ug/ug_interlaken.pdf?GSA_pos=4&WT.oss_r=1&WT.oss=interlaken
- Understand Stratix Devices and Transceiver functions

Worksheet Section for Parameter Configuration and Throughput Calculation

This section provides user interface to enter Interlaken MegaCore related parameters including MetaFrameLength, BurstMax, BurstMin, BurstShort and ChannelWidth. It also provides user entries for transceiver parameters including data rate per lane and number of lanes used in design as shown below.

Table 1. Transceiver Lane Parameter Characteristics

Parameters	Type	Description
Data Rate per Lane	User Input	The transceiver link data speed in Gbps
Number of Lanes	User Input	The number of transceivers used by Interlaken MegaCore

The first section of the calculator worksheet provides calculated results for Raw Aggregate Link Bandwidth, PCS Interface Throughput and MetaFrame Payload Throughput as shown in Figure 2 blue-shaded fields. These three parameters are not affected by packet length and traffic pattern.

Table 2. Calculator Throughput Output Characteristics

Parameters	Type	Description
Raw Aggregate Link Bandwidth	Calculator Output	The SUM of data rate from all transceivers used by Interlaken
PCS Interface Throughput	Calculator Output	The data rate PCS must provide in order to keep Raw Aggregate Link Bandwidth fully utilized
MetaFrame Payload Throughput	Calculator Output	The maximum data rate a MetaFrame can carry without overhead.

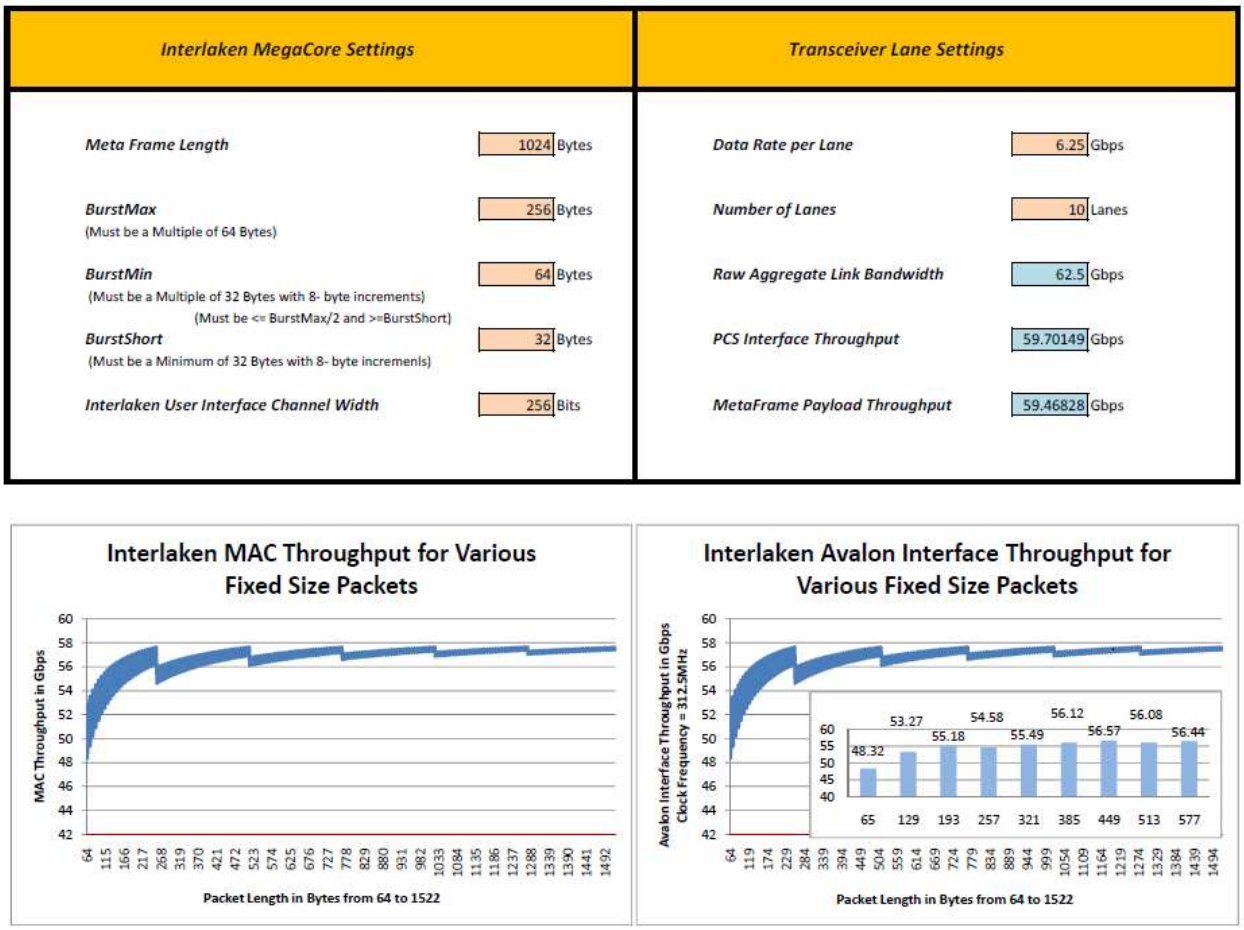


Figure 2. Screenshot for Parameter Configuration and Throughput Calculation Section

The Raw Aggregate Link Bandwidth is calculated from worksheet automatically after Data Rate per Lane and Number of Lanes provided.

The raw aggregate link bandwidth is not the real throughput that can be used for packets transmission. This note will provide throughput calculation at each node as shown in Figure 3.

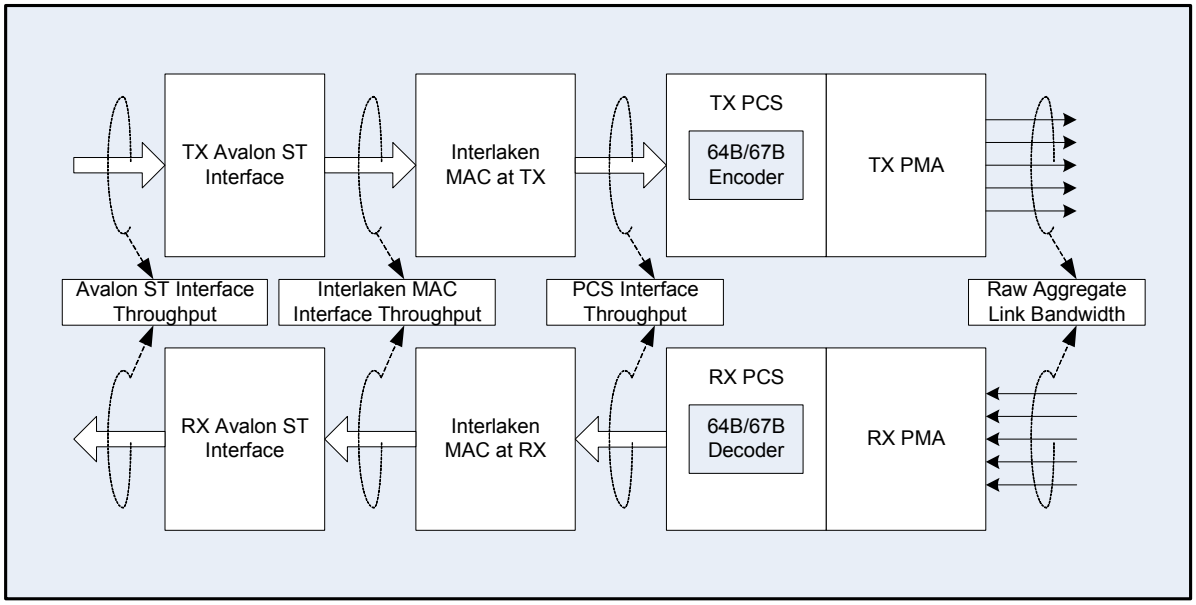


Figure 3. Interlaken Block Diagram and Interface Bandwidth Nodes

Raw Aggregate Link Bandwidth

Interlaken's scalable bandwidth is achieved by its ability to run over a varying number of lanes at varying data rates. The effective bandwidth corresponded directly with the number of lanes and data rate per lane are called Raw Aggregate Link Bandwidth.

$$\text{Raw Aggregate Link Bandwidth} = \text{Number of Lane} \times \text{Data Rate per Lane}$$

The Interlaken MegaCore IP for Stratix IV devices supports a limited number of link configurations as listed in Table 3:

Table 3. Stratix IV Supported Raw Aggregate Link Bandwidth in Gbps

Number of Lanes	Raw Aggregate Link Bandwidth in Gbps			
	3.125	6.25	6.375	10.3125
4	12.5	25.00	25.50	—
8	25	50.00	51.00	—
10	—	62.50	63.75	—
12	—	75.00	76.50	123.75
20	—	125.00	127.50	—

Stratix V provides better scalability and flexibility to support Interlaken. The data rates tested include 3.125Gbps, 5Gbps, 6.25Gbps, 6.375Gbps, 10.3125Gbps. The number of lane supported can be any from 1 to 24.

PCS Interface Throughput

Interlaken Protocol requires 64B/67B encoding before data transmission. The encoding scheme creates an overhead of roughly 4.5%. So the maximum bandwidth that PCS can carry data at PCS TX interface and PCS RX interface are calculated in following equation:

$$\text{PCS Interface throughput} = \text{Raw Aggregate Link Bandwidth} \times (64/67)$$

Meta Frame Payload Throughput

The first section of the calculator worksheet provides pink-shaded field for Interlaken MegaCore parameters listed in Table 4 which affects packet throughput.

Table 4. Interlaken MegaCore Parameter Characteristics

Parameters	Type	Description
MetaFrameLength	User Input	The Meta Frame is defined as the per-lane set of the Synchronization, Scrambler State, Skip, and Diagnostic words, along with the payload data (burst data and control information) carried on each lane. The length of Meta Frame sent on each lane is in 8-bit (1-byte) words
BurstMax	User Input	Maximum size of a data burst which must be multiple of 64 bytes and greater than 2x BurstMin.
BurstMin	User Input	Parameter to specify the smallest end-of-packet burst which must be a minimum of 32 bytes with 8-byte increments.
BurstShort	User Input	Minimum interval between Burst Control Words which must be a minimum of 32 bytes with 8-byte increments. BurstShort can not be greater than BurstMin.
ChannelWidth	User Input	The data bus width at user interface. Interlaken MegaCore provides three user selectable options: 128, 256 and 512 bits

The Interlaken use Meta Frame as payload carrier. The Meta Frame requires per-lane insertion of Synchronization, Scrambler State, Skip, and Diagnostic words, along with the payload data carried on each lane as shown in Figure 4. Because the Synchronization, Diagnostic, and Scrambler State Words are sent so infrequently they consume a minimal amount of interface bandwidth. The overhead is dependent on the size of MetaFrameLength. The maximum usable payload throughput in Meta Frame can be calculated from following equation:

$$\text{MetaFramePayload throughput} = \text{PCS Interface throughput} \times (\text{MetaFrameLength} - 4)/\text{MetaFrameLength}$$

For a hypothetical 2K words the worst-case overhead (with one Skip Word) is:

$$32/ (16{,}384) = 0.20\%$$

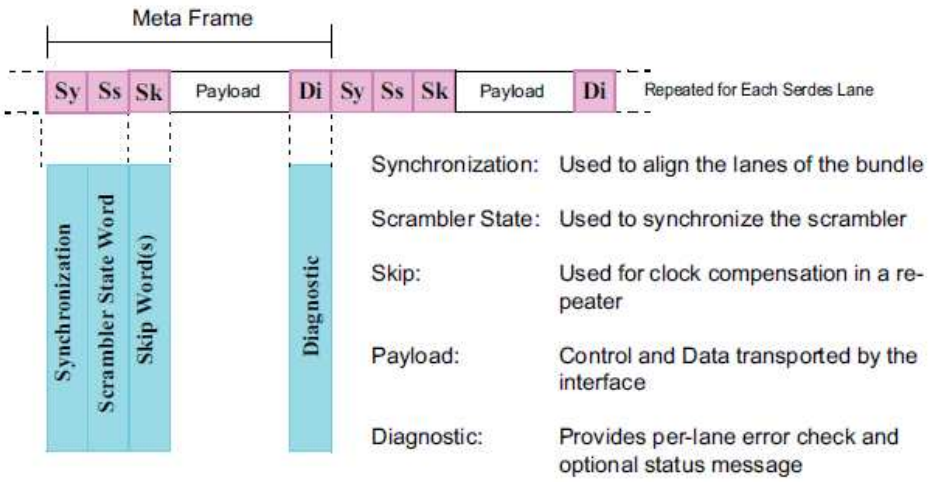


Figure 4. Interlaken Meta Frame Structure from Interlaken Protocol Definition Specification V1.2

Interlaken MAC throughput

The Interlaken MAC typically operates by sending a burst of data of BurstMax length followed by a Control Word. For the purpose of segmenting a packet of arbitrary size into bursts, BurstMax, BurstMin and BurstShort are defined by Interlaken Protocol Definition Specification. The first section of the calculator worksheet provides pink-shaded field for user to select BurstMax, BurstMin and BurstShort as shown in Figure 2 and listed in Table 4. Control words are extra overhead to occupy link bandwidth. The maximum usable data bandwidth at Interlaken MAC interface can be calculated from following equation:

$$\text{Interlaken MAC Interface throughput} = \text{MetaFramePayload throughput} \times \text{MetaFrameDataBurst throughput}$$

Which the **MetaFrameDataBurst** throughput is calculated from:

$$\text{MetaFrameDataBurst throughput} = \sum \text{DataBurstEachFrame} / \sum (\text{DataBurst} + \text{ControlWord}) \text{EachFrame}$$

From above equation, increasing MetaFrameLength and/or BurstMax will improve Interlaken MAC throughput. Because the packet length variation, there will be a very small amount of remaining data left for certain packet size which cause higher overhead. The higher percentage overhead would need MAC to be clocked at higher rates to keep up throughput at desired line rate. The bottom left chart in worksheet of parameter configuration and throughput calculation section as shown in Figure 2 shows Interlaken MAC throughput when passing various fixed sized packets. Figure 5 shows MAC throughputs when BurstMax=256 and BurstMax=512. It shows higher BurstMax will increase MAC throughput and less throughput variation for bigger length packets.

Adjusting parameters in worksheet of parameter configuration and throughput calculation section, user could find that Meta Frame Length or BurstMin or BurstShort only cause MAC throughput vary slightly. BurstMax is a key factor to achieve better MAC throughput. MegaCore Channel Width has no effect on MAC throughput but the throughput of user interface for

MegaCore. Avalon interface is one of the user interfaces supported by Altera Interlaken MegaCore.

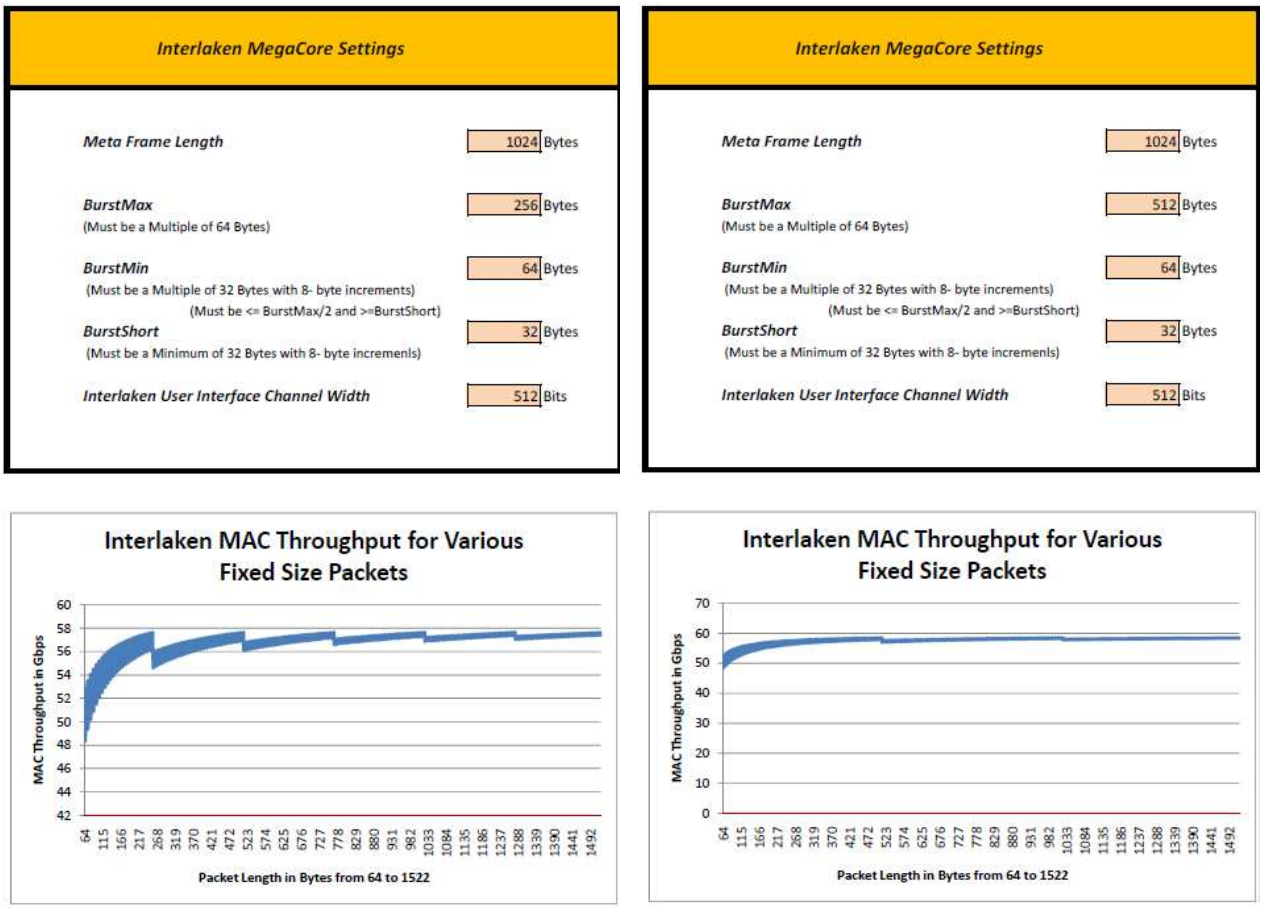


Figure 5. Interlaken MAC throughput comparison for various fixed size packets,

Left Chart BurstMax = 256, Right Chart BurstMax = 512

Avalon ST Interface Throughput

Interlaken MegaCore for Stratix IV and V supports Avalon ST interface for user to integrate their design in FPGA fabric. Because Avalon interface can be channelized, end-of-packet may occur back-to-back on several channels with a very small amount of remaining data on each channel. Avalon ST interface uses startofpacket (SOP) to indicate packet start and endofpacket (EOP) to signal packet end as shown in Figure 6. Empty signal indicates number of bytes not carrying data at the cycle when EOP becomes effective. The data bits not carrying data at each EOP cycle can't be used to transmit the start bytes of next packet.

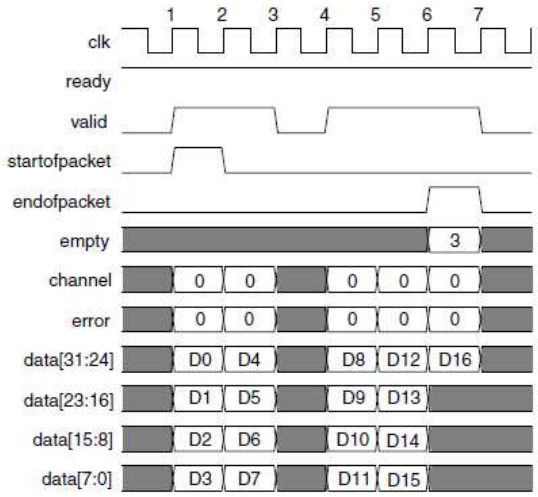
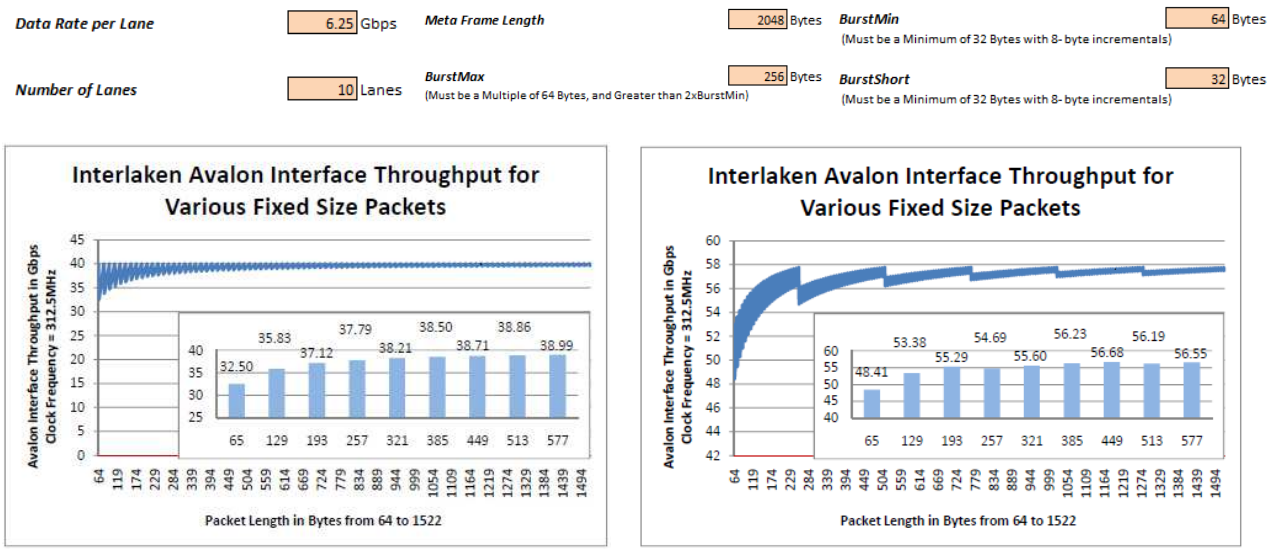


Figure 6. Avalon ST Interface for Packet Transfer

To transmit fixed length packet or cell, if the packet/cell length is multiple of Channel Width, the Avalon ST interface can achieve most throughput efficiency. The bottom right chart in worksheet of parameter configuration and throughput calculation section as shown in Figure 2 shows Avalon interface throughput when passing various fixed sized packets. Figure 7 shows two throughput examples when Avalon interface running at 312.5MHz, and ChannelWidth=128 vs. ChannelWidth=256. For design using 10 lanes @6.25Gbps and Avalon interface running at 312.5MHz, the worksheet shows no throughput difference for Avalon interface using ChannelWidth=256 or using ChannelWidth=512. So this worksheet helps user to select right ChannelWidth for their design to achieve less fabric resource utilization.



ChannelWidth =128Bits

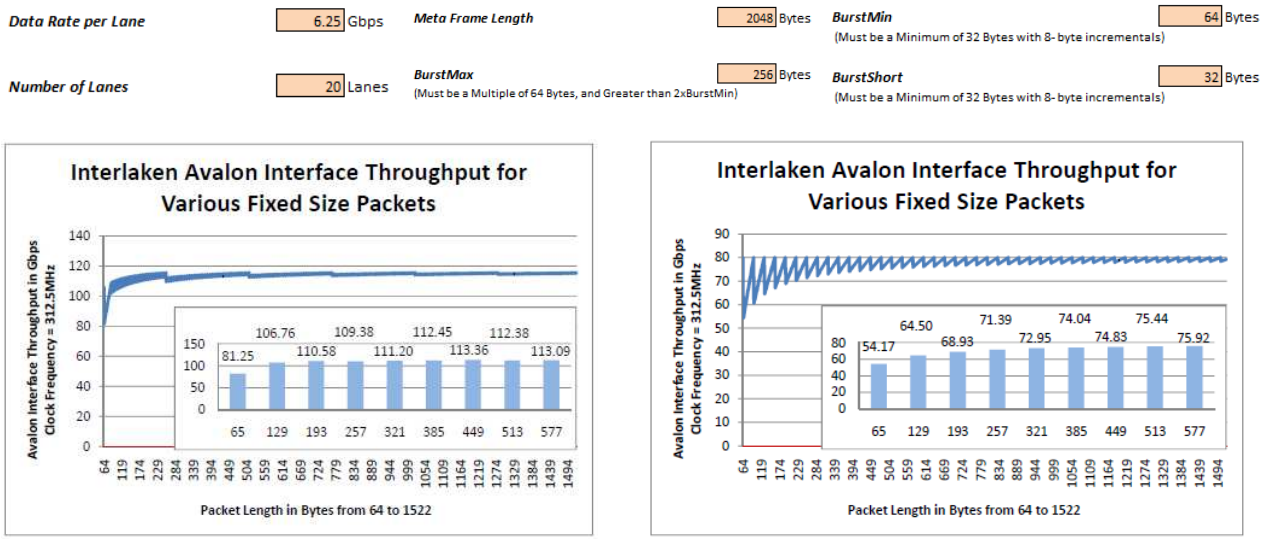
Avalon Interface Clock = 312.5MHz

ChannelWidth=256Bits

Avalon Interface Clock = 312.5MHz

Figure 7. Interlaken Avalon Interface Throughput for Various Fixed Size Packets running at 10 lanes @6.25Gbps

Figure 8 shows another two throughput examples when Avalon interface running at 312.5MHz, and ChannelWidth=512 vs. ChannelWidth=256. For design using 20 lanes @6.26Gbps and Avalon interface running at 321.5MHz, the worksheet shows the maximum throughput of Avalon interface is 80Gbps when ChannelWidth=256bits. This is not enough to keep up throughput requirement from MAC and transceiver lanes. ChannelWidth=512bits is desired configuration for 20 lanes @6.25Gbps.



ChannelWidth = 512Bits

Avalon Interface Clock = 312.5MHz

ChannelWidth = 256Bits

Avalon Interface Clock = 312.5MHz

Figure 8. Interlaken Avalon Interface Throughput for Various Fixed Size Packets running at 20 lanes @6.25Gbps

Worksheet Section for Cell Based/Fixed Size Packet Design

This worksheet section is designed for cell based/fixed size packets traffic application running on Interlaken interface. In Figure 1 40G packet over sonet example, the packets can be segmented into fixed length cells to pass traffic manager and switch fabric. This worksheet is designed to help balance user interface clock frequency and ChannelWidth. For same line rate configuration, higher ChannelWidth can achieve same throughput at slower clock frequency but cost higher fabric resource utilization, narrower ChannelWidth use less hardware resources but has to run at higher clock frequency to meet throughput requirement. The calculator provides information for different options, such as minimum required clock frequencies at ChannelWidth equals to 128, 256 and 512. However, this information does not infer that the MegaCore function can meet these frequencies. For example, Figure 9 shows a worksheet screenshot for 12 lanes @10.375Gbps. It is configured for fixed size packets that packet size is 65 bytes. The worksheet provides three reference clock frequencies for Avalon interface using 128, 256 and 512 bus ChannelWidth. The worksheet indicates that the Interlaken MegaCore function needs to run at an internal frequency of over 500 MHz if uses 128 bits ChannelWidth. This calculation result does not infer that the MegaCore function can run at over 500 MHz. For maximum clock frequency that fabric can run, please refer to Stratix device datasheet. The maximum fabric clock frequency

listed in device datasheet does not guarantee Interlaken MegaCore can achieve. For configuration shown in Figure 9, it is easier to close timing for 512 bits ChannelWidth running at 371MHz.

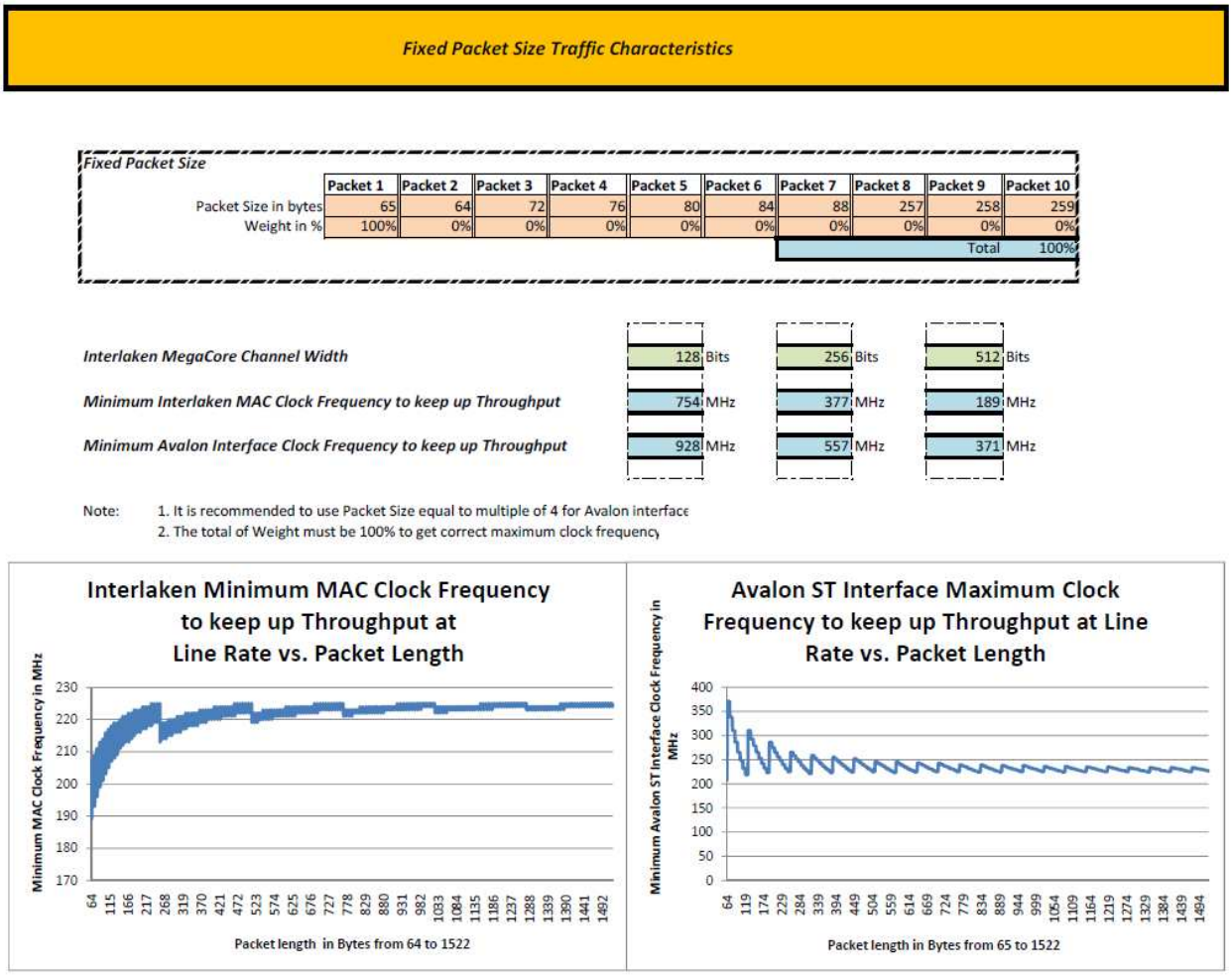


Figure 9. Worksheet screenshot for cell based/fixed size packets design

To use this worksheet, the Total showing the SUM of "Weight in %" for 10 different packet sizes must be 100% to get correct clock frequencies. If a user wants to set configuration for only one packet size, he only need to pick one cell space among 10 different Packet Size cells and give 100% under that cell space, 0% under non-selected cell space. This worksheet provides convenience for user design handling up to 10 different packet sizes simultaneously. One design example that handles a few amount of packet size variation is a traffic manager processes cell based traffic plus a small percentage of management cells in different size. Figure 10 gives an example of a design handling 95% 128-byte data traffic and 5% 64-byte management cells. The line rate for this example is 12lanes@10.375Gbps. The worksheet indicates that 256 bits ChannelWidth requires clock frequency more than 400MHz which is hard to close timing. The user interface clock frequency is less than 250MHz if ChannelWidth = 512 which is ideal for design handling 12lanes@10.375Gbps raw bandwidth.

Fixed Packet Size Traffic Characteristics

Fixed Packet Size

	Packet 1	Packet 2	Packet 3	Packet 4	Packet 5	Packet 6	Packet 7	Packet 8	Packet 9	Packet 10
Packet Size in bytes	128	64	72	76	80	84	88	257	258	259
Weight in %	95%	5%	0%	0%	0%	0%	0%	0%	0%	0%
									Total	100%

Interlaken MegaCore Channel Width	128 Bits	256 Bits	512 Bits
Minimum Interlaken MAC Clock Frequency to keep up Throughput	871 MHz	436 MHz	218 MHz
Minimum Avalon Interface Clock Frequency to keep up Throughput	871 MHz	436 MHz	218 MHz

Note: 1. It is recommended to use Packet Size equal to multiple of 4 for Avalon interface
2. The total of Weight must be 100% to get correct maximum clock frequency

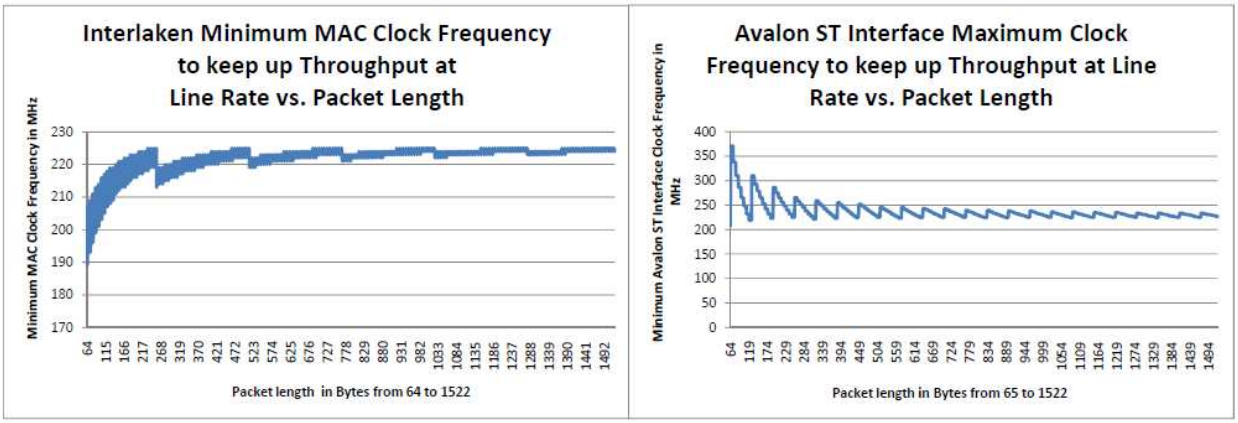


Figure 10. A 12 lanes@10.375Gbps configuration example for cell based traffic which pattern has 95% 128-byte data traffic and 5% flow control cells

Worksheet Section for Variable Size Packet with Random Weighted Distribution

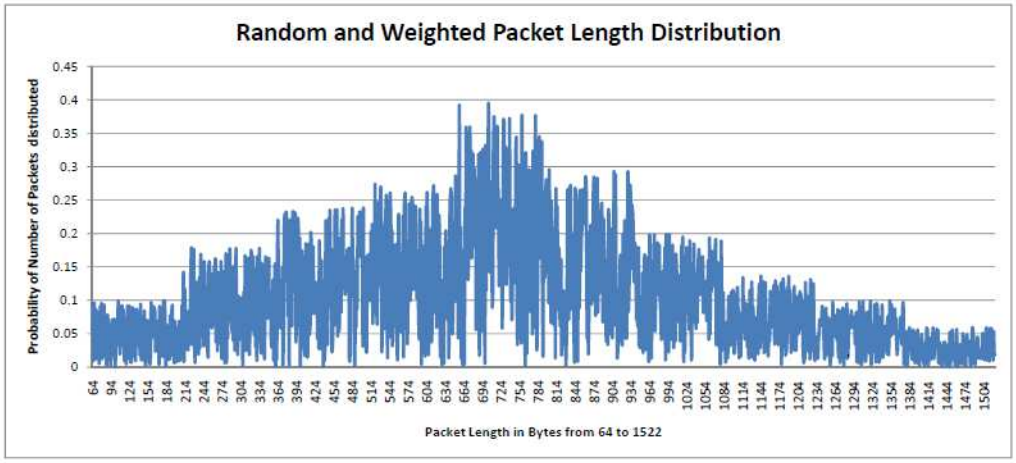
This worksheet section is designed for data traffic with variable packet sizes running on Interlaken interface. An example is 40G packet over SONET in Figure 1, the variable length packets coming from STS-768 framer, cross Interlaken chip-to-chip interface and processed by NPU. This worksheet provides random packet length distribution with user configurable weight. It provides reference user interface clock frequency vs. ChannelWidth for weighted random traffic pattern as shown in Figure 11. It allows user to enter ten different packet size range and weight for each range. The worksheet provides random distribution according to packet size range and weight. It also provides reference minimum clock frequency at Avalon interface in order to keep up throughput requirement for weighted random traffic pattern shown in worksheet. Three reference clock frequencies are provided for ChannelWidth = 128, 256 and 512 to help balance fabric resource utilization and ease of timing closure. Same as the worksheet for cell based data traffic, the reference clock frequencies provided in this worksheet does not guarantee

the FPGA device can run at such frequency or the MegaCore function can close timing at such frequency.

Configurable Random Weighted Packet Size Traffic Characteristics

Configurable Packet Size in Range

		Packet 1	Packet 2	Packet 3	Packet 4	Packet 5	Packet 6	Packet 7	Packet 8	Packet 9	Packet 10
Packet Size Range	Minimum	64	210	357	502	648	792	938	1084	1230	1376
Packet Size Range	Maximum	209	356	502	648	792	938	1084	1230	1376	1522
	Weight in %	5%	9%	12%	14%	20%	15%	10%	7%	5%	3%
										Total	100%



Interlaken MegaCore Channel Width	128 Bits	256 Bits	512 Bits
Minimum Interlaken MAC Clock Frequency to keep up Throughput	887 MHz	444 MHz	222 MHz
Minimum Avalon Interface Clock Frequency to keep up Throughput	887 MHz	444 MHz	235 MHz

Note: 1. It is recommended to use Packet Size equal to multiple of 4 for Avalon interface
2. The total of Weight must be 100% to get correct maximum clock frequency

Figure 11. An example of random packet size distribution with user configurable weight

Conclusion

This application note and accompanying worksheet calculator intend to provide user a configurable environment to determine parameters for throughput, user interface bus width and minimum clock frequency.