QUICK START GUIDE

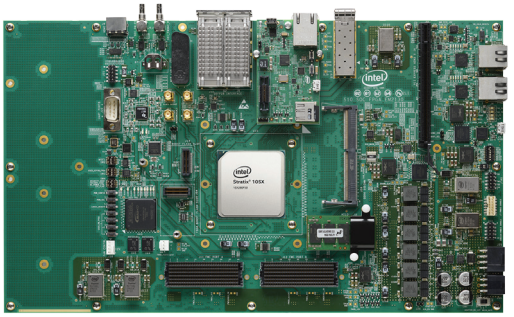
Intel® Stratix® 10 SoC Development Kit

A Complete Development Environment

Intel® Stratix® 10 SX SoC Board Features

- Intel Stratix 10 SX FPGA
  - Please refer to Intel site for exact device part number on this development kit
- Embedded Intel FPGA USB Download Cable II for hard processor system (HPS) or FPGA programming/debugging
- PCI Express* (PCIe*)
  - 1X Gen3 x16 root port
  - 2X Gen3 x16 end ports (need to use FMC+ ports to connect with PCIe cable)
- 2X 100GbE quad small form factor pluggable (QSFP) 28 ports (QSFP28) ports
- Dual FPGA mezzanine card (FMC+) expansion headers
- Two 10/100/1000 SGMII Ethernet ports[¤], one 10/100/1000 RGMII Ethernet port and one small form factor pluggable (SFP+) cage
- USB On-The-Go (USB OTG) port
- One High-Definition Multimedia Interface (HDMI)
- One serial digital interface (SDI) port[¤]

[¤] Intellectual property (IP) is not available in v18.0.



What's in the Box

- Intel Stratix 10 SoC development board
- 1X mini USB cable
- 1X micro USB cable
- 1X Ethernet cable
- HPS IO48 OOBE daughtercard
- Flash configuration daughtercards
  - 1X Quad SPI flash
  - 1X NAND flash
  - 1X MicroSD flash
- 2x FMC+ loopback daughtercards
- 1X DDR4 HILO memory card
- 1X DDR4 SoDIMM memory card
- Quick start guide

Available Resources

The following software and tools are available for download:

- Documentation
- Schematics and design files
- Intel Stratix 10 SoC Development Kit User Guide
- Intel SoC FPGA Embedded Development Suite (SoC EDS) User Guide
- Golden System Reference Design User Manual
- Design and development tools
- Intel SoC FPGA Embedded Development Suite, including ARM* Development
  - Studio 5* (DS-5*) Intel SoC FPGA Edition Toolkit
- Intel Quartus® Prime Pro Edition design software
- Design examples
- Golden System Reference Design

Verify Basic Operation

1. Attach the Ethernet cable on the HPS OOBE daughtercard's Ethernet jack (J3) to your network and the USB cable to the UART port J7 on the HPS OOBE daughtercard.
2. The MicroSD boot card is inserted into the J5 socket on the HPS OOBE daughtercard.
3. Connect the power adapter from an A/C outlet to J25 on the main board, then turn on the board using the power switch SW7.
4. The HPS begins booting the Golden System Reference Design Linux* image and the UART message is shown in the UART console window.
5. To obtain the IP address of the board, access the UART console window.
   a. Hit enter to get a login prompt and log in as root,
   b. Type “ifconfig” in the console window,
   c. IP address will show on line 3 (inet addr) if network is available,

```
root@stratix10:~# ifconfig
eth0      Link encap:Ethernet  HWaddr f2:0d:7d:43:ec:31
          inet addr:192.168.199.119  Bcast:192.168.199.255  Mask:255.255.255.0
          inet6 addr: fe80::f00d:7dff:fe43:ec31/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST DYNAMIC  MTU:1500  Metric:1
          RX packets:85 errors:0 dropped:0 overruns:0 frame:0
          TX packets:119 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:19518 (19.0 KiB)  TX bytes:14630 (14.2 KiB)
          Interrupt:5 Base address:0xc000

lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1/128 Scope:Host
          UP LOOPBACK RUNNING  MTU:65536  Metric:1
          RX packets:364 errors:0 dropped:0 overruns:0 frame:0
          TX packets:364 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1
          RX bytes:26814 (26.1 KiB)  TX bytes:26814 (26.1 KiB)

root@stratix10:~#
```

6. To see the Board Update Portal web server, open a browser, and type the IP address from the UART console into the URL field. The Board Update Portal web server allows you to verify operation of the board and the FPGA.

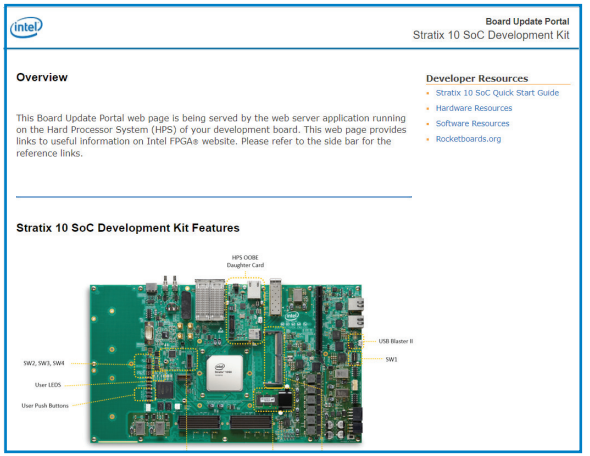


Figure 1. Board Update Portal

7. For additional Linux resources, browse to the rocketboards.org community portal and select the “Start” button.

Electromagnetic interference caused by any modification made to the kit contents is the sole responsibility of the user. This equipment is designated for use only in an industrial research environment.
Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

FCC NOTICE: This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under FCC Part 5 of CFR Title 47.