Intel® Stratix® 10 SoC Development Kit

A Complete Development Environment

Intel® Stratix® 10 SX SoC Board Features

- Intel Stratix 10 SX FPGA
  - Please refer to Intel site for exact device part number on this development kit
- Embedded Intel FPGA USB Download Cable II for hard processor system (HPS) or FPGA programming/debugging
- PCI Express* (PCIe*)
  - 1X Gen3 x16 root port
  - 2X Gen3 x16 end ports (need to use FMC+ ports to connect with PCIe cable)
- 2X 100GbE quad small form factor pluggable (QSFP) 28 ports (QSFP28) ports
- Dual FPGA mezzanine card (FMC+) expansion headers
- Two 10/100/1000 SGMII Ethernet ports*, one 10/100/1000 RGMII Ethernet port and one small form factor pluggable (SFP+) cage
- USB On-The-Go (USB OTG) port
- One High-Definition Multimedia Interface (HDMI)
- One serial digital interface (SDI) port*

* Intellectual property (IP) is not available in v18.0.

What's in the Box

- Intel Stratix 10 SoC development board
- 1X mini USB cable
- 1X micro USB cable
- 1X Ethernet cable
- HPS IO48 OOBEx daughterboard
- Flash configuration daughtercards
  - 1X Quad SPI flash
  - 1X NAND flash
  - 1X MicroSD flash
- 2x FMC+ loopback daughtercards
- 1X DDR4 HILO memory card
- 1X DDR4 SoDIMM memory card
- Quick start guide

Available Resources

The following software and tools are available for download:

- Documentation
- Schematics and design files
- Intel Stratix 10 SoC Development Kit User Guide
- Intel SoC FPGA Embedded Development Suite (SoC EDS) User Guide
- Design and development tools
- Intel SoC FPGA Embedded Development Suite, including ARM® Development
  - Studio 5® (DS-5®) Intel SoC FPGA Edition Toolkit
- Intel Quartus® Prime Pro Edition design software
- Design examples
- Golden System Reference Design
**Quick Start Guide | Intel Stratix 10 SoC Development Kit**

**Verify Basic Operation**

1. Attach the Ethernet cable on the HPS OOB daughtercard's Ethernet jack (J3) to your network and the USB cable to the UART port J7 on the HPS OOB daughtercard.

2. The MicroSD boot card is inserted into the J5 socket on the HPS OOB daughtercard.

3. Connect the power adapter from an A/C outlet to J25 on the main board, then turn on the board using the power switch SW7.

4. The HPS begins booting the Golden System Reference Design Linux* image and the UART message is shown in the UART console window.

5. To obtain the IP address of the board, access the UART console window.
   a. Hit enter to get a login prompt and log in as root,
   b. Type “ifconfig” in the console window,
   c. IP address will show on line 3 (inet addr) if network is available,

6. To see the Board Update Portal web server, open a browser, and type the IP address from the UART console into the URL field. The Board Update Portal web server allows you to verify operation of the board and the FPGA.

7. For additional Linux resources, browse to the rocketboards.org community portal and select the “Start” button.

---

**Electromagnetic interference caused by any modification made to the kit contents is the sole responsibility of the user. This equipment is designated for use only in an industrial research environment. Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.**

---

© Intel Corporation. All rights reserved. Intel, the Intel logo, the Intel Inside mark and logo, the Intel. Experience What’s Inside mark and logo, Altera, Arria, Cyclone, Enpirion, Intel Atom, Intel Core, Intel Xeon, MAX, Nios, Quartus and Stratix are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. *Other marks and brands may be claimed as the property of others. Intel reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.