QUICK START GUIDE

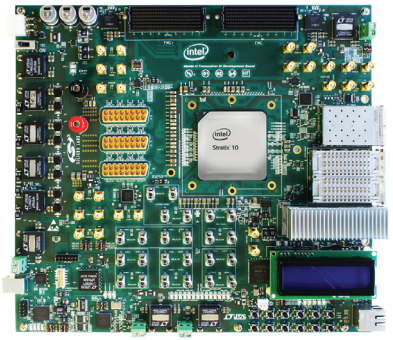
Transceiver Signal Integrity Development Kit, Intel® Stratix® 10 GX Edition

A Complete Development Platform for Prototyping

Introduction

Intel's Transceiver Signal Integrity Development Kit, Intel® Stratix® 10 GX Edition helps you thoroughly evaluate the signal integrity of Intel Stratix 10 GX FPGA transceivers. With this kit, you can:

- Evaluate transceiver performance
- Generate and check pseudo-random binary sequence (PRBS) patterns via an easy-to-use GUI
- Dynamically change differential output voltage (VOD), pre-emphasis, and equalization settings to optimize transceiver performance for your channel
- Perform jitter analysis
- Verify physical medium attachment (PMA) compliance to PCI Express*(PCIe*), Gigabit Ethernet (GbE), XAUI, CEI-6G, Serial RapidIO*, high-definition serial digital interface (HD-SDI), and other major standards



What's in the Box

- **Hardware**
  The development kit includes the following hardware:
  - Intel Stratix 10 GX Signal Integrity board
  - Six full-duplex transceiver channels with 2.4 mm SMA connectors
  - 24 full-duplex transceiver channels to FMC+ A connector
  - 16 full-duplex transceiver channels to FMC+ B connector
  - Four full-duplex transceiver channels to CFP4 optical interface
  - Four full-duplex transceiver channels to each QSFP+ 0 and QSFP+ 1 optical interfaces
  - Single transceiver channel to both SFP+ 0 and SFP+ 1 optical interfaces
  - Four full-duplex transceiver channels to each MXP 0, MXP 1, and MXP 2 high-density connectors
  - LCD
  - Ethernet PHY
  - AC adapter power supply and 24-pin to 6-pin power adapter cable
  - Intel FPGA Download Cable
  - FMC+ loopback daughtercard
  - Ethernet cable

Downloadable Content

- **Software**
  Download and install the Intel Stratix 10 GX FPGA Development Kit installer to obtain the following items:

  Design examples
  - Board Update Portal design
  - Board Test System (BTS)design

  Documentation
  - Intel Stratix 10 GX FPGA Development kit user guide
  - Board design files

  Dowload and install design software
  - Intel Quartus® Prime software (required)
  - Nios® II processor (optional)
  - Mentor Graphics* ModelSim*-Intel FPGA software (optional)

You can download the kit installer directly from
www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/kit-s10-transceiver-si.html

Using the Board Update Portal

The Board Update Portal design example in this kit facilitates easy development kit software and board flash memory updates, allowing you to:

- Access useful information on www.intel.com/content/www/us/en/products/programmable.html, including updated software and design examples
- Load designs into the flash memory on your board

The following steps ensure that you have the latest software on your computer and board. The Board Update Portal design example—which consists of a Nios® II embedded processor, an Ethernet media access control (MAC), and a web page—is stored in the "factory" portion of your board's flash memory. The source for this design is released with the development kit software. When your board is connected to the network, the Nios II processor obtains an Internet protocol (IP) address and allows you to interface with your board over the network through the web page.

Before you proceed, ensure that you have the following:

- A computer connected to a working Ethernet port on a DHCP-enabled network
- A separate working Ethernet port connected to the same network for your board
- The Ethernet, power cables, and development board included in your kit

Step 1. Connect to the Board Update Portal

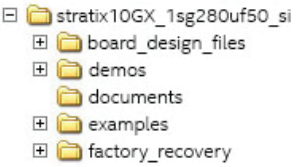
1. With the board powered down, set the dipswitch SW6.1 to the OFF position.
2. Attach the Ethernet cable from the board to your network hub.
3. Power up the board. The LCD displays "Connecting" as it connects to your network server (may take a couple of minutes). It then obtains an IP address, which is displayed on the board's LCD.
4. Launch a web browser on a computer that is connected to the same network, and type the IP address displayed on the LCD in the address bar. The Board Update Portal web page appears on your screen.
5. Click on "Signal Integrity Development Kit" link and ensure you have the latest version of the development kit software. The version is displayed in the "Downloads" section of the website.
6. Download any designs that interest you to your computer. Check this website often for new designs and for updates to existing designs and documentation.
7. If necessary, download the latest Intel® software tools (Intel Quartus Prime software, Nios II processor, and intellectual property functions). This development kit comes with an IntelQuartus Prime software license.

If you cannot connect to the Board Update Portal, go to www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/kit-s10-transceiver-si.html to ensure that you have the latest development kit software.

Step 2. Download the development kit software

Download the latest development kit software tools from www.intel.com unzip the software package to anywhere on your computer.

Directory Structure



Step 3. Use the Board Update Portal to update your board and load the Transceiver Signal Integrity Demonstration

The Board Update Portal allows you to download new FPGA configurations to the "user" portion of the board's flash memory. If you cannot connect to the Board Update Portal, refer to the kit's user guide for other options to update the flash memory.

If you downloaded a new version of the development kit software, follow these steps to update your board:

1. Type the IP address shown on the board's LCD into your PC's web browser to display the Board Update Portal web page.
2. In the **Hardware File Name** field, specify the **.flash** file (<installation **stratix10GX_1sg280uf50_si\examples\board_test_system\qts_sma\qts_sma.flash**) that you downloaded from the website. The design does not have a software component, so leave the **Software File Name** field blank.
3. Click **Upload**.
4. Reconfigure the FPGA with the new files by changing switch SW6.1 to the ON position, then repowering your board or pushing MAX_RESETn (S12) to reconfigure the FPGA.

The demonstration design should now be running in the FPGA.

The Board Update Portal can also be used to upload your custom designs. The kit's user guide describes how to prepare your designs for use with the Board Update Portal.

Using the Transceiver Signal Integrity Demonstration

The Transceiver Signal Integrity Demonstration consists of a Java-based GUI and an FPGA design. After updating your board as described in Step 3, your board's FPGA contains the Transceiver Signal Integrity Demonstration design, which communicates with the GUI through the embedded Intel FPGA Download Cable on the board. To run the demonstration follow these steps:

1. Connect the Intel FPGA Download Cable from your PC to the board.
2. If the Intel FPGA Download Cable driver is not installed on your PC, install the driver using the instructions in the user guide.
3. Connect 2.4 mm SMA cables from one or more channels on the board to an oscilloscope capable of displaying the data rates you wish to observe. Make sure SW6.1 is set to ON position and power up the board.
4. Launch the **BoardTestSystem.exe** file, located at **stratix10GX_1sg280uf50_si\examples\board_test_system**. For optimal viewing, your screen resolution must be 1024x768 or greater.
5. Set PMA options in the Transceiver Channel Controls section.
6. Observe the resulting eye diagram on the oscilloscope and monitor the link statistics shown on the screen.

For information on bit error rate (BER) calculation, equalization settings, and other details regarding this demonstration, refer to the user guide. Visit the Transceiver Signal Integrity Development Kit page (www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/kit-s10-transceiver-si.html) for the latest documentation and designs.

Related Links

Kit-specific Resources

- Transceiver Signal Integrity Development Kit homepage
  www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/kit-s10-transceiver-si.html
- Transceiver Portfolio
  www.intel.com/content/www/us/en/products/programmable/fpga/stratix-10/features.html
- Intel Stratix 10 FPGAs
  www.intel.com/content/www/us/en/products/programmable/fpga/stratix-10.html

General Design Resources

- Board Design Resource Center
  www.intel.com/content/www/us/en/programmable/support/support-resources/support-centers/board-design-guidelines.html
- Licensing
  www.intel.com/content/www/us/en/programmable/support/support-resources/support-centers/licensing.html
- Software Download Center
  www.intel.com/content/www/us/en/programmable/downloads/download-center.html
- Technical Support Center
  www.intel.com/content/www/us/en/programmable/support/support-resources.html
- Development Kits
  www.intel.com/content/www/us/en/programmable/products/development-kits/kit-index.html
- Intel FPGA Community
  forums.intel.com

Electromagnetic interference caused by any modification made to the kit contents is the sole responsibility of the user. This equipment is designated for use only in an industrial research environment.
Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

CE

FCC NOTICE: This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under FCC Part 5 of CFR Title 47.

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