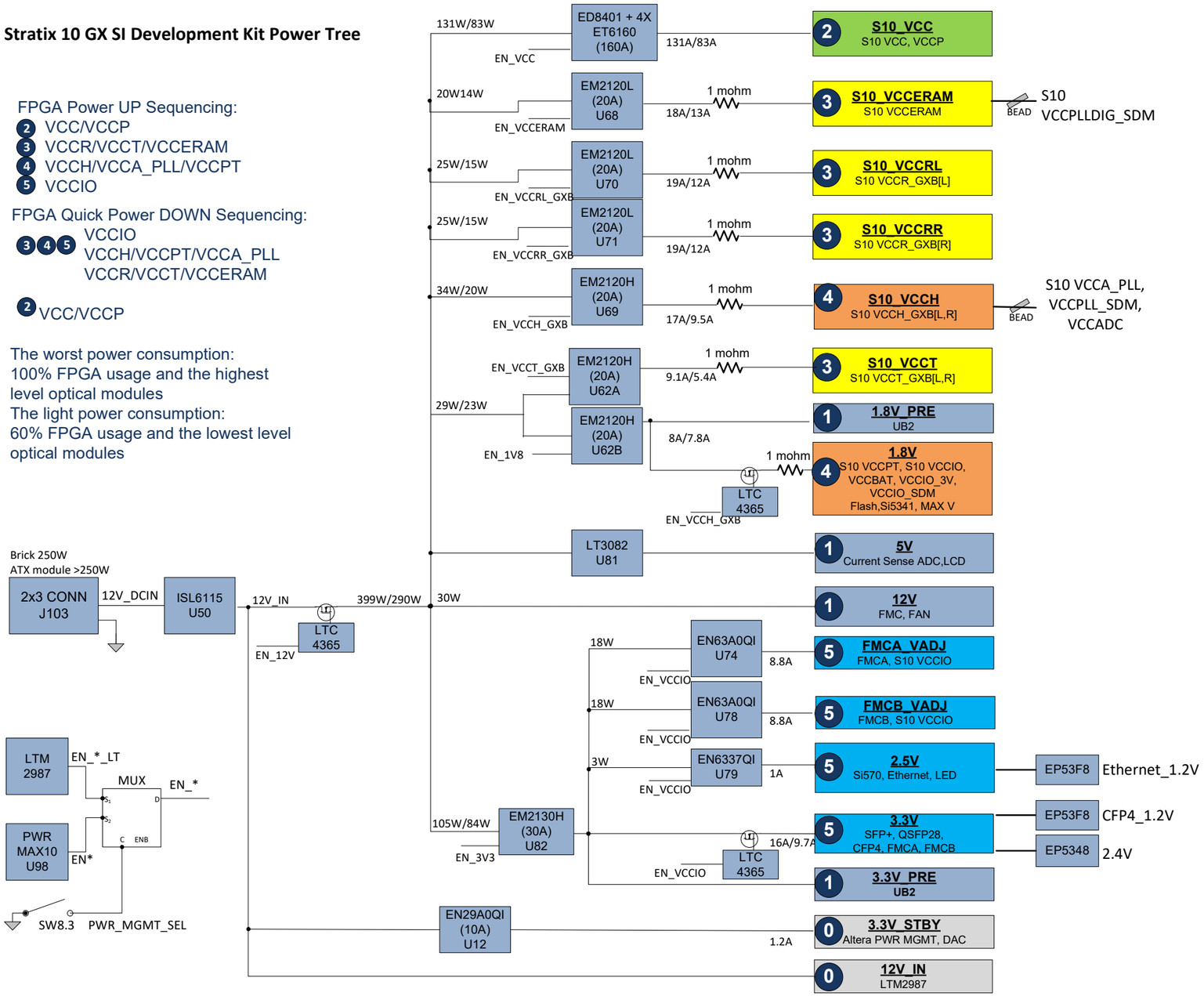
Stratix 10 GX SI Development Kit Power Tree

FPGA Power UP Sequencing:
- 2 VCC/VCCP
- 3 VCCR/VCCT/VCCERAM
- 4 VCCH/VCCA_PLL/VCCPT
- 5 VCCIO

FPGA Quick Power DOWN Sequencing:
- 3 4 5 VCCIO VCCH/VCCPT/VCCA_PLL VCCR/VCCT/VCCERAM
- 2 VCC/VCCP

The worst power consumption:
100% FPGA usage and the highest level optical modules
The light power consumption:
60% FPGA usage and the lowest level optical modules



Stratix 10 GX SI Development Kit Power Up/Down Sequence