Pre-Release Schematic
DO NOT COPY

NOTES:

1. Project Drawing Numbers:
   - Raw PCB: 100-0330632-A1
   - Fabric Plot: 110-0330632-A1
   - PCB Design Files: 120-0330632-A1
   - Fabric Drawing: 130-0330632-A1
   - Schematic Drawing: 140-0330632-A1
   - Bill of Materials: 150-0330632-A1
   - Schematic Design Files: 160-0330632-A1
   - Functional Specification: 170-0330632-A1
   - PCB Layout Guidelines: 220-0330632-A1
   - Assembly Notes: 230-0330632-A1

2. This board was designed for Stratix 10 SoC Development Kit.

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**PREL RELEASE SCHEMATIC**

**DATE**

**DESCRIPTION**

A initial schematic release

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**PAGE**

**DESCRIPTION**

1. Title
2. IO48 Connector
3. RGMII Ethernet
4. USB2.0 OTG
5. Micro SD Card
6. US220UART
7. Mictor, PBs, LEDs
8. Power

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- IO48 Connector
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**PAGE**

**DESCRIPTION**

1. Page Description, revision history

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Current limit for Rseti of 137k is 1.01A

Place R63 as close as possible to USB3320

Place C39 near the USB connector

RESETB must be held low until the VDD18 and VDDIO supplies are stable

USB Current Limit
The B-side pullup resistors should be sized according to signal frequency and current limits.
Notes:
LED is ON when HPS_LEDx is high
LED is OFF when HPS_LEDx is low
12V -> 5V/3.3V

Output Voltages:
- 3.3V/1A (Max.)
- 5V/1.1A (Max.)

Components:
- R456: 13.3K
- C900: 47uF
- C921: 0.01uF
- R668: 0
- R669: 8.25K
- R612: 1.00K
- C922: 0.01uF
- C896: 10uF
- R670: 0
- U15: LTM4622EY
- VOUT2_1
- A1
- VOUT2_2
- B1
- VOUT1_1
- D1
- VOUT1_2
- E1
- VIN1
- A2
- VIN2
- E2
- VIN3
- B3
- VIN4
- D3
- INTVCC
- C3
- GND1
- C1
- GND2
- C2
- GND3
- B5
- GND4
- D5
- RUN1
- D2
- RUN2
- B2
- TRACK/SS1
- E3
- TRACK/SS2
- A3
- FB1
- E4
- FB2
- A4
- PGOOD1
- D4
- PGOOD2
- B4
- COMP1
- E5
- COMP2
- A5
- FREQ
- C4
- SYNC/MODE
- C5