NOTES:
1. Project Drawing Numbers:
   - Raw PCB: 100-0330633-A1
   - Bill of Materials: 170-0330633-A1
   - Schematic Drawing: 180-0330633-A1
   - Gerber Files: 210-0330633-A1
   - Assembly Drawing: 320-0330633-A1
   - PCB Layout Guidelines: 220-0330633-A1

2. This board was designed for Stratix 10 SoC Development Kit.

Pre-Release Schematic
DO NOT COPY

2. This board was designed for Stratix 10 SoC Development Kit.

- NAND/eMMC (IO48)
- RGMII Ethernet
- NAND/SLC
- Microchip KSZ9001EX 10/100/1000Mbit Ethernet PHY
- FT232R
- UART-USB
- 25MHz OSC
- GPIO (IO48)
- Power
- PBs, LEDs

Only one works at the same time

Notes:
2. This board was designed for Stratix 10 SoC Development Kit.
Used in S10 Check out board

Reset FPGA logic externally by HPS

Update external watchdog for HP
When LOCK is HIGH during power-up, the BLOCK LOCK function is enabled. When LOCK is LOW during power-up, the BLOCK LOCK function is disabled.

Socketable: Ironwood SG-BGA-6367
LED, PushButton, CLK

Notes:
LED is ON when HPS_LEDx is high
LED is OFF when HPS_LEDx is low
12V -> 3.3V

- **VCC 12V**
- **LT_INTVCC**
- **VCC 3.3V**
- **3.3V/1A (Max.)**

**Components:****
- **U15**: LTM4623EY#PBF
- **D1, D2, D3, D4, D5**: VOUT_1, VOUT_2, VOUT_3, VOUT_4, VOUT_5
- **E1, E2, E3**: FB, ClockOUT, MODE
- **B1, B2, B3, B4**: GND_1, GND_2, GND_3, GND_4
- **A1, A2, A3, A4**: TRACK/SS, PHMODE, RUN, R5275 DNI
- **C922, C900, C949, C76**: C1, C2, C3, C4
- **R667, R5259**: R521, R522
- **C917**: 10uF
- **R668**: 1.00K
- **5.6uF**: 100pF
- **3.3V**: 0.01uF

**Labels:**
- VCC - Continuous Mode
- GND - Discontinuous Mode
- Soft-start time~1ms

**Notes:**
- **R667**: 324K
- **C922**: 10uF
- **R668**: 0.01uF
- **C76**: 47uF
- **R667**: 13.3K
- **C949**: 2.2uF
- **R5259**: 1.00K

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**Title:**
HPS IO48 NAND Daughter Card

**Document Information:**
- **Rev**: A1
- **Date**: Wednesday, April 19, 2017
- **Sheet**: 7 of 7

**Revision History:**
- **Rev A1**