Cyclone V SoC FPGA Development Kit Board

1. Project Drawing Numbers:
   - PCB Design File: 110-0321003-E1
   - Bill of Materials: 110-0321003-E1
   - Schematic Design File: 110-0321003-E1
   - PCB Layout Guidelines: 200-0321003-E1
   - Assembly Rele 520-0321003-E1

2. Notes:
   - Title, Notes, Block Diag, Rev. History
   - 1024MB DDR3 + ECC
   - Cyclone V GX SoC Clocks
   - Cyclone V GX SoC Configuration
   - 1024MB DDR3 (x32) - FPGA
   - 1024MB DDR3 (x32 + ECC) - HPS
   - QSPI FLASH & RESET Circuit
   - USB2.0 & Micro SD Card
   - UART, CAN
   - Power 1.1V_HPS, 5.0V, 1.8V
   - On-Board USB Blaster II
   - FPGA Power Monitor
   - HPS Power Monitor
   - Power 1 - DC I/P & 12V, 3.3V O/P
   - Power 2
   - Power 3 - 1.5V FPGA
   - Power 3 - 2.5V HPS
   - Power 3 - 1.5V & 1.5V HPS
   - Power 3 - 3.3V HPS
   - Power 3 - Power 6 & Temp Monitor
   - Power 4 - Linear Regulators
   - Power 5 - CycloneV GX SoC Power
   - Power 6 - CycloneV GX SoC Ground
   - Decoupling
   - Changes History

3. Title, Notes, Block Diag, Rev. History
   - Cyclone V GX SoC Bank 3,4
   - Cyclone V GX SoC Bank 5,6
   - Cyclone V GX SoC Bank 7
   - Cyclone V GX SoC Bank 8
   - Cyclone V GX SoC Transceiver Banks
   - Cyclone V GX SoC Clocks
   - Cyclone V GX SoC Power
   - Cyclone V GX SoC Ground

4. Copyright Information
   - Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121
   - Copyright (c) 2013, Altera Corporation. All Rights Reserved.
### I/O Bank Usage

<table>
<thead>
<tr>
<th>I/O Bank</th>
<th>Usage</th>
<th>VCCIO Voltage</th>
<th>VREF Voltage</th>
<th>VCCPD Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>B2L</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>B3L</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>B4L</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>3A</td>
<td>28 / 32 (88%)</td>
<td>2.5V</td>
<td>2.5V</td>
</tr>
<tr>
<td>5</td>
<td>3B</td>
<td>43 / 48 (90%)</td>
<td>1.5V</td>
<td>0.75V</td>
</tr>
<tr>
<td>6</td>
<td>4A</td>
<td>58 / 80 (73%)</td>
<td>1.5V</td>
<td>0.75V</td>
</tr>
<tr>
<td>7</td>
<td>5A</td>
<td>25 / 32 (78%)</td>
<td>2.5V</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>5B</td>
<td>13 / 16 (81%)</td>
<td>2.5V</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>6B</td>
<td>34 / 45 (76%)</td>
<td>1.5V</td>
<td>0.75V</td>
</tr>
<tr>
<td>10</td>
<td>6A</td>
<td>48 / 57 (84%)</td>
<td>1.5V</td>
<td>0.75V</td>
</tr>
<tr>
<td>11</td>
<td>7A</td>
<td>19 / 19 (100%)</td>
<td>3.3V</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>7B</td>
<td>20 / 22 (91%)</td>
<td>3.3V</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>7C</td>
<td>12 / 12 (100%)</td>
<td>3.3V</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>7D</td>
<td>12 / 14 (86%)</td>
<td>3.3V</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>8A</td>
<td>74 / 80 (93%)</td>
<td>2.5V</td>
<td></td>
</tr>
</tbody>
</table>

**Top View - Wire Bond**

**Cyclone V - 5CSXFC6D6F31C7**
Cyclone V GX SoC Configuration

USER I/O INTERFACES

2.5V BANK

FPGA_nSTATUS
FPGA_CONFIG_D7
FPGA_CONFIG_D0
FPGA_CONFIG_D1
FPGA_CONFIG_D2
FPGA_CONFIG_D3
FPGA_CONFIG_D4
FPGA_CONFIG_D5
FPGA_CONFIG_D6
FPGA_CONF_DONE
FPGA_CONFIG_D8
FPGA_CONFIG_D9
FPGA_CONFIG_D10
FPGA_CONFIG_D11
FPGA_CONFIG_D12
FPGA_CONFIG_D13
FPGA_CONFIG_D14
FPGA_CONFIG_D15

Title
Size Document Number Rev
Date: Sheet

Cyclone V SoC FPGA Development Kit Board

B

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121
Copyright (c) 2013, Altera Corporation. All Rights Reserved.
- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.
QSPI Flash & Reset Circuit

QSPI FLASH

RESET CIRCUIT

USB_RESET is active HIGH and is inverted through the MAX II system controller.

Input only to CV device cold reset

Input/output to CV device warm reset

3.3V PLACE NEAR QSPI FLASH
### USB 2.0 OTG, Micro SD Card

<table>
<thead>
<tr>
<th>RSET (kΩ)</th>
<th>TYPICAL CURRENT LIMIT/THRESHOLD (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>91.78</td>
<td>1500</td>
</tr>
<tr>
<td>121</td>
<td>1145</td>
</tr>
<tr>
<td>221</td>
<td>632</td>
</tr>
<tr>
<td>301</td>
<td>466</td>
</tr>
<tr>
<td>422</td>
<td>333</td>
</tr>
<tr>
<td>563.12</td>
<td>250</td>
</tr>
<tr>
<td>∞ (Open)</td>
<td>0</td>
</tr>
</tbody>
</table>

#### Current limit is set to 1.1 A

### USB INTERFACE

#### Micro SD Card

- Part Number: MAX14523AATA+T
- Manufacturer: Maxim Integrated Products, Inc.

#### Micro SD / USB INTERFACE

- SD_CLK
- SD_CMD
- SD_DAT0
- SD_DAT1
- SD_DAT2
- SD_DAT3
- SD_DIR
- SD_ID
- SD_MAX
- SD_SD
- SD_STP
- SD_RESET
- SD_VDD
- USB_5.0V
- USB_ID
- USB_DP_P
- USB_DM_N
- USB_DATA[7..0]
- USB_NXT
- USB_DIR
- USB_STP
- USB_RBIAS
- USB_RESET_PHY
- USB_RESET
- USB_VDD
- USB_VDDA
- USB_VDD3.3
- USB_VDD1.8
- USB_EXTVBUS
- USB_RESET_PHY
- USB_RESET
- USB_VDD
- USB_VDDA
- USB_VDD3.3
- USB_VDD1.8
- USB_EXTVBUS

#### Schematic Diagram

- Place near USB3300

- USB 2.0 OTG

- Current limit is set to 1.1 A

- R730 is leakage path for 3.3V_SD rail, share footprint with C4

- QSPI_RESETn

- X2 24MHz
These GND connections to each VSENSEMx pin needs to be placed close to a GND pin of the BGA!
There are totally 11x22μF buck caps on 12V rail, the value of C78 needs to be set based on this.

There are totally 2x22μF+2x47μF buck caps on DC_IN rail, the value of C78 needs to be set based on this.
Power 2

R590 and R665 resistors should be close to each other.

Place this SENSE PAD close to SOC.
Power 3 - 2.5V HPS
<table>
<thead>
<tr>
<th>REV</th>
<th>DATE</th>
<th>PAGES</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>E1</td>
<td>7/11/2014</td>
<td>28</td>
<td>Add two Hot-Plug controller circuits (LTC4218).</td>
</tr>
<tr>
<td></td>
<td>7/11/2014</td>
<td>29</td>
<td>When 12V_ATX is using, disable LTC3855's 12V_REG by SW.</td>
</tr>
<tr>
<td></td>
<td>7/11/2014</td>
<td>38</td>
<td>Generate ENABLE signal using resistor divider circuit for all Empirion parts.</td>
</tr>
<tr>
<td></td>
<td>7/11/2014</td>
<td>39</td>
<td>Replace EN23F0QI with EN23F2QI, EN2340QI with EN2342QI.</td>
</tr>
<tr>
<td></td>
<td>7/11/2014</td>
<td>40</td>
<td>Put option for enabling voltage on internal 1.1V regulator in SW.</td>
</tr>
<tr>
<td></td>
<td>7/11/2014</td>
<td>41</td>
<td>Change switching frequency of EN23FQI (1MHz-2MHz)</td>
</tr>
<tr>
<td></td>
<td>7/11/2014</td>
<td>42</td>
<td>Add some buffer such as using 1 to 1 VCC rel. only use MAX66053, 1209, and 1219.</td>
</tr>
<tr>
<td></td>
<td>7/11/2014</td>
<td>43</td>
<td>Change all C11 to 1.1V.</td>
</tr>
<tr>
<td></td>
<td>7/11/2014</td>
<td>44</td>
<td>Put option to change the HPS power management chip.</td>
</tr>
<tr>
<td></td>
<td>7/11/2014</td>
<td>45</td>
<td>Add some buffer such as using 1 to 1 VCC rel. only use MAX66053, 1209, and 1219.</td>
</tr>
<tr>
<td></td>
<td>7/11/2014</td>
<td>46</td>
<td>Change all C11 to 1.1V.</td>
</tr>
<tr>
<td></td>
<td>7/11/2014</td>
<td>49</td>
<td>Change R588 to 46.4K for EN23F2QI parts which has data code U418 or higher.</td>
</tr>
<tr>
<td></td>
<td>7/15/2014</td>
<td>50</td>
<td>Update 5CSXFC6D_F 896 schematic symbol on HPS_GPIO[13:0] and VCCRSTCLK_HPS.</td>
</tr>
<tr>
<td></td>
<td>8/01/2014</td>
<td>51</td>
<td>Move R137/R135 to the right side of R138/R136.</td>
</tr>
<tr>
<td></td>
<td>8/01/2014</td>
<td>52</td>
<td>Change all R137 to 56k.</td>
</tr>
<tr>
<td>8/29/2014</td>
<td>54</td>
<td>24</td>
<td>Replace R721 with 1K. Replace C6 with 100ohm resistor.</td>
</tr>
</tbody>
</table>

**Note:** The changes are minor and are aimed at improving the functionality and reliability of the system.