

# FMC-200 Programmable Camera Interface Hardware Manual



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0.1	June 30, 2010	Initial revision.
0.2	July 2, 2010	Updated various cross references. Added Table 3-1. Added additional bit assignment details to tables 6-3, 6-4, 6-5.
0.3	June 21, 2011	Updated to reflect increase in fmc_vclk to 90 MHz
0.4	November 1, 2011	Revert the fmc_vclk back to 85 MHz coupled with a change that eliminates sending all but one interval of non-image data used to indicate an end of line or end of frame condition.
0.5	August 21, 2012	Added Figure 2-2, Figure 6-2

**Table 1-1 Document Revision History**

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## Chapter 1. Introduction

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The FMC-200 is a FPGA Mezzanine Card (VITA 57.1) providing a high performance yet flexible Camera Link compliant connection. It is ideally suited to industrial, scientific, defense, and aerospace applications demanding high speed and/or real time data processing of image data.

The on-board Altera Cyclone® III FPGA can be reconfigured to capture video from a variety of cameras including a single Base, Medium, Full or Extended (80-bit) configuration camera; or two Base configuration cameras. Application specific data pre-processing or proprietary protocols are easily accommodated via customization of the on-board FPGA. Image data is presented to the FMC Carrier in a memory mapped pixel format abstracting away the details of the Camera Link connections.

FMC-200 build options include switchable SafePower PoCL, supporting both conventional and PoCL Camera Link cameras as well as the option for programmable external LVCMOS/Differential input and output signals for event synchronization.



## Chapter 2. FMC-200 Overview

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### 2.1 FMC-200 Product Family Features

- Camera Link v1.2 Base, Medium, and Full configurations, plus extended and Dual-Base configurations
- FMC VITA 57.1 Compliant, Low Pin Count Connector (LPC)
- Power Over Camera Link (PoCL) SafePower v1.2 support
- 7.14 Gbit/sec Camera Link Interface
- 7.48 Gbit/sec FMC Interface
- Acquisition pixel clock rates up to 85MHz and higher depending on image framing parameters
- Supports all Camera Link pixel assignment configurations
- Real-time data transfers to FMC Carrier
- On-board Altera Cyclone III FPGA (EP3C16) for card customization and remote system upgrade
- Altera FPGA can be downgraded in size to EP3C10 or EP3C5 for lower cost/power solutions
- On-board Altera EPCS16 Serial EEPROM allows for storage of up to 8 FPGA images (configurations)
- In-System reprogramming of FPGA configuration EEPROM through FMC JTAG or Register Interface
- Front bezel contains additional general purpose connector providing (2) single ended signals (2.5V) and (2) differential pairs (LVDS)
- Card contains a general purpose ribbon cable header connector providing (4) differential pairs (LVDS)
- Flexible clocking options—on card oscillator, FMC carrier provided clock, or Camera Link clock

## 2.2 FMC-200 Functional Blocks

The major components of the FMC-200 circuit board are shown in **Figure 2-1 FMC-200 Block Diagram**.

The blocks include:

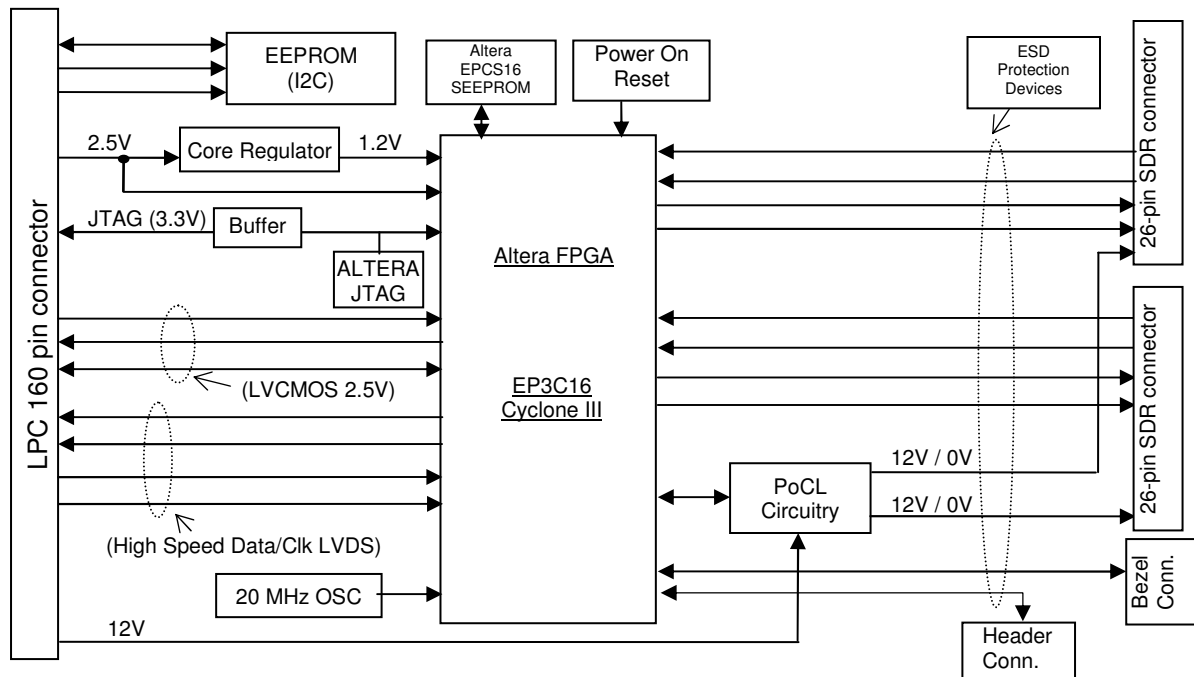
- FPGA
- Power over Camera Link (PoCL) circuitry
- Serial EEPROMs for holding IPMI data and FPGA configuration images
- Oscillator
- Core regulator
- Connectors

The front panel contains:

- Two 26-pin SDR format standard camera link connectors.
- Micro connector providing general-purpose IO signals which are routed to FPGA pins.

The FMC-200 board contains:

- FMC compliant 160-pin low pin count connector for interfacing to the carrier board.
- Standard ribbon cable header providing 4 general-purpose LVDS pairs, routed to FPGA pins.
- Pads for an optional Altera JTAG header



**Figure 2-1 FMC-200 Block Diagram**





## 2.2.1 FMC Interface

The FMC interface consists of a 160 pin, VITA 57.1 compliant, Low Pin Count Connector (LPC). Region of interest image data received from the Camera Link interface is serialized at a factor of 8:1 over 11 LVDS channels on the FMC connector to the carrier board. Data is transferred to the carrier board using an internally generated 85 MHz clock. The serialized data has a per-pin data rate of 680Mbit/sec (8 x 85MHz), yielding a total bandwidth of 7.48 Gbit/sec (11 channels x 680Mbit/sec). With 11 LVDS channels serialized at 8:1, 88 parallel bits are serialized per transfer clock from the FMC-200 down to the carrier. The camera link interface can provide a maximum of 84 data bits for every one of its transfer clocks (80 bits of image data, plus 4 valid signals). This means the FMC interface contains 4 “spare” bits per transfer clock that can be driven by the FPGA with additional data or image tags.

A parallel microprocessor type synchronous data bus connection to the on-board FPGA is used by the FMC Carrier to configure, monitor, and actively participate in the Camera Link activities. The data bus has separate 5 bit address and 8 bit data lines along with the clock, enable, read/write, and interrupt lines. The speed of the synchronous data bus is defined by the FMC Carrier’s output clock which can be up to 80 MHz.

Additional high speed LVDS and lower speed single ended general purpose I/O connections to the onboard FPGA are available on the FMC connector. These lines can be used by the FMC Carrier FPGA for low latency control and status operations which may be required for custom applications.

The FMC-200 also supports the standard FMC connector functionality for IPMI and optional JTAG access of the onboard FPGA.

## 2.2.2 Camera Link Interface

The two front bezel 26-pin SDR connectors provide the interface to Camera Link v1.2 type devices. Camera Link devices transmit serialized 7:1 data over 4 differential lines per link. A base configuration camera has one link which is used for video data and the qualifying valid signals (data, line, frame). The medium configuration expands this by 1 additional link on a second 26-pin connector; the full configuration by another link on the second connector. Dedicated differential lines on each link contain a clock used as a sampling reference for the other 4 data lines. The Camera Link specified maximum frequency of these parallel clocks is 85MHz. With a 7:1 x 4 transmission protocol, this corresponds to 28 bits of data transmitted per parallel clock. For the full Camera Link configuration, there are 28bits x 3 = 84 bits transmitted per clock. The **maximum data rate from the Camera Link interface is (84bits)\*(85MHz) = 7.14Gbit/sec.**

The frequency of the **data signals received from the Camera Link interface is (7 bits/parallel clk)\*(85MHz) = 595MHz.**

Cameras with pixel rates above the internally generated 85 MHz FMC transfer rate are supported. Most of the data received from the camera during the horizontal image margin is not transferred to the FMC interface. The margin time is instead utilized to transfer up to 256 pixels of the accumulated higher speed line image data. The only non-image data transferred on the FMC interface consists of the data received to mark the end of line or end of frame condition. Other limitations include cable length/quality and FPGA PLL restrictions.

The 26-pin Camera Link base connector also contains dedicated pins for the Camera Control (CC) lines, optional PoCL wires, and the Frame Grabber to Camera full duplex serial communication lines. These additional base connector functions are fully supported by the FPGA including SafePower PoCL control. The FMC-200 can utilize the second 26-pin Camera Link connector as either a medium/full/extended data connection or as an independent fully functional second base camera connector including PoCL support.

Here is a sample of a camera timing diagram. See the specific camera specifications for your camera of interest.

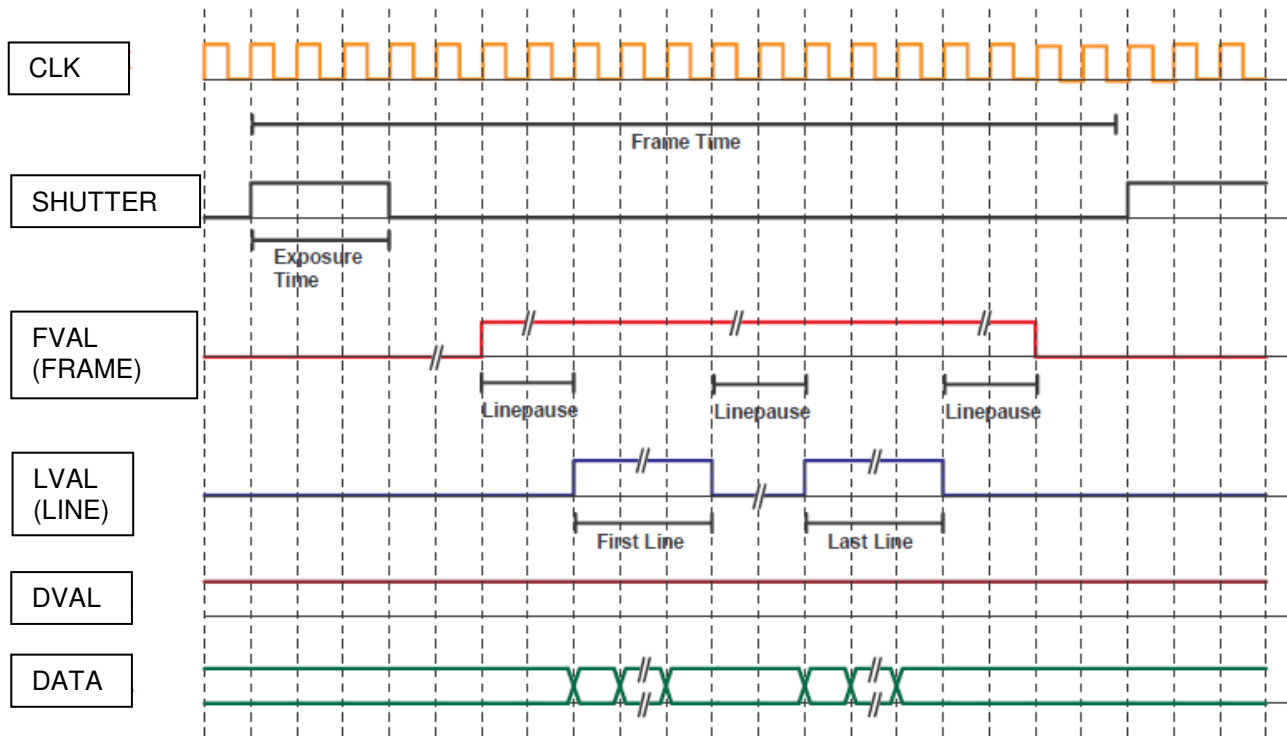


Figure 2-2 Sample Camera Timing Diagram

## 2.2.3 FPGA

The FMC-200 contains an Altera EP3C16 Cyclone III device in a 256 pin FBGA. This board layout is compatible with the alternative EP3C10 and EP3C5 devices.

The primary purpose of the FPGA is to receive and process the Camera Link serialized data. It de-serializes the camera data and sends it through cross clock domain synchronization FIFOs. Depending on the camera configuration that is programmed in the FPGA's registers, the data is read from the FIFOs and bitwise re-ordered appropriately. Because the three PLLs that are used to de-serialize the incoming camera link data can attain lock at different times, it is necessary to send the re-ordered data to another set of three FIFOs that are used for line alignment. The data is read out of these FIFOs after line alignment is achieved, parsed into memory mapped pixel data, and sent to an output stage FIFO (all 88 bits of parallel data) prior to being serialized for transmit down the FMC connector to the FMC Carrier.

### 2.2.3.1 FPGA Control & Setup Registers

See **Chapter 5 User Programmable Registers** for details on the registers used to control the operation of the FMC-200 module.

### 2.2.3.2 FPGA UART Description

The FPGA contains two UART modules, one for camera A and a second for camera B (when in dual base mode). The UARTs implement the Camera Link defined (1) Start bit, (1) Stop bit, and no parity bit.

The UARTs are controlled using the following registers: **Baud Rate Divisor UART A Register**, **Baud Rate Divisor UART B Register**, **Rx/Tx Buffer UART A Register**, **Rx/Tx Buffer UART B Register**, and **UART Status Register**.

Operation is straight forward. A write to the Rx/Tx buffer register will cause the 8 bit parallel data to be serially transmitted LSB first to the Camera Link SerTC line. A read of the Rx/Tx buffer register returns the data byte received via the Camera Link SerTFG line and buffered in a FIFO. The baud rate is determined by the baud rate divisor register value. See **Table 2-1 Baud Rate Divisor vs. Baud Rate, 20MHz oscillator** to determine the divisor value for some common baud rates.

The baud rate is determined by the board's oscillator frequency using the following equation.

$$\text{Baud rate} = (\text{oscillator frequency}) / (16 * (\text{Baud Rate Divisor}))$$

The on-board oscillator is 20MHz. This clock is divided down by a fixed factor of 16 prior to final determination of the baud rate using the baud rate divisor value.

Baud Rate Divisor Value	Nominal Baud Rate
255	4900
130 (default)	9600
65	19200
32	38400
16	76800

**Table 2-1 Baud Rate Divisor vs. Baud Rate, 20MHz oscillator**

The Rx/Tx buffer registers are implemented using separate FIFOs configured as 256 words x 8 bits. There are preset Tx FIFO status flags of 16 words for almost empty and 240 words for almost full. These flags may be used to determine the timing of burst Tx buffer writes which offload the host from the task of monitoring UART status.

Rx data monitoring of the serial data communications is accomplished using the UART Status Register. When a byte of data is received, the "rx\_valid\_uart\_a/b" bit will be asserted. In future FPGA releases the interrupt signal to the FMC connector will also assert. If the receive FIFO overflows prior to reading the received data, then the "rx\_over\_run\_uart\_a/b" bit asserts.

For Tx data flow control the "tx\_almost..." bits of the UART Status Register are used. The host can write bytes of data to the Rx/Tx buffer register in a large burst based on a set almost empty status or in smaller bursts until the almost full bit is set. In future FPGA releases the interrupt signal to the FMC connector will also assert on rising edges of both the almost empty and almost full flags.

Transient status conditions are captured (latched) in the UART Status Register. Reading the status register will refresh the latched contents to the current status and therefore some bits may be cleared due to the read.



## 2.2.4 Serial EEPROM

The FPGA's configuration data is stored in an Altera EPCS16SI8N serial EEPROM device. This device is 16M bit and can hold up to (8) FPGA images (configurations).

## 2.2.5 Serial (I2C) EEPROM

The FMC-200 contains a 2K bit I2C EEPROM device available to store hardware definition information that may be accessed by an external controller implementing IPMI reads and writes using FMC I2C serial bus transactions.

## 2.2.6 Oscillator, Core Regulator, and Power On Reset

The FMC-200 contains a 20MHz oscillator that may be used by the FPGA's PLLs to create the internal clocks required to process the received camera link video data and transmit it to the FMC carrier.

A voltage regulator is used to convert the FMC 2.5V Vadj power to the FPGA's required 1.2V core logic voltage.

The on-board Power On Reset device ensures that the FPGA logic powers up in a known state.

## 2.2.7 Power Over Camera Link (PoCL)

A robust Power Over Camera Link (PoCL) scheme, with the SafePower protocol has been implemented. This logic is designed to prevent a frame grabber from attempting to supply power to a conventional camera link cable or camera. The SafePower protocol logic is implemented within the FPGA, and the power switching and sensing circuitry is implemented using discrete components on the FMC-200 board. Manual control of the PoCL circuitry is also possible through the FMC-200 register interface.

## Chapter 3. Getting Started

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This section provides information on installing and configuring the FMC-200 Programmable Camera Interface FMC Card.

### 3.1 Unpacking the FMC-200



**Figure 3-1 FMC-200 Front View**

The FMC-200 is delivered preassembled as shown above. FMC mounting standoffs and screws are provided for mounting to the FMC Carrier. The Camera Link connectors are labeled 1 and 2; the general purpose micro connector has a black dot located by its pin 1.

Connector	Function
26-pin SDR Camera Link – 1	Base mode configuration.
26-pin SDR Camera Link – 2	Medium, Full, Dual Base configurations.
14-pin micro connector	General purpose I/O. Pin 1 is located by the black dot.

**Table 3-1 Front Panel Connectors Description**

### 3.2 System Requirements

An FMC Carrier with at least one LPC connector. FMC Carrier must provide 12V power if using PoCL. The FMC Vadj voltage level is not specified in the IPMI I2C EEPROM but it must be 2.5V.



### 3.3 Compatibility

The baseline FMC-200 is compatible with cameras operating up to 85 MHz and beyond. With cameras operating above 85 MHz camera, careful characterization of the cables and the environmental noise must be considered and tested. See section 2.2.2 Camera Link Interface for additional information.

The FMC specification Rule 3.20 states: "Boards shall provide a minimum of 500Vdc and 1 M $\Omega$  of isolation between the FMC front panel bezel and the mezzanine circuit ground". The 3M SDR connectors used in the FMC-200 have an insulation resistance of 500 M $\Omega$  min at @250 VDC. Additional information is required to guarantee FMC compliance to Rule 3.20.

### 3.4 Electrical and Environmental

Operating Temperature Range: 0°C (32°F) to 55°C (131°F)

Air Cooled

FMC Vadj = 2.5V, 1 A max

FMC 12V0P 800 mA (~400 mA per optional PoCL output)

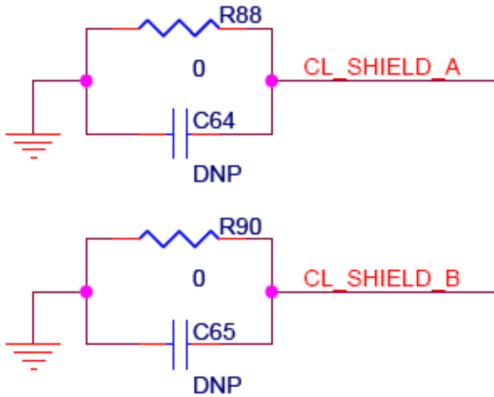
### 3.5 Switch and Jumper Options and Locations

This FMC-200 does not contain any user configurable switcher or jumpers. All configurations are via user programmable registers.

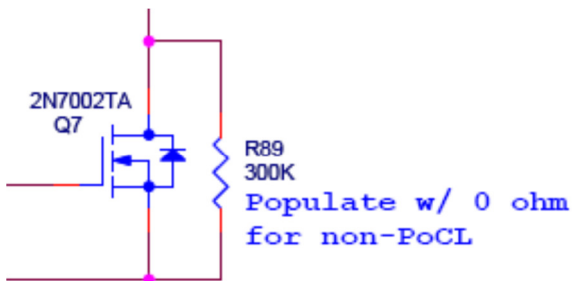
See **Chapter 5 User Programmable Registers** for information on the FMC-200 setup and control registers.

### 3.6 Optional Camera Link Shield Connections

The default FMC-200 shield termination is a zero ohm resistor to digital ground as shown below. The optional capacitor connection (C64, C65) is also available. Both the resistor and capacitor are SMT 0603 parts located on the back of the FMC-200 near the SDR Camera Link connectors.



R87 (not shown) and R89 are 300K SMT 0603 resistors in parallel with the non-PoCL Shield termination MOSFETs which are turned on for non-PoCL applications (Q5 not shown). These resistors may be changed to zero ohms if a lower impedance shield connection is desired on pins 1 and 26 of the SDR connector. For complete isolation of the shields the MOSFETs must be removed along with R87 and R89.





## **Chapter 4. FMC-200 I/Os**

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### **4.1 FMC-200 External Connections**

This section details the various I/O ports available on the FMC-200 module.



### 4.1.1 FMC 160-pin LPC Connector Pinout

**Table 4-1 FMC LPC Connector Pinout** details the pin assignments of the 160-pin LPC FMC connector. “Dir” (Direction) is with respect to the FMC module; i.e. **In = from** carrier card, **Out = to** carrier card.

FMC LPC Pin#	FMC LPC Pin Name	FMC Module Signal Name	Dir	FMC LPC Pin#	FMC LPC Pin Name	FMC Signal Name	Dir
D1	PG_C2M	fmc_pg_c2m	In	C1	GND		
D2	GND			C2	DP0_C2M_P	Unused	
D3	GND			C3	DP0_C2M_N	Unused	
D4	GBTCLK0_M2C_P	resistor tie lo	Out	C4	GND		
D5	GBTCLK0_M2C_N	resistor tie hi	Out	C5	GND		
D6	GND			C6	DP0_M2C_P	Unused	
D7	GND			C7	DP0_M2C_N	Unused	
D8	LA01_P_CC	gp_diff_data	In	C8	GND		
D9	LA01_N_CC	gp_diff_data(n)	In	C9	GND		
D10	GND			C10	LA06_P	db_clk	In
D11	LA05_P	db_data[6]	In	C11	LA06_N	db_addr[0]	In
D12	LA05_N	db_data[7]	In	C12	GND		
D13	GND			C13	GND		
D14	LA09_P	db_en	In	C14	LA10_P	fmc_gpio[1]	Bidi
D15	LA09_N	fmc_gpio[0]	Bidi	C15	LA10_N	fmc_gpio[2]	Bidi
D16	GND			C16	GND		
D17	LA13_P	fmc_v_data[1]	Out	C17	GND		
D18	LA13_N	fmc_v_data[1](n)	Out	C18	LA14_P	fmc_v_data[2]	Out
D19	GND			C19	LA14_N	fmc_v_data[2](n)	Out
D20	LA17_P_CC	db_addr[4]	In	C20	GND		
D21	LA17_N_CC	resistor tie lo	Out	C21	GND		
D22	GND			C22	LA18_P_CC	fmc_v_data[5]	Out
D23	LA23_P	fmc_v_data[10]	Out	C23	LA18_N_CC	fmc_v_data[5](n)	Out
D24	LA23_N	fmc_v_data[10](n)	Out	C24	GND		
D25	GND			C25	GND		
D26	LA26_P	Unused		C26	LA27_P	Unused	
D27	LA26_N	Unused		C27	LA27_N	Unused	
D28	GND			C28	GND		
D29	TCK	TCK	In	C29	GND		
D30	TDI	TDI	In	C30	SCL	SCL	In
D31	TDO	TDO		C31	SDA	SDA	Bidi
D32	3P3VAUX	3P3VAUX		C32	GND		
D33	TMS	TMS	In	C33	GND		
D34	TRST_L	Unused		C34	GA0	GA0	In
D35	GA1	GA1	In	C35	12P0V	12P0V	
D36	3P3V	3P3V		C36	GND		
D37	GND			C37	12P0V	12P0V	
D38	3P3V	3P3V		C38	GND		
D39	GND			C39	3P3V	3P3V	
D40	3P3V	3P3V		C40	GND		

FMC LPC Pin#	FMC LPC Pin Name	FMC Module Signal Name	Dir	FMC LPC Pin#	FMC LPC Pin Name	FMC Signal Name	Dir
H1	VREF_A_M2C	Unused		G1	<b>GND</b>		
H2	PRSENT_M2C_L	PRSENT_M2C_L	Out	<b>G2</b>	<b>CLK0_C2M_P</b>	<b>resistor tie lo</b>	In <sup>1</sup>
H3	GND			<b>G3</b>	<b>CLK0_C2M_N</b>	<b>resistor tie hi</b>	In <sup>1</sup>
H4	CLK0_M2C_P	fmc_vclk	Out	G4	GND		
H5	CLK0_M2C_N	fmc_vclk(n)	Out	G5	GND		
H6	GND			G6	LA00_P_CC	gp_diff_clk	In
H7	LA02_P	db_data[0]	Bidi	G7	LA00_N_CC	gp_diff_clk(n)	In
H8	LA02_N	db_data[1]	Bidi	G8	GND		
H9	GND			G9	LA03_P	db_data[2]	Bidi
H10	LA04_P	db_data[4]	Bidi	G10	LA03_N	db_data[3]	Bidi
H11	LA04_N	db_data[5]	Bidi	G11	GND		
H12	GND			G12	LA08_P	db_addr[3]	In
H13	LA07_P	db_addr[1]	In	G13	LA08_N	db_rnw	In
H14	LA07_N	db_addr[2]	In	G14	GND		
H15	GND			G15	LA12_P	fmc_v_data[0]	Out
H16	LA11_P	fmc_gpio[3]	Bidi	G16	LA12_N	fmc_v_data[0](n)	Out
H17	LA11_N	interrupt	Out	G17	GND		
H18	GND			G18	LA16_P	fmc_v_data[4]	Out
H19	LA15_P	fmc_v_data[3]	Out	G19	LA16_N	fmc_v_data[4](n)	Out
H20	LA15_N	fmc_v_data[3](n)	Out	G20	GND		
H21	GND			G21	LA20_P	fmc_v_data[7]	Out
H22	LA19_P	fmc_v_data[6]	Out	G22	LA20_N	fmc_v_data[7](n)	Out
H23	LA19_N	fmc_v_data[6](n)	Out	G23	GND		
H24	GND			G24	LA22_P	fmc_v_data[9]	Out
H25	LA21_P	fmc_v_data[8]	Out	G25	LA22_N	fmc_v_data[9](n)	Out
H26	LA21_N	fmc_v_data[8](n)	Out	G26	GND		
H27	GND			G27	LA25_P	Unused	
H28	LA24_P	Unused		G28	LA25_N	Unused	
H29	LA24_N	Unused		G29	GND		
H30	GND			G30	LA29_P	Unused	
H31	LA28_P	Unused		G31	LA29_N	Unused	
H32	LA28_N	Unused		G32	GND		
H33	GND			G33	LA31_P	Unused	
H34	LA30_P	Unused		G34	LA31_N	Unused	
H35	LA30_N	Unused		G35	GND		
H36	GND			G36	LA33_P	Unused	
H37	LA32_P	Unused		G37	LA33_N	Unused	
H38	LA32_N	Unused		G38	GND		
H39	GND			G39	VADJ	VADJ (2.5V)	
H40	VADJ	VADJ (2.5V)		G40	GND		

**Color Legend Below**

Ground	12.0V	3.3V	Vadj 2.5V	JTAG signal
Clock Pin	Single Ended Sig.	Differential Pair	I2C signal	Unused

**Table 4-1 FMC LPC Connector Pinout**

<sup>1</sup> It is anticipated that this signal, CLK0\_C2M, pins G2/G3 will **switch direction to an output** in the next revision of the FMC specification and become a mezzanine to carrier clock signal

### 4.1.2 Front Bezel Camera Link Interface Connector Diagram

Figure 4-1 Camera Link Interface Connections shows a Camera Link interface with base, medium and full configurations defined.

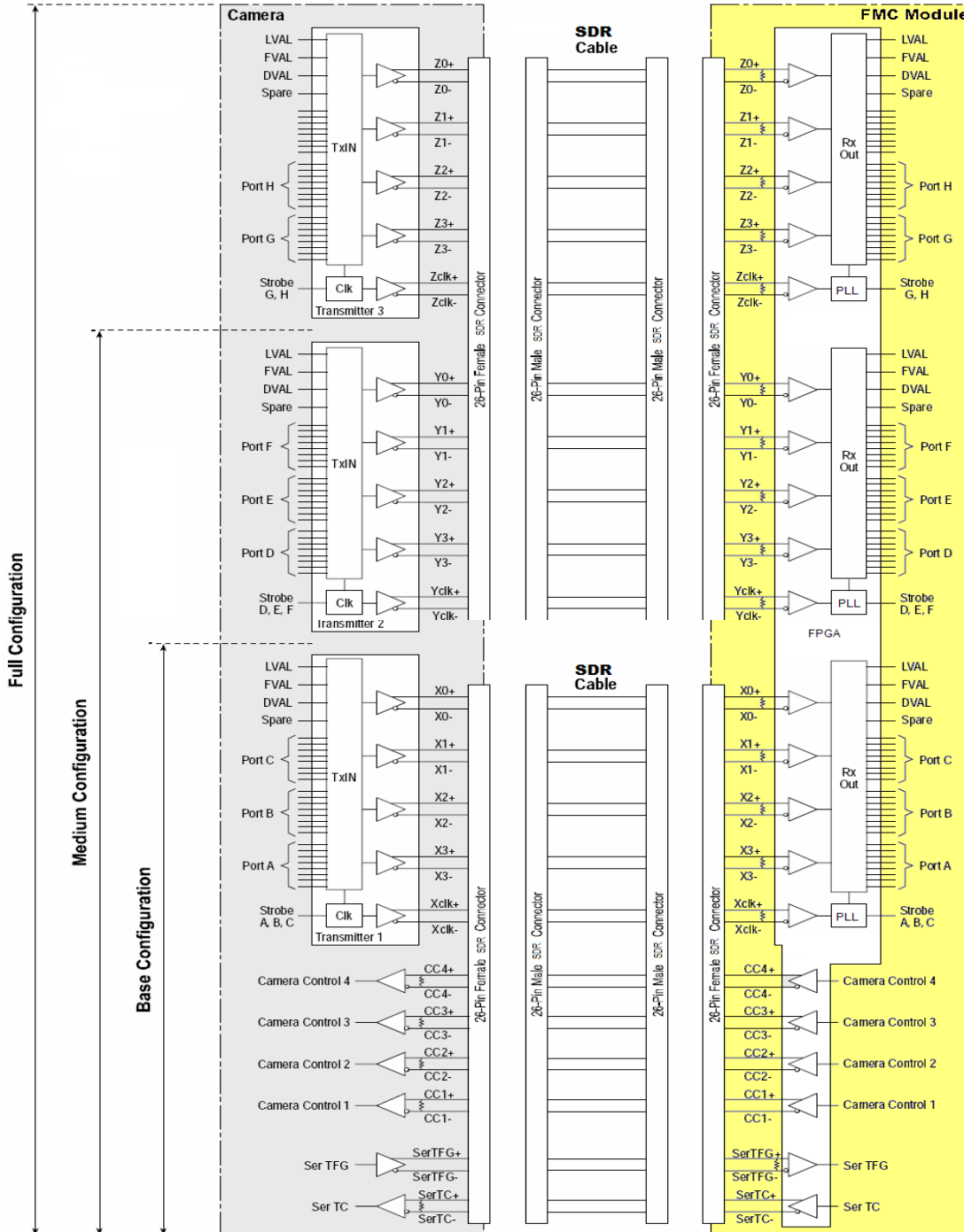


Figure 4-1 Camera Link Interface Connections

### 4.1.3 Front Bezel Camera Link 26-pin SDR Connectors Pinout

**Table 4-2 Base, Medium, Full Camera Link pinout** shows the functions of the Mini CL pins when the board is configured as a **base**, **medium**, or **full** Camera Link interface. The mini-Camera Link connectors are labeled “1” and “2” on the front bezel.

Medium & Full Configurations			Base Configuration		
Mini-CL connector 2 pin #	CL Signal	Direction	Mini-CL connector 1 pin #	CL Signal	Direction
1	Inner shield	-	1	Inner shield/PoCL	-
14	Inner shield	-	14	Inner shield	-
25	Y0-	In	25	X0-	In
12	Y0+	In	12	X0+	In
24	Y1-	In	24	X1-	In
11	Y1+	In	11	X1+	In
23	Y2-	In	23	X2-	In
10	Y2+	In	10	X2+	In
22	Yclk-	In	22	Xclk-	In
9	Yclk+	In	9	Xclk+	In
21	Y3-	In	21	X3-	In
8	Y3+	In	8	X3+	In
20	100 ohm	-	20	SerTC+	Out
7	Terminated	-	7	SerTC-	Out
19	Z0-	In	19	SerTFG-	In
6	Z0+	In	6	SerTFG+	In
18	Z1-	In	18	CC1-	Out
5	Z1+	In	5	CC1+	Out
17	Z2-	In	17	CC2+	Out
4	Z2+	In	4	CC2-	Out
16	Zclk-	In	16	CC3-	Out
3	Zclk+	In	3	CC3+	Out
15	Z3-	In	15	CC4+	Out
2	Z3+	In	2	CC4-	Out
13	Inner shield	-	13	Inner shield	-
26	Inner shield	-	26	Inner shield/PoCL	-

**Table 4-2 Base, Medium, Full Camera Link pinout**

**Table 4-3 Dual Base Camera Link pinout** shows the functions of the Mini CL pins when the board is configured as a **dual base** Camera Link interface.

Dual Base Configuration-Camera B			Dual Base Configuration-Camera A		
Mini-CL connector 2 pin #	CL Signal	Direction	Mini-CL connector 1 pin #	CL Signal	Direction
1	Inner shield/PoCL	-	1	Inner shield/PoCL	-
14	Inner shield	-	14	Inner shield	-
25	X0-	In	25	X0-	In
12	X0+	In	12	X0+	In
24	X1-	In	24	X1-	In
11	X1+	In	11	X1+	In
23	X2-	In	23	X2-	In
10	X2+	In	10	X2+	In
22	Xclk-	In	22	Xclk-	In
9	Xclk+	In	9	Xclk+	In
21	X3-	In	21	X3-	In
8	X3+	In	8	X3+	In
20	SerTC+	Out	20	SerTC+	Out
7	SerTC-	Out	7	SerTC-	Out
19	SerTFG-	In	19	SerTFG-	In
6	SerTFG+	In	6	SerTFG+	In
18	CC1-	Out	18	CC1-	Out
5	CC1+	Out	5	CC1+	Out
17	CC2+	Out	17	CC2+	Out
4	CC2-	Out	4	CC2-	Out
16	CC3-	Out	16	CC3-	Out
3	CC3+	Out	3	CC3+	Out
15	CC4+	Out	15	CC4+	Out
2	CC4-	Out	2	CC4-	Out
13	Inner shield	-	13	Inner shield	-
26	Inner shield/PoCL	-	26	Inner shield/PoCL	-

**Table 4-3 Dual Base Camera Link pinout**

#### 4.1.4 Front Bezel General Purpose Connector Pinout

**Table 4-4 Bezel General Purpose Connector Pinout** details the pinout of the front panel general purpose connector.

**Note:** Pin 1 is indicated on the front bezel by a black dot next to the connector.

Name	Direction*	Connector Pin #	I/O Standard
ground	-	3	-
bez_diff_io[0]	Out	7	LVDS
bez_diff_io[0](n)		8	LVDS
bez_diff_io[1]	In	1	LVDS
bez_diff_io[1](n)		2	LVDS
bez_gpio[0]	Bidi	13	LVC MOS 2.5V
bez_gpio[1]	Bidi	14	LVC MOS 2.5V
ground	-	9	-

**Table 4-4 Bezel General Purpose Connector Pinout**

\* Default direction for standard configuration. Pins can be configured as an In or Out, depending on application desired.

- Re-configuration of pin direction for the single-ended IO is controlled via the *bezel\_gpio\_dir\_dir* register (see **Table 5-6**).
- Re-configuration of pin direction for the differential IO **cannot** occur on the fly. The FPGA configuration file needs to be modified to change the IO specification **and** the termination resistor configuration on the board needs to be modified (to ensure LVDS compliance). Differential direction change is available upon request.

#### 4.1.5 Module Board Header Connector Pinout

**Table 4-5 Header Connector Pinout** details the pinout of the circuit board's header connector.

Name	Direction*	Connector Pin #	I/O Standard
hdr_diff_io[0]	Out	3	LVDS
hdr_diff_io[0](n)		1	LVDS
hdr_diff_io[1]	In	4	LVDS
hdr_diff_io[1](n)		2	LVDS
<i>The following 2 differential pairs are <b>not</b> available when the FPGA is configured for Base only configuration (EP3C10, EP3C5 parts).</i>			
hdr_diff_io[2]	In	9	LVDS
hdr_diff_io[2](n)		7	LVDS
hdr_diff_io[3]	Out	10	LVDS
hdr_diff_io[3](n)		8	LVDS

**Table 4-5 Header Connector Pinout**

\* Default direction shown for standard configuration. Differential signal direction can be configured as an In or Out, depending on application desired, however, modification of pin direction for the differential IO **cannot** occur on the fly. The FPGA configuration file needs to be modified to change the IO specification **and** the termination resistor configuration on the board needs to be modified (to ensure LVDS compliance). Differential direction change is available upon request.

## Chapter 5. User Programmable Registers

### 5.1 Data Bus Interface

The camera link FMC module is configured and controlled by a basic data bus interface. It consists of an (8) bit bidirectional data bus, (5) address bits, (1) enable, (1) read-not-write direction control, and a clock. **Figure 5-1 Data Bus Interface Timing** shows some example write and read cycles. Note that **two IDLE bus cycles are mandatory between Read to Write direction changes** to allow for a bus “turnaround” cycle. Two cycles are needed due to read data pipelining that was required to meet IO timing requirements. Write data on the db\_data bus is driven by the FMC carrier board, read data is driven by the FMC module’s FPGA.

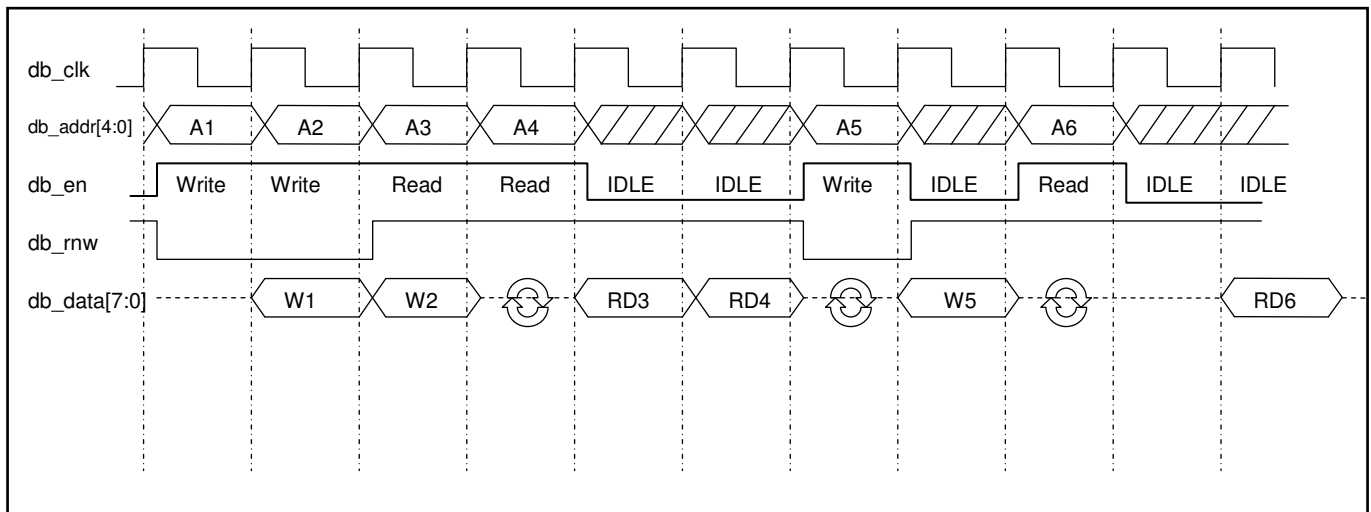


Figure 5-1 Data Bus Interface Timing

## 5.2 Register Map

The register map for the FMC-200 module is shown in Table 5-1: Register Map.

Address (hex)	Register Name	Bits Used	Type	Reset Value	Cross Reference
0x00	mode_configuration	[7:0]	R/W	0x03	Table 5-2
0x01	baud_rate_div_uart_a	[7:0]	R/W	0x82	Table 5-3
0x02	baud_rate_div_uart_b	[7:0]	R/W	0x82	Table 5-4
0x03	fmc_gpio_dir	[3:0]	R/W	0x00	Table 5-5
0x04	bezel_gpio_dir	[1:0]	R/W	0x00	Table 5-6
0x05	<b>Not Used</b>	--	--	--	--
0x06	x_bit_slip	[3:0]	R/W	0x05	Table 5-7
0x07	y_bit_slip	[3:0]	R/W	0x05	Table 5-8
0x08	z_bit_slip	[3:0]	R/W	0x05	Table 5-9
0x09	camera_ctrl_a	[4:0]	R/W	0x00	Table 5-10
0x0A	camera_ctrl_b	[4:0]	R/W	0x00	Table 5-11
0x0B	rx_tx_buff_uart_a	[7:0]	R/W	0x00	Table 5-12
0x0C	rx_tx_buff_uart_b	[7:0]	R/W	0x00	Table 5-13
0x0D	uart_status	[7:0]	R/O	0x00	Table 5-14
0x0E	pocl_ctrl_a	[6:0]	R/W	0x00	Table 5-15
0x0F	pocl_ctrl_b	[6:0]	R/W	0x00	Table 5-16
0x10	fmc_gpio_data	[3:0]	R/W	--	Table 5-17
0x11	bezel_data	[3:0]	R/W	--	Table 5-18
0x12	header_data	[3:0]	R/W	--	Table 5-19
0x13	pocl_status_a	[7:0]	R/O	0x00	Table 5-20
0x14	pocl_status_b	[7:0]	R/O	0x00	Table 5-21
0x15	camera_setup_a	[7:0]	R/W	0x00	Table 5-22
0x16	camera_setup_b	[7:0]	R/W	0x00	Table 5-23
0x17-0x1C	<b>Not Used</b>	--	--	--	--
0x1D	reconfig_ctrl	[7:0]	R/W	0x00	Table 5-24
0x1E	reconfig_data	[7:0]	W/O	--	Table 5-25
0x1F	revision_control	[7:0]	R/O	--	Table 5-26

**Table 5-1: Register Map**



## 5.2.1 Detailed Register Descriptions

The tables below provide detailed register descriptions.

Name	mode_configuration		
Address	0x00		
Bit	Description	Type	Reset Value
7	<b>AwaitingRxSerLockZ</b> 0 = Channel Link Z receiver PLL is locked, or Z link not enabled. 1 = Channel Link Z receiver PLL not locked and Z link enabled.	R/O	-
6	<b>AwaitingRxSerLockY (or Dual Camera X)</b> 0 = Channel Link Y receiver PLL is locked, or Y link not enabled. 1 = Channel Link Y receiver PLL not locked and Y link enabled.	R/O	-
5	<b>AwaitingRxSerLockX</b> 0 = Channel Link X receiver PLL is locked, or X link not enabled. 1 = Channel Link X receiver PLL not locked and X link enabled.	R/O	-
4:2	<b>mode_config</b> <b>Note:</b> <i>Can only be changed when camera or cameras, in the case of dual mode, are in reset (bits [1:0]).</i> 000 = Base camera link mode 001 = Medium camera link mode 010 = Full camera link mode 011 = Extended camera link mode (FPGA Revision specific) 100 = Dual Base camera link mode (Certain FPGA Revisions)	R/W	'000'
1	<b>ResetCamB</b> 0 = Camera B processing logic is not in reset, check bit 6 (AwaitingRxSerLockY) for indication of Camera B lock status 1 = Camera B processing logic is in reset, Camera B setup (Register x16) can be used to configure the processing logic.	R/W	1
0	<b>ResetCamA</b> 0 = Camera A processing logic is not in reset, check bits 5/6/7 (AwaitingRxSerLockX/Y/Z) for indication of Camera A lock status 1 = Camera A processing logic is in reset, Camera A setup (Register x15) can be used to configure the processing logic.	R/W	1

**Table 5-2 Mode Configuration Register**

Name	baud_rate_div_uart_a		
Address	0x01		
Bit	Description	Type	Reset Value
7:0	<b>brd_uart_a</b> = clock divider value used to set the baud rate. See Table 2-1 for settings other than the reset default 9600 baud	R/W	0x82

**Table 5-3 Baud Rate Divisor UART A Register**

Name	baud_rate_div_uart_b		
Address	0x02		
NOTE: This register has effect only in dual base mode!			
Bit	Description	Type	Reset Value
7:0	<b>brd_uart_b</b> = clock divider value used to set the baud rate. See Table 2-1 for settings other than the reset default 9600 baud	R/W	0x82

**Table 5-4 Baud Rate Divisor UART B Register**

Name	fmc_gpio_dir		
Address	0x03		
Bit	Description	Type	Reset Value
7:4	Reserved	-	-
3:0	<b>fmc_gpio_dir</b> Direction control for the FMC connector gpio pins, <i>fmc_gpio[3:0]</i> : 0 = Input to FMC module's FPGA. 1 = Output from FMC module's FPGA. <b>Note:</b> Regardless of whether the FMC Carrier or the FMC-200 is driving the <i>fmc_gpio[3:0]</i> pins some or all of these pin values may also be directed to the Camera A or B Camera Link Camera Control lines. See Camera A Control Register and Camera B Control Register (0x09 and 0x0A)	R/W	0

**Table 5-5 FMC GPIO and Header Direction Register**

Name	bezel_gpio_dir		
Address	0x04		
Bit	Description	Type	Reset Value
7:2	Reserved	-	-
1:0	<p><b>bezel_gpio_dir</b>            Direction control for the bezel connector <i>single ended</i> gpio pins, <i>bez_gpio[1:0]</i> :            0 = Input to FMC module's FPGA.            1 = Output from FMC module's FPGA.</p> <p><b>Note:</b> The additional (2) <i>differential</i> gpio channels on the front bezel connector are fixed as (1) differential IN, (1) differential OUT. See Table 4-4. User register control of direction is not available. Customization of channel direction is available upon request.</p>	R/W	0

**Table 5-6 Front Bezel GPIO Direction Register**

Name	x_bit_slip		
Address	0x06		
Bit	Description	Type	Reset Value
7:4	Reserved	-	-
3:0	<p><b>X_bit_slip</b>            This register configures the de-serializer associated with Channel Link X(3:0) differential signal inputs and should not require modification by the user.</p>	R/W	0x05

**Table 5-7 X-bit Slip Register**

Name	y_bit_slip		
Address	0x07		
Bit	Description	Type	Reset Value
7:4	Reserved	-	-
3:0	<p><b>Y_bit_slip</b>            This register configures the de-serializer associated with Channel Link Y(3:0) differential signal inputs and should not require modification by the user.</p>	R/W	0x05

**Table 5-8 Y-bit Slip Register**

Name	z_bit_slip		
Address	0x08		
Bit	Description	Type	Reset Value
7:4	Reserved	-	-
3:0	<b>Z_bit_slip</b> This register configures the de-serializer associated with Channel Link Z(3:0) differential signal inputs and should not require modification by the user.	R/W	0x05

**Table 5-9 Z-bit Slip Register**

Name	camera_ctrl_a		
Address	0x09		
Bit	Description	Type	Reset Value
7:5	Reserved	-	-
4	<b>control_sel_a</b> 0 = Camera Control lines for Camera A are controlled by both this register's value and the FMC connector pins: CC[4:3] = bits [3:2] (reg_cc_a) * CC[2:1] = fmc_gpio[1:0] pins 1 = Camera Control lines for Camera A are controlled by this register's value only: CC[4:1] = bits [3:0] (reg_cc_a) *  * <b>Note:</b> reg_cc_a[3:2] drive CC[4:3] for both states of control_sel_a because there are not enough fmc_gpio available to drive these signals in a dual base mode. The fmc_gpio[3:2] pins are used to drive camera B's CC[2:1] signals in dual base mode.	R/W	0
3:0	<b>reg_cc_a</b> Use to drive camera A CC[4:1] when bit 4 (control_sel_a) = 1, otherwise only bits 3:2 used to drive camera A CC[4:3]	R/W	0

**Table 5-10 Camera A Control Register**

Name	camera_ctrl_b		
Address	0x0A		
NOTE: This register has effect only in dual base mode!			
Bit	Description	Type	Reset Value
7:5	Reserved	-	-
4	<p><b>control_sel_b</b></p> <p>0 = Camera Control lines for Camera B are controlled by both this register's value and the FMC connector pins:            CC[4:3] = bits [3:2] (reg_cc_b) *            CC[2:1] = fmc_gpio[3:2]</p> <p>1 = Camera Control lines for Camera B are controlled by this register's value only            CC[4:1] =bits [3:0] (reg_cc_b) *</p> <p>* <b>Note:</b> reg_cc_b[3:2] drive CC[4:3] for both states of control_sel_b because there are not enough fmc_gpio available to drive these signals in a dual base mode. fmc_gpio[1:0] pins are used to drive camera A's CC[2:1] signals in dual base mode.</p>	R/W	0
3:0	<p><b>reg_cc_b</b></p> <p>Use to drive camera B CC[4:1] when bit 4 (control_sel_b) = 1, otherwise only bits 3:2 used to drive camera B CC[4:3]</p>	R/W	0

**Table 5-11 Camera B Control Register**

Name	rx_tx_buff_uart_a		
Address	0x0B		
Bit	Description	Type	Reset Value
7:0	<p><b>buff_data_uart_a</b></p> <p>Read = UART A Receive buffer data FIFO.            Write = UART A Transmit buffer data FIFO.</p>	R/W	0

**Table 5-12 Rx/Tx Buffer UART A Register**

<b>Name</b>	<b>rx_tx_buff_uart_b</b>		
<b>Address</b>	<b>0x0C</b>		
<b>NOTE: This register has effect only in dual base mode!</b>			
<b>Bit</b>	<b>Description</b>	<b>Type</b>	<b>Reset Value</b>
7:0	<b>buff_data_uart_b</b> Read = UART B Receive buffer data FIFO. Write = UART B Transmit buffer data FIFO.	R/W	0

**Table 5-13 Rx/Tx Buffer UART B Register**

Name	uart_status		
Address	0x0D		
	<p><b>Note:</b> The interrupt function is not yet available. Transient status conditions are captured (latched) in the UART Status Register. Reading the status register will refresh the latch contents to the current status and therefore some bits may be cleared due to the read.</p>		
Bit	Description	Type	Reset Value
7	<p><b>rx_over_run_uart_b</b>            '1' = indicates over run of UART B Rx buffer.            Causes assertion of interrupt output.  <b>Note: Enabled only in dual base mode.</b></p>	R/O	0
6	<p><b>tx_almost_full_uart_b</b>            '1' = indicates UART B transmit FIFO almost full.            Rising edge causes assertion of interrupt output.  <b>Note: Enabled only in dual base mode.</b></p>	R/O	0
5	<p><b>tx_almost_empty_uart_b</b>            '1' = indicates UART B transmit FIFO almost empty.            Rising edge causes assertion of interrupt output.  <b>Note: Enabled only in dual base mode.</b></p>	R/O	0
4	<p><b>rx_valid_uart_b</b>            '1' = indicates UART B receive FIFO contains valid data.            Causes assertion of interrupt output.  <b>Note: Enabled only in dual base mode.</b></p>	R/O	0
3	<p><b>rx_over_run_uart_a</b>            '1' = indicates over run of UART A Rx buffer.            Causes assertion of interrupt output.</p>	R/O	0
2	<p><b>tx_almost_full_uart_a</b>            '1' = indicates UART A transmit FIFO almost full.            Rising edge causes assertion of interrupt output.</p>	R/O	0
1	<p><b>tx_almost_empty_uart_a</b>            '1' = indicates UART A transmit FIFO almost empty.            Rising edge causes assertion of interrupt output.</p>	R/O	0
0	<p><b>rx_valid_uart_a</b>            '1' = indicates UART A receive FIFO contains valid data.            Causes assertion of interrupt output.</p>	R/O	0

**Table 5-14 UART Status Register**

Name	pocl_ctrl_a		
Address	0x0E		
Bit	Description	Type	Reset Value
7	Reserved	-	-
6	<b>pocl_enable_a</b> Camera A Power over Camera Link (PoCL) circuit enable. 0 = disabled, Camera A shield pins 1 and 26 are connected to 0V 1 = enabled, functioning in either SafePower or Manual mode	R/W	0
5	<b>pocl_voltsense_hi_a</b> Camera A PoCL voltage sensing circuit input. 0 = PoCL voltage sense is below camera detect high threshold. 1 = PoCL voltage sense is above camera detect high threshold.	R/O	-
4	<b>pocl_voltsense_lo_a</b> Camera A PoCL voltage sensing circuit input. 0 = PoCL voltage sense is above camera detect low threshold. 1 = PoCL voltage sense is below camera detect low threshold.	R/O	-
3	<b>pocl_ctrl_sel_a</b> 0 = <b>SafePower Automatic</b> control of PoCL functions. 1 = <b>Manual</b> control of PoCL functions (0V, 12V, iccsrc enables). <b>Note:</b> Bit is sampled on a 0 to 1 transition of bit 6 (pocl_enable_a).	R/W	0
2	<b>reg_pocl_iccsrc_en_a</b> 0 = Camera A pins 1 and 26 <b>are not</b> connected to 52uA source. 1 = Camera A pins 1 and 26 <b>are</b> connected to 52uA source. <b>Note:</b> This bit only enabled when bit 3 (pocl_ctrl_sel_a) is '1'.	R/W	0
1	<b>reg_pocl_12v_en_a</b> 0 = Camera A pins 1 and 26 <b>are not</b> connected to 12V. 1 = Camera A pins 1 and 26 <b>are</b> connected to 12V. <b>Note:</b> This bit only enabled when bit 3 (pocl_ctrl_sel_a) is '1' and bit 2 (reg_pocl_iccsrc_en_a) is '0'. <b>WARNING:</b> Forcing 12V with a non-PoCL cable or Camera may result in damage to the FMC-200 and/or Camera.	R/W	0
0	<b>reg_pocl_0v_en_a</b> 0 = Camera A pins 1 and 26 <b>are not</b> connected to 0V. 1 = Camera A pins 1 and 26 <b>are</b> connected to 0V if bit 1 (reg_pocl_12v_en_a) is <b>not</b> set. <b>Note:</b> This bit only enabled when bit 3 (pocl_ctrl_sel_a) is '1' and bit 2 (reg_pocl_iccsrc_en_a) is '0'.	R/W	0

**Table 5-15 Camera A Power over Camera Link Control Register**



Name	pocl_ctrl_b		
Address	0x0F		
NOTE: This register has effect only in dual base mode!			
Bit	Description	Type	Reset Value
7	Reserved	-	-
6	<b>pocl_enable_b</b> Camera B Power over Camera Link (PoCL) circuit enable. 0 = disabled, Camera B shield pins 1 and 26 are connected to 0V 1 = enabled, functioning in either SafePower or Manual mode	R/W	0
5	<b>pocl_voltsense_hi_b</b> Camera B PoCL voltage sensing circuit input. 0 = PoCL voltage sense is below camera detect high threshold. 1 = PoCL voltage sense is above camera detect high threshold.	R/O	-
4	<b>pocl_voltsense_lo_b</b> Camera B PoCL voltage sensing circuit input. 0 = PoCL voltage sense is above camera detect low threshold. 1 = PoCL voltage sense is below camera detect low threshold.	R/O	-
3	<b>pocl_ctrl_sel_b</b> 0 = <b>SafePower Automatic</b> control of PoCL functions. 1 = <b>Manual</b> control of PoCL functions (0V, 12V, iccsrc enables). <b>Note:</b> Bit is sampled on a 0 to 1 transition of bit 6 (pocl_enable_b).	R/W	0
2	<b>reg_pocl_iccsrc_en_b</b> 0 = Camera B pins 1 and 26 <b>are not</b> connected to 52uA source. 1 = Camera B pins 1 and 26 <b>are</b> connected to 52uA source. <b>Note:</b> This bit only enabled when bit 3 (pocl_ctrl_sel_b) is '1'.	R/W	0
1	<b>reg_pocl_12v_en_b</b> 0 = Camera B pins 1 and 26 <b>are not</b> connected to 12V. 1 = Camera B pins 1 and 26 <b>are</b> connected to 12V. <b>Note:</b> This bit only enabled when bit 3 (pocl_ctrl_sel_b) is '1' and bit 2 (reg_pocl_iccsrc_en_b) is '0'. <b>WARNING:</b> Forcing 12V with a non-PoCL cable or Camera may result in damage to the FMC-200 and/or Camera.	R/W	0
0	<b>reg_pocl_0v_en_b</b> 0 = Camera B pins 1 and 26 <b>not</b> connected to 0V. 1 = Camera B pins 1 and 26 <b>are</b> connected to 0V if bit 1 (reg_pocl_12v_en_b) is <b>not</b> set. <b>Note:</b> This bit only enabled when bit 3 (pocl_ctrl_sel_b) is '1' and bit 2 (reg_pocl_iccsrc_en_b) is '0'.	R/W	0

**Table 5-16 Camera B Power over Camera Link Control Register**

Name	fmc_gpio_data		
Address	0x10		
Bit	Description	Type	Reset Value
7:4	Reserved	-	-
3:0	<p><b>fmc_gpio</b>            Read indicates state of <i>fmc_gpio[3:0]</i> pins (regardless of configured direction).            Write is value to drive on <i>fmc_gpio[3:0]</i> pins (only pins configured as outputs).</p> <p><b>Note:</b> Some or all of these write values may also be directed to the Camera A or B Camera Link Camera Control lines. See Camera A Control Register and Camera B Control Register(0x09 and 0x0A)</p>	R/W	0

**Table 5-17 FMC GPIO Connector Data Register**

Name	bezel_data		
Address	0x11		
Bit	Description	Type	Reset Value
7:4	Reserved	-	-
3:2	<p><b>bezel_diff</b>            Read indicates state of <i>bez_diff_io[1:0]</i> pins (regardless of configured direction).            Write is value to drive on <i>bez_diff_io[1:0]</i> pins (only pins configured as outputs).</p> <p><b>Note:</b> The (2) differential gpio channels on the front bezel connector are fixed as (1) differential IN, (1) differential OUT. SeeTable 4-4. User register control of direction is not available. Customization of channel direction is available upon request.</p>	R/W	0
1:0	<p><b>bezel_gpio</b>            Read indicates state of <i>bez_gpio[1:0]</i> pins (regardless of configured direction).            Write is drive value to <i>bez_gpio[1:0]</i> pins (only pins configured as outputs).</p>	R/W	0

**Table 5-18 Front Bezel Connector Data Register**

Name	header_data		
Address	0x12		
Bit	Description	Type	Reset Value
7:4	Reserved	-	-
3:0	<p><b>hdr_diff</b> Read indicates state of <i>hdr_diff_io[3:0]</i> pins (configured for any direction). Write is drive value to <i>hdr_diff_io[3:0]</i> pins (only pins configured as outputs).</p> <p><b>Note:</b> The (4) differential gpio channels on the header connector are fixed as (2) differential IN, (2) differential OUT. See Table 4-5. User register control of direction is not available. Customization of channel direction is available upon request.</p>	R/W	0

**Table 5-19 Header Connector Data Register**

Name	<b>pocl_status_a</b>		
Address	<b>0x13</b>		
	<b>Note:</b> This register is valid only when the PoCL A circuitry is enabled by bit 6 (pocl_enable_a) being set in the Camera A Power over Camera Link Control Register(0x0E).		
Bit	Description	Type	Reset Value
7	<b>DetectedCamClk</b> 1 = Camera XCLK active.	R/O	0
6	<b>DetectedNonPoclConn</b> 1 = Non-PoCL compliant device connection detected.	R/O	0
5	<b>DetectedOpenConn</b> 1 = A connected impedance of greater than 10K detected	R/O	0
4	<b>DetectedPoclCamera</b> 1 = PoCL compliant camera connection detected.	R/O	0
3	<b>PoweredCamera</b> 1 = 12V is being applied to PoCL wires.	R/O	0
2	<b>ErrDeadCamera</b> 1 = Power removed from camera due to lack of XCLK.	R/O	0
1	<b>ErrFailedStartup</b> 1 = Camera failed to produce XCLK relative to 12V application, qualifies bit 2 (ErrDeadCamera).	R/O	0
0	<b>ErrCameraDropout</b> 1 = Camera XCLK has stopped suddenly, qualifies bit 2 (ErrDeadCamera).	R/O	0

**Table 5-20 PoCL Status A**

Name	<b>pocl_status_b</b>		
Address	<b>0x14</b>		
	<b>Note:</b> This register is valid only when the PoCL B circuitry is enabled by bit 6 (pocl_enable_b) being set in the Camera B Power over Camera Link Control Register(0x0F).		
Bit	Description	Type	Reset Value
7	<b>DetectedCamClk</b> 1 = Camera XCLK active.	R/O	0
6	<b>DetectedNonPoclConn</b> 1 = Non-PoCL compliant device connection detected.	R/O	0
5	<b>DetectedOpenConn</b> 1 = A connected impedance of greater than 10K detected	R/O	0
4	<b>DetectedPoclCamera</b> 1 = PoCL compliant camera connection detected.	R/O	0
3	<b>PoweredCamera</b> 1 = 12V is being applied to PoCL wires.	R/O	0
2	<b>ErrDeadCamera</b> 1 = Power removed from camera due to lack of XCLK.	R/O	0
1	<b>ErrFailedStartup</b> 1 = Camera failed to produce XCLK relative to 12V application, qualifies bit 2 (ErrDeadCamera).	R/O	0
0	<b>ErrCameraDropout</b> 1 = Camera XCLK has stopped suddenly, qualifies bit 2 (ErrDeadCamera).	R/O	0

**Table 5-21 PoCL Status B**

Name	<b>camera_setup_a</b>		
Address	<b>0x15</b>		
	<b>Note:</b> <i>Can only be changed when camera processing logic is in reset ( Mode Configuration Register, 0x00, bit 0).</i>		
Bit	Description	Type	Reset Value
7	<b>RGB</b> 0 = Non-RGB mode camera mode. 1 = RGB mode camera mode, bits 6:4 (NumChannels) are ignored and a value of 3 channels is assumed. Bits 2:0 (BitDepthCode) are also restricted to bit depths defined in the Camera Link V1.2 Specification for Base and Medium Cameras.	R/W	0
6:4	<b>NumChannels</b> This value corresponds to the number of pixels that are sent by the camera on every transfer clock over the Camera Link connection.	R/W	011
3	Reserved	R/W	0
2:0	<b>BitDepthCode</b> Sets the bit width of the base/medium camera pixel data. 000 = 8-bit 010 = 10-bit (Assumed for Medium RGB Cameras if not 12-bit) 011 = 12-bit 100 = 14-bit (not available for medium cameras) 101 = 16-bit (not available for medium cameras)	R/W	000

**Table 5-22 Camera Setup A**

**Note:**

Register camera\_setup\_a applies only to Base, Medium, and dual Base modes and is restricted to the valid combinations of bit depth and number of channels defined in the Camera Link V1.2 Specification. Full and Extended modes are not configurable.

Name	<b>camera_setup_b</b>		
Address	<b>0x16</b>		
<b>Note:</b> <i>Can only be changed when camera processing logic is in reset ( Mode Configuration Register, 0x00,bit1).</i>			
Bit	Description	Type	Reset Value
7	<b>RGB</b> 0 = Non-RGB mode camera mode. 1 = RGB mode camera mode, bits 6:4 (NumChannels) are ignored and a value of 3 channels is assumed. Bits 2:0 (BitDepthCode) are also restricted to a bit depth of 8 as defined in the Camera Link V1.2 Specification for a Base camera.	R/W	0
6:4	<b>NumChannels</b> This value corresponds to the number of pixels that are sent by the camera on every transfer clock over the Camera Link connection.	R/W	011
3	Reserved	R/W	0
2:0	<b>BitDepthCode</b> Sets the bit width of the dual base camera pixel data. 000 = 8-bit 010 = 10-bit 011 = 12-bit 100 = 14-bit 101 = 16-bit	R/W	000

**Table 5-23 Camera Setup B**

**Note:** Register camera\_setup\_b applies only to dual Base mode.

Name	reconfig_ctrl		
<b>NOTE: This register function available upon request! Not present in standard configuration.</b>			
Address	0x1D		
Bit	Description	Type	Reset Value
7:6	Reserved	--	--
5:3	<b>config_image_id</b> This value is used to select the desired configuration image contained in the FMC-200 serial EEPROM used for programming the Altera FPGA.	R/W	000
2	<b>reboot</b> This bit is used to cause the on board FPGA to boot itself to the configuration image selected by bits(5:3) of this register (config_image_id). Write a '1' to this bit to initiate the re-programming of the FPGA. The FPGA will immediately become inaccessible until the re-programming completes. Therefore it is necessary to wait TBD ms after asserting this bit before attempting to access the FPGA again.	W/O	0
1	<b>reprogram</b> This bit is used to enable the loading of new image data to the FPGA's serial EEPROM. 1 = enable re-programming of EEPROM 0 = disable re-programming of EEPROM	R/W	0
0	<b>reconfig_data_reg_rdy</b> This bit is used is a flow control indicator for the host. The host should poll this bit after performing a write to register reconfig_data to know when a new data byte can be loaded. 1 = reconfig_data register ready for new data byte. 0 = reconfig_data register not ready for new data byte.	R/O	1

**Table 5-24 Reconfiguration Control Register**



Name	<b>reconfig_data</b>		
	<b>NOTE: This register function available upon request! Not present in standard configuration.</b>		
Address	<b>0x1D</b>		
Bit	Description	Type	Reset Value
7:0	This is a write only register that is used for loading new configuration data to the FMC-200 serial EEPROM. Any write to this register while register reconfig_ctrl(1)=reprogram is asserted will send the data byte to the configuration image selected by reconfig_ctrl(5:3)=config_image_id.	WO	-

**Table 5-25 Reconfiguration Data Register**

Name	<b>revision_control</b>		
Address	<b>0x1F</b>		
Bit	Description	Type	Reset Value
7	<b>Dual_mode_capable</b> 0 = Dual base camera mode not supported. 1 = Dual base camera mode supported.	R/O	-
6	<b>PoCL_capable</b> 0 = Power over Camera Link not supported. 1 = Power over Camera Link supported.	R/O	-
5:0	<b>Revision_code</b> Integre Technologies use only.	R/O	2

**Table 5-26 Revision Control**

## Chapter 6. Data Ordering and Rates

### 6.1 Camera Link Serial Data Transmit Ordering

Figure 6-1 Base, Medium, Full Configuration Port Ordering shows the 7:1 by 4 data transmit / receive sequence for **base, medium, and full Camera Link configurations**. See **Figure 4-1 Camera Link Interface Connections** and **Table 4-2 Base, Medium, Full Camera Link pinout** for details on how the valid signals and A, B, C... port data is wired through the Channel Link transmitters contained in the camera and sent over the cables to the FMC-200 receiver inputs.

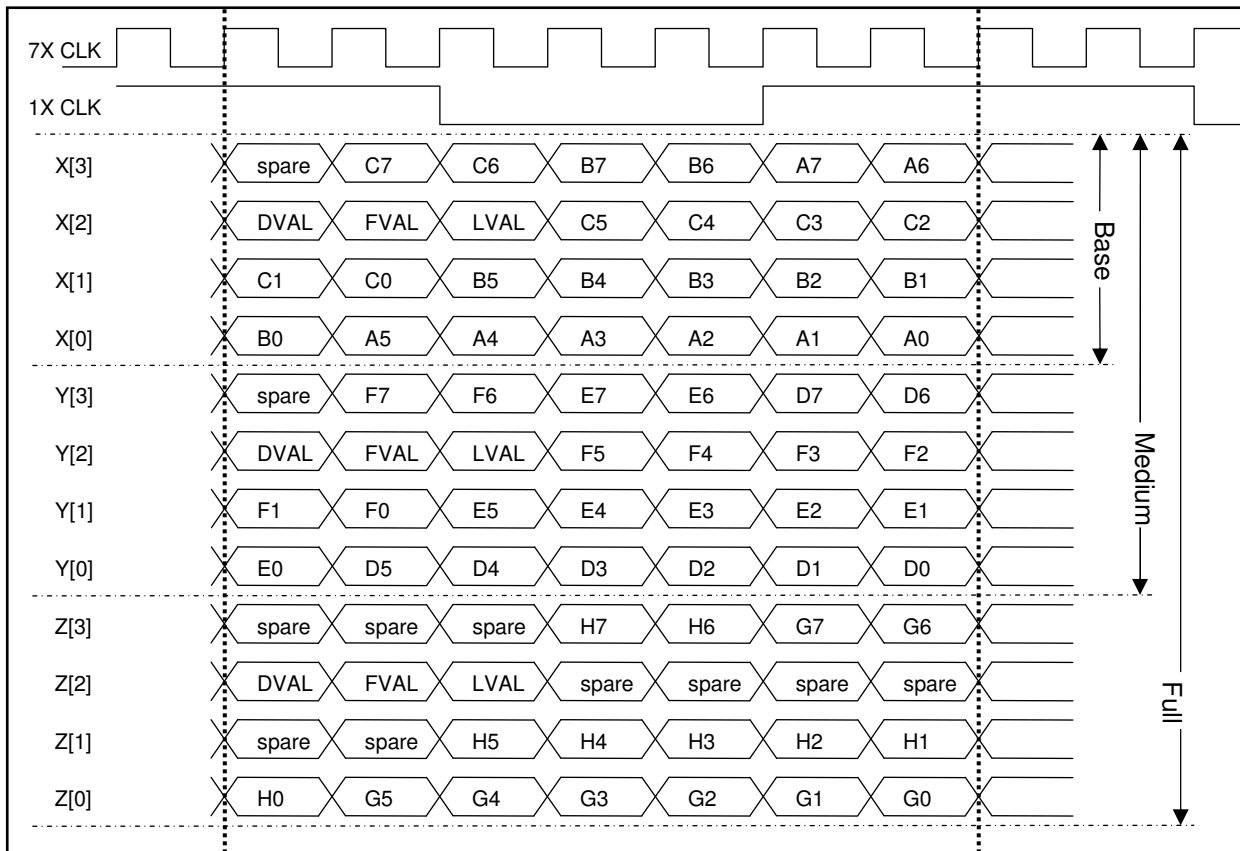
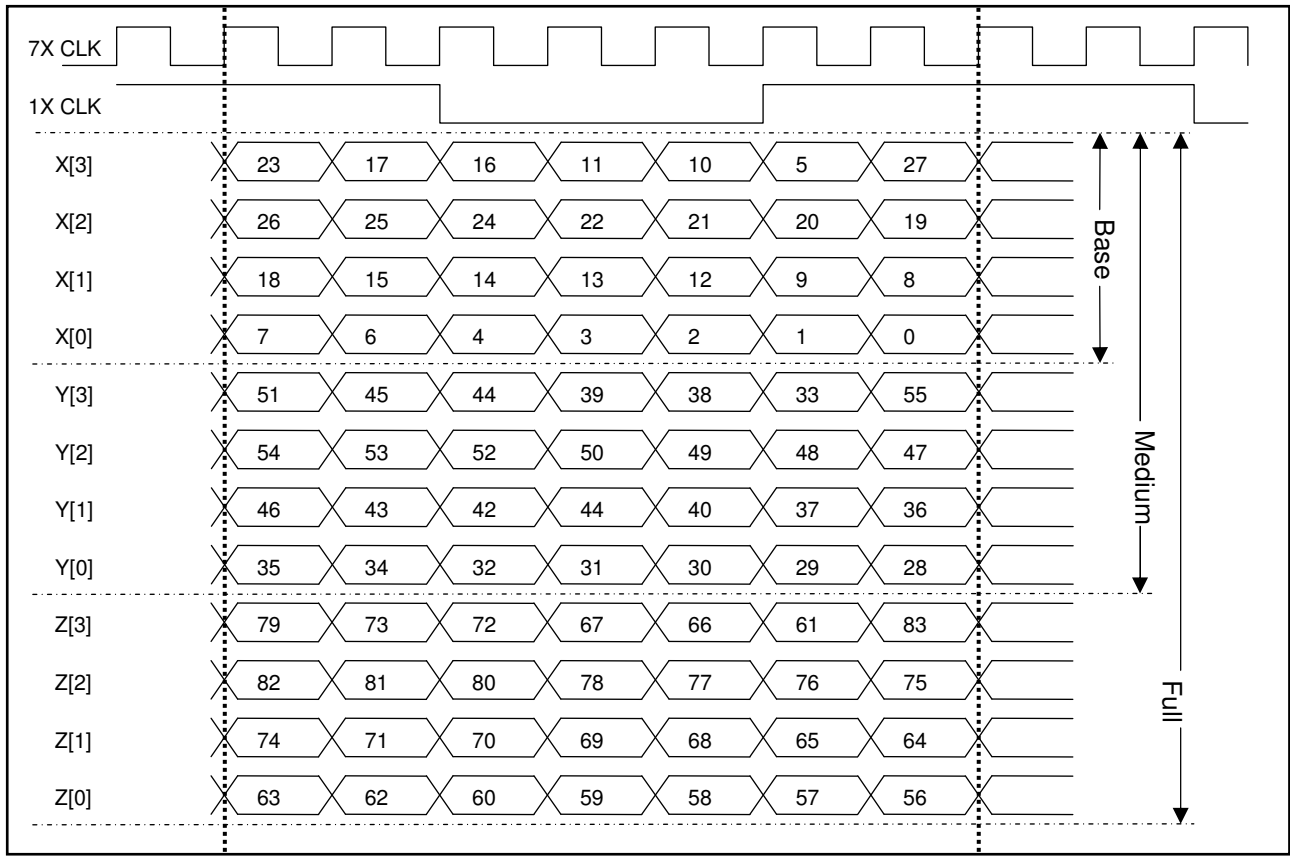


Figure 6-1 Base, Medium, Full Configuration Port Ordering



**Figure 6-2 Base, Medium, Full Configuration Serial to Parallel bus Bit map**

## 6.2 Camera Link Data Rate

The front bezel 26-pin SDR connectors provide the interface to Camera Link v1.2 type devices. Camera Link devices transmit data as serialized 7:1 over 4 differential channels for a base configuration. The medium configuration expands this by 4 more channels; the full configuration by another 4 channels. Dedicated clocks are transmitted in parallel on separate differential pairs, one per data channel. The maximum frequency of these parallel clocks is 85MHz.

With a 7:1 x 4 transmission protocol, this corresponds to 28 bits of data transmitted per parallel clock. For the full Camera Link configuration, there are 28bits x 3 = 84 bits transmitted per clock. The **maximum data rate from the Camera Link interface is (84bits)\*(85MHz) = 7.14Gbit/sec**. It should be noted that this is the theoretical maximum using 7:1 by 4 bit transmission protocol because the Camera Link specification does not utilize all the available bits. Some of the 28 bits transmitted per parallel clock are “spare” bits.

The frequency of the **data signals received from the Camera Link interface is (7 bits/parallel clk)\*(85MHz) = 595MHz**.

### 6.3 FMC Video Data Transmit Ordering

The tables below detail the byte ordering of the decoded video data that is serialized and then sent down the FMC connector to the carrier board. The pixel data locations are based on camera configuration. The extended mode shown in Table 6-1 **is specific to a Basler A504 model camera**. Note that for this mode, the user available “Side Band” bits are shifted from bit location (87:84) to (75:72). Extended modes for other vendor cameras can be implemented upon request.

The configurations detailed in Table 6-2, Table 6-3, Table 6-4, and Table 6-5 are derived from v1.2 of the Camera Link specification.

8 bits	4 bits	4 bits	72 bits							
Channel Data	Prim Valid	Side Band	Memory Mapped Channel Data ( <b>Extended Mode</b> ) 8 bit, 10 pixel							
← 8:1 Serialization by 11 data lanes →										
10	9	8	7	6	5	4	3	2	1	0
87:80	79:72	71:64	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
P9(7:0)		P8(7:0)	P7(7:0)	P6(7:0)	P5(7:0)	P4(7:0)	P3(7:0)	P2(7:0)	P1(7:0)	P0(7:0)

**Table 6-1 FMC Byte Order—Extended Configuration (Basler A504 camera specific)**

4 bits	4 bits	4 bits	12 bits	64 bits						
Side Band	Not Used	Prim Valid	Not Used	Memory Mapped Channel Data ( <b>Full Mode</b> )						
← 8:1 Serialization by 11 data lanes →										
10	9	8	7	6	5	4	3	2	1	0
87:80	79:72	71:64	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
8 bit, 8 pixel			P7(7:0)	P6(7:0)	P5(7:0)	P4(7:0)	P3(7:0)	P2(7:0)	P1(7:0)	P0(7:0)

**Table 6-2 FMC Byte Order--Full Configuration**

4 bits	4 bits	4 bits	12 bits	64 bits						
Side Band	Not Used	Prim Valids	Not Used	Memory Mapped Channel Data ( <b>Medium Mode</b> )						
← 8:1 Serialization by 11 data lanes →										
10	9	8	7	6	5	4	3	2	1	0
87:80	79:72	71:64	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
8 bit, 4 pixel			-	-	-	-	P3(7:0)	P2(7:0)	P1(7:0)	P0(7:0)
10 bit, 3 to 4 pixel			(57:56) = P3(9:8)	P3(7:0)	(41:40) = P2(9:8)	P2(7:0)	(25:24) = P1(9:8)	P1(7:0)	(9:8) = P0(9:8)	P0(7:0)
12 bit, 3 to 4 pixel			(59:56) = P3(11:8)	P3(7:0)	(43:40) = P2(11:8)	P2(7:0)	(27:24) = P1(11:8)	P1(7:0)	(11:8) = P0(11:8)	P0(7:0)
30 bit, RGB			-	-	(41:40) = B(9:8)	B(7:0)	(25:24) = G(9:8)	G(7:0)	(9:8) = R(9:8)	R(7:0)
36 bit, RGB			-	-	(43:40) = B(11:8)	B(7:0)	(27:24) = G(11:8)	G(7:0)	(11:8) = R(11:8)	R(7:0)

**Table 6-3 FMC Byte Order--Medium Configuration**

4 bits	4 bits	4 bits	44 bits				32 bits			
Side Band	Not Used	Prim Valid	Not Used				Memory Mapped Channel Data (Base Mode)			
← 8:1 Serialization by 11 data lanes →										
10	9	8	7	6	5	4	3	2	1	0
87:80	79:72	71:64	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
8 bit, 1 to 3 pixel							-	P2(7:0)	P1(7:0)	P0(7:0)
10 bit, 1 to 2 pixel							(25:24) = P1(9:8)	P1(7:0)	(9:8) = P0(9:8)	P0(7:0)
12 bit, 1 to 2 pixel							(27:24) = P1(11:8)	P1(7:0)	(11:8) = P0(11:8)	P0(7:0)
14 bit, 1 pixel							-	-	(15:8) = P0(13:8)	P0(7:0)
16 bit, 1 pixel							-	-	P0(15:8)	P0(7:0)
24 bit, RGB							-	B(7:0)	G(7:0)	R(7:0)

**Table 6-4 FMC Byte Order—Base Configuration**

4 bits	4 bits	4 bits	4 bits	8 bits	32 bits				32 bits			
Side Band	Not Used	Prim Valid	Dual Valid	Not Used	Memory Mapped Channel Data (Camera 2, Base Mode)				Memory Mapped Channel Data (Camera 1, Base Mode)			
←8:1 Serialization by 11 data lanes→												
10	9	8	7	6	5	4	3	2	1	0		
87:80	79:72	71:64	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0		
8 bit, 1 to 3 pixel			-	P2(7:0)	P1(7:0)	P0(7:0)	-	P2(7:0)	P1(7:0)	P0(7:0)		
10 bit, 1 to 2 pixel			(57:56) = P1(9:8)	P1(7:0)	(41:40) = P0(9:8)	P0(7:0)	(25:24) = P1(9:8)	P1(7:0)	(9:8) = P0(9:8)	P0(7:0)		
12 bit, 1 to 2 pixel			(59:56) = P1(11:8)	P1(7:0)	(43:40) = P0(11:8)	P0(7:0)	(27:24) = P1(11:8)	P1(7:0)	(11:8) = P0(11:8)	P0(7:0)		
14 bit, 1 pixel			-	-	(45:40) = P0(13:8)	P0(7:0)	-	-	(13:8) = P0(13:8)	P0(7:0)		
16 bit, 1 pixel			-	-	P0(15:8)	P0(7:0)	-	-	P0(15:8)	P0(7:0)		
24 bit, RGB			-	B(7:0)	G(7:0)	R(7:0)	-	B(7:0)	G(7:0)	R(7:0)		

**Table 6-5 FMC Byte Order—Dual Base Configuration**



	Camera_DVAL	FMC_FVAL	FMC_LVAL	FMC_DVAL
	Bit Position in 88-bit word transmitted to FMC Carrier			
<b>Primary</b>	79	78	77	76
<b>Dual</b>	75	74	73	72
<b>Definition</b>	This is the “data valid” signal from the X channel of Channel Link. This signal must be used to qualify any data received by the FMC carrier.	This tracks the “frame valid” signal from the X channel of Channel Link.	This tracks the “line valid” signal from the X channel of Channel Link.	This is an FMC-200 “data valid” signal. This signal can assert high even when Camera_DVAL is not asserted. <b>All data</b> received from the Channel Link interface is passed down to the FMC carrier. When this signal is asserted, and Camera_DVAL is not asserted—this indicates a data “bubble” (no data) was received from the camera. Data “bubbles” are inherent to the FMC-200 design as the architecture relies on the camera clock running at a slower speed than the <code>fmc_vclk</code> .

**Table 6-6 Valid Bit Location in 88-bit FMC Data Word**

## 6.4 FMC Video Data Rate

The FMC-200 will re-package the incoming data from the Camera Link interface for transmission to the FMC carrier board. In order to accommodate the maximum number of data bits possible from the Camera Link (84 bits) an 8:1 serialization factor over (11) differential channels was selected. This allows the maximum data package (84 bits) to be transmitted down to the FMC carrier in (1) parallel clock. To ensure that the throughput exceeds the maximum rate of the Camera Link interface, a 85MHz parallel clock rate was selected along with a filtering scheme that removes non-image data other than that required to mark the end of line or end of frame.

With an 8:1 x 11 transmission protocol, this corresponds to 88 bits of data transmitted per parallel clock. This covers the 84 bits maximum from Camera Link, with 4 spare bits. At 85 MHz, this corresponds to a **data rate of (88bits)\*(85MHz) = 7.48 Gbit/sec**.

The frequency of the **data signals sent to the FMC carrier is (8 bits/parallel clk)\*(85MHz) = 680MHz**.

## 6.5 Summary of Data Rates

**Table 6-7 Camera Link & FMC Data Rate Summary** summarizes the data rates for the FMC Camera Link inputs, and the outputs to the FMC carrier board. **Note that a board implemented as a base only configuration using an EP3C10 or EP3C5 part can support only (5) differential channels on the FMC interface**, but this is sufficient to handle the Camera Link base configuration data rate.

Interface	Data Rate	Per pin rate
Camera Link (Full)	7 bits/chan x 12 chan x 85MHz = <b>7.140 Gbit/sec</b>	7 bits/chan x 1 chan x 85MHz = <b>595 Mbit/sec</b>
Camera Link (Medium)	7 bits/chan x 8 chan x 85MHz = <b>4.760 Gbit/sec</b>	7 bits/chan x 1 chan x 85MHz = <b>595 Mbit/sec</b>
Camera Link (Base)	7 bits/chan x 4 chan x 85MHz = <b>2.380 Gbit/sec</b>	7 bits/chan x 1 chan x 85MHz = <b>595 Mbit/sec</b>
FMC connector (EP3C16)	8 bits/chan x 11 chan x 85MHz = <b>7.480 Gbit/sec</b>	8 bits/chan x 1 chan x 85MHz = <b>680 Mbit/sec</b>
FMC connector (Base only) (EP3C10, EP3C5)	8 bits/chan x 5 chan x 85MHz = <b>3.400 Gbit/sec</b>	8 bits/chan x 1 chan x 85MHz = <b>680 Mbit/sec</b>

**Table 6-7 Camera Link & FMC Data Rate Summary**



## Chapter 7. Specifications

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### 7.1 Connectors

This section details the various connectors present on the FMC-200.

#### 7.1.1 Camera Link Camera Interface Connector

- Two 26-pin SDR connectors: supporting Base, Medium, Full, Extended, or Dual-Base configurations. (3M 12226-5150-00FR)

#### 7.1.2 FMC Connector

- 160 pin LPC (Low Pin Count) Connector: (Samtec ASP-134606-01)

#### 7.1.3 General Purpose IO Connectors

There are two general purpose connectors available on the FMC-200 and they are described below:

- Bezel Connector: 2 bidirectional single-ended signals (3.3v tolerant) and 2 bidirectional LVDS differential pairs. (Hirose DF19G-14P-1H)
- Board Header: 4 bidirectional differential pairs.(Samtec FTSH-105-03-F-DV)

#### 7.1.4 JTAG Header Connector

An Altera JTAG connector (optional) can be populated on the FMC-200 for use in re-programming the Altera FPGA. However, please note that **if this connector is present the card will not be in compliance** with the maximum height restrictions for the IO area for FMC boards. The FMC specification sets an **8mm height** restriction in the IO connector area of the board. The Altera JTAG connector is **9.7mm high**, not including the height of the associated mating connector.

- Altera JTAG Connector: (FCI 95278-101A10)