ADI Sub6GHz Development Platform
Startup and Debug Document
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REVISION HISTORY

Mar 12, 2020 — Rev 0.1  Chen, Leo  First draft
Mar 21, 2020 — Rev 0.2  Chen, Leo  Add "Overwrite FPGA Image" section
                                Add “Power Supply Voltage Test” section
                                Update "Summary of Workaround on Current Board" section
                                Update "Summary of Update for Next Design" section
Mar 27, 2020 — Rev 0.3  Chen, Leo  Add TX performance verification result
Apr 1, 2020 — Rev 0.3  Luo, Patrick  Add RX flatness test result
                                Update software operations
SYSTEM OVERVIEW

The ADRV902x (Madura) is a family of highly integrated RF agile transceivers designed for use in small cell and macro base station equipment used in advanced communications systems. The device contains four independently controlled transmitters, dedicated observation receiver inputs for monitoring transmitter channel outputs, four independently controlled receivers, integrated synthesizers, and digital signal processing functions to provide a complete transceiver solution. The device provides the high radio performance and low power consumption demanded by cellular infrastructure applications such as macro 2G/3G/4G/5G and massive MIMO base stations.

As the wireless industry evolves and rolls out 5G, most operators are seeking new business models that provide them more control of their networks and better supply chain security. One way they are seeking to do this is by developing and sponsoring the O-RAN Alliance (www.o-ran.org). O-RAN's primary objective is to enable a 'white-box' ecosystem for 5G similar to the one created for network servers a few years ago. To achieve this goal, O-RAN has created an alliance of more than 100 operators, system integrators and IC vendors who are diligently working to make this model a reality. What this offers to operators is more flexibility in network deployment, better security of their supply chain and more efficient ways to monetize that network. What it offers for integrators and IC vendors is the opportunity to more effectively connect with the needs and requirements of the operators. ADI is one of the early members of O-RAN.

Over the last five months ADI China team have been developing a Madura based Sub6G reference platform to promote whole ADI signal chain and make customer adoption easier. The target customer is mainly O-RAN system integrators, and the solution is also available for other communication systems, such as macro base stations.

The reference platform is comprised of a radio daughter-board and a FPGA motherboard. For the mother board, we can use ADS9 board with some software changes, and this is supported by Chinese Transceiver Software Team. Moreover, we work together with Intel team to develop another evaluation system with Arria 10 SoC mother board. The daughter-board is re-designed from the Madura Customer Evaluation board by Chinese Application Team, and we named it as Madura Small Cell board. This platform is designed to facilitate customer evaluation and influences their product selection. It provides a single stop option for customer evaluate with Multi-band & FDD/TDD support.

Below are the main changes of Madura SC board compared with Madura CE board:
- Add PA pre-driver stage HMC625B/ADL5611 to enable the reference platform can connect to PA EVB directly, however, not put PAs on the board to make flexibility on PA selections and partners
- Move ADP5054 from a power card to the main board
- Change single clock AD9528 to dual clock domains AD9545 to add SyncE capability needed for O-RAN
- Add ADI RF Front end products ADRF5545A/ADRF5549 for TDD channels, and switch products on ORx channels
- Make the board support middle/high RF bands simultaneously. For example, some channels support 2.6G and below, and some channels support 3.5G. Currently different Madura CE board for that
- Leave interface for external PoE EVB + ADI power brick supply

The ADS9 + Madura SC platform is shown in below figure Error! Reference source not found..
The Intel Arria 10 + Madura SC platform is shown in below figure.

This document is focus on the Madura SC board hardware development, debugging and evaluation.
HARDWARE DESIGN

CLOCK DESIGN

The high-level diagram of clock generation / distribution as below

Reference Clock Input

In default, use REFA/REFAA as the reference clock input. User can input an external clock through SMA interface (J613). With below AD9545 configuration, a 30.72MHz, +5dBm reference clock is desired.

AD9545 configuration for Madura based small cell board v1 20200212.txt

REFB/REFBB can also be configured as reference clock to receive a differential clock signal from FPGA board.

AD9545 Output

AD9545 has dual channel of DPLL synchronizes. DPLL0 has 3 differential outputs:

- OUT0A/OUT0AA: Device clock input to AD9508, HCSL 15MA, output freq is 245.76MHz
- OUT0B/OUT0BB: Sysref signal to Madura, CML 15MA
- OUT0C/OUT0CC: Sysref signal to FPGA board, CML 15MA

DPLL1 has 2 differential outputs:

- OUT1A/OUT1AA: Reserved as test port, HCSL 15MA
- OUT1B/OUT1BB: Backup of device clock to FPGA board, not used in default, HCSL 15MA

AD9508 Output

AD9508 is a clock fanout buffer with output dividers. By controlling the jumpers (P13~P20), each of the 4 outputs can be selected to divide 1, divide 2, divide 3 and divide 4 mode. This distribution of AD9508 outputs:

- OUT0: FPGA MMCM clock only for ADS9 platform, output freq is 245.76MHz
- OUT1: FPGA reference clock. The desired clock rate for ADS9 platform is 245.76MHz, and for A10 platform is 122.88MHz
- OUT2: Madura reference clock, output freq is depending on the use case
- OUT3: Reserved as test port

POWER SUPPLY DESIGN

The high-level diagram of power supply / distribution as below
The maximum power consumption data of Madura SC board is listed in the below table. This power solution can cover all the power requirement here.

<table>
<thead>
<tr>
<th>Device</th>
<th>Power Supply</th>
<th>Current Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADRV9025</td>
<td>Dig, 1.0</td>
<td>2300mA/2900mA +900mA</td>
</tr>
<tr>
<td></td>
<td>1.3V</td>
<td>1900mA/3200mA</td>
</tr>
<tr>
<td></td>
<td>1.8V</td>
<td>660mA/800mA</td>
</tr>
<tr>
<td></td>
<td>JESD, 1.0</td>
<td>450mA/400mA</td>
</tr>
<tr>
<td>AD9543</td>
<td>VDDIO, 1.8~3.3V</td>
<td>8mA</td>
</tr>
<tr>
<td></td>
<td>VDD, 1.8V</td>
<td>430mA</td>
</tr>
<tr>
<td>AD9508*2</td>
<td>VDD, 3.3V</td>
<td>213*2mA</td>
</tr>
<tr>
<td>ADL5611*4</td>
<td>VDD, 5V</td>
<td>124*4mA</td>
</tr>
<tr>
<td>ADF5546*4</td>
<td>VDD, 5V</td>
<td>86*4mA</td>
</tr>
</tbody>
</table>

There are some compatible designs:
• Compatible design of Madura synthesizers power supply. In default, it uses 1.0V and bypass the Madura internal LDO. As the internal LDO is fully verified currently, we'll rework the board to use 1.3V power supply and enable the Madura internal LDO. Refer to "Enable Madura Internal LDO" section for details
• Compatible design of VIF. In default, it uses on-board power supply from ADP5054 CH3. The other option is the power supply from FPGA (through FMC interface)
• Compatible design of 3.3V for AD9508. In default, it uses on-board power supply from ADM7171. The other option is the power supply from FPGA (through FMC interface)

We leave an interface for external PoE EVB + ADI power brick supply, this can be selected by S1.

**RF FRONT END DESIGN**

The high-level diagram of RF front end as below.
**TX Channels**

TX1 use high band matching (2.8G~6GHz) for Madura, connect to HMC625B (DVGA) as the pre-drive amplifier. Mainly for 3.5GHz band verifications. In default, the TX signal is output at TX1_ANT port, user can also output the TX signal through TX1_TRX port by switch a 0ohm resistor on board.

TX2 use high band matching (2.8G~6GHz) for Madura, connect to ADL5611 as the pre-drive amplifier. Mainly for 3.5GHz band verifications. In default, the TX signal is output at TX2_ANT port, user can also output the TX signal through TX2_TRX port by switch a 0ohm resistor on board.

TX3 use middle band matching (0.65G~2.8GHz) for Madura, connect to ADL5611 as the pre-drive amplifier. Mainly for 2.6GHz band verifications. In default, the TX signal is output at TX3_ANT port, user can also output the TX signal through TX3_TRX port by switch a 0ohm resistor on board.

TX4 use middle band matching (0.65G~2.8GHz) for Madura, connect to HMC625B (DVGA) as the pre-drive amplifier. Mainly for 2.6GHz band verifications. In default, the TX signal is output at TX4_ANT port, user can also output the TX signal through TX4_TRX port by switch a 0ohm resistor on board.

**RX Channels**

RX1/RX2 use high band matching (2.8G~6GHz) for Madura. A dual channel RFFE module (ADRF5545A, SW+LNA) is added on the RX antenna side, the working band of this module is 2.4G~4.2GHz. These two RX channels are mainly for 3.5GHz band verifications. A compatible design of SAW filter is added after the RFFE module but bypassed in default. The main RX input is RX_ANT port, user can also input the RX signal through RX_TRX port by switch a 0ohm resistor on board.

RX3/RX4 use middle band matching (0.65G~2.8GHz) for Madura. A dual channel RFFE module (ADRF5549, SW+LNA) is added on the RX antenna side, the working band of this module is 1.8G~2.8GHz. These two RX channels are mainly for 2.6GHz band verifications.
verifications. A compatible design of SAW filter is added after the RFFE module but bypassed in default. The main RX input is RX_ANT port, user can also input the RX signal through RX_TRX port by switch a 0ohm resistor on board.

**ORX Channels**

ORX1/ORX2 use high band matching (2.8G~6GHz) for Madura and mainly for 3.5GHz band verifications. A compatible design is added to use a RFSW (HMC8038) loop back dual channel's data through ORX2 path (both TX1 and TX2 data loopback to ORX2 and selected by RFSW), this is a typical design for 4T4R2ORX applications. However, we still use 4T4R4ORX application in default, then TX1 data will loopback to ORX1 and TX2 data will loopback to ORX2 (RFSW always switch to ORX2_ANT port).

ORX3/ORX4 use middle band matching (0.65G~2.8GHz) for Madura and mainly for 2.6GHz band verifications. A compatible design is added to use a RFSW (HMC8038) loop back dual channel’s data through ORX3 path (both TX3 and TX4 data loopback to ORX3 and selected by RFSW), this is a typical design for 4T4R2ORX applications. However, we still use 4T4R4ORX application in default, then TX3 data will loopback to ORX3 (RFSW always switch to ORX3_ANT port) and TX4 data will loopback to ORX4.

**GPIO Controls of RFFE**

Below is the GPIO control truth table.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Function</th>
<th>High Level Control</th>
<th>Low Level Control</th>
<th>Power Up/Down</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO_RFFE_5V_0</td>
<td>ADL5611/HMC625B TX1&amp;TX2 POWER</td>
<td>POWER OFF</td>
<td>POWER ON</td>
<td>HIGH</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_1</td>
<td>ADL5611/HMC625B TX3&amp;TX4 POWER</td>
<td>POWER OFF</td>
<td>POWER ON</td>
<td>HIGH</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_2</td>
<td>ADRF5545 SWCTRL_CHAB (RX12)</td>
<td>RX TO TERM(TRANSMIT)</td>
<td>RX TO LNA(RECEIVE)</td>
<td>HIGH</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_3</td>
<td>ADRF5545 BP_CHA (RX1)</td>
<td>2ND LNA BYPASS</td>
<td>2ND LNA ENABLE</td>
<td>LOW</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_4</td>
<td>ADRF5545 PD_CHAB (RX12)</td>
<td>LNA POWER DOWN</td>
<td>LNA POWER UP</td>
<td>HIGH</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_5</td>
<td>ADRF5545 BP_CHB (RX2)</td>
<td>2ND LNA BYPASS</td>
<td>2ND LNA ENABLE</td>
<td>LOW</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_6</td>
<td>ADRF5549 SWCTRL_CHAB (RX34)</td>
<td>RX TO TERM(TRANSMIT)</td>
<td>RX TO LNA(RECEIVE)</td>
<td>HIGH</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_7</td>
<td>ADRF5549 BP_CHA (RX3)</td>
<td>2ND LNA BYPASS</td>
<td>2ND LNA ENABLE</td>
<td>LOW</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_8</td>
<td>ADRF5545 PD_CHAB (RX34)</td>
<td>LNA POWER DOWN</td>
<td>LNA POWER UP</td>
<td>HIGH</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_9</td>
<td>ADRF5545 BP_CHB (RX4)</td>
<td>2ND LNA BYPASS</td>
<td>2ND LNA ENABLE</td>
<td>LOW</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_10</td>
<td>CONTROL HMC8038 ORX12</td>
<td>SWITCH TO ORX1 ANT</td>
<td>SWITCH TO ORX2 ANT</td>
<td>LOW</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_11</td>
<td>CONTROL HMC8038 ORX34</td>
<td>SWITCH TO ORX4 ANT</td>
<td>SWITCH TO ORX3 ANT</td>
<td>LOW</td>
</tr>
</tbody>
</table>

There is a compatible design of using FPGA GPIO or Madura GPIO to control the RF front end devices. In default, we suggest using FPGA GPIO control, then user need to connect Pin 1 and Pin 2 of the jumpers P1 ~ P12. For Madura GPIO control, we use Madura analog GPIO to control the LNA bypass pins, this can be used to verify the Madura special gain table and AGC feature.
Refer to the "ADG3308(1.8->5V LEVEL SHIFTER) ISSUES" section, to solve the ADG3308 drive strength problem, we got some workaround on current design. Then TX channel control signals (GPIO_RFFE_5V_0 and GPIO_RFFE_5V_1) will force low, and RX control signals (GPIO_RFFE_5V_2 to GPIO_RFFE_5V_9) will use 1.8V control interface directly.

**HMC625B Attenuation Control**

The default attenuation when HMC625B power up is -31.5dB (max attenuation). User can use 3-wire SPI interface to configure the attenuation.

**Serial Control Interface**

The HMC625BLP5E contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). It is activated when P/S is kept high. The 6-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. If mechanical switches were used, sufficient debouncing should be provided. When LE is high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high and CLK is masked to prevent data transition during output loading. When P/S is low, 3-wire SPI interface inputs (SERIN, CLK, LE) are disabled and serial input register is loaded asynchronously with parallel digital inputs (D0-D5). When LE is high, 6-bit parallel data is transferred to the attenuator. For all modes of operations, the DVGA state will stay constant while LE is kept low.
FMC INTERFACE
See the attached spreadsheet for the FMC interface. Both ADS9 and Intel A10 platform are included.

![ADI-Intel FMC interface_V2.xlsx](ADI-Intel_FMC_interface_V2.xlsx)

HARDWARE DESIGN RESOURCE
- Schematic
  
  ![02-059737-01-a.pdf](02-059737-01-a.pdf)

- Assemble (Can be used to check the location of a component on board)
  
  ![01-059737-01-a.pdf](01-059737-01-a.pdf)

For more design resources, please check in the below link:
SOFTWARE OPERATIONS

WRITE EEPROM INFORMATION WITH ADS9

The EEPROM file and the EEPROM written tool is here:

EEPROM.rar

Writing process:
1. Login the Linux system of ADS9 platform. IP address: 192.168.1.10; User: root; SN: analog
2. Put the “eeprom” file as attached into the director “/root/” of the ADS9 system.
3. Put the “write_eeprom” file as attached into the director “/root/” of the ADS9 system.
4. Change execution mode of “write_eeprom” by “chmod 777 write_eeprom”.
5. Run “write_eeprom” by “./write_eeprom”.

If it prints “open eeprom successfully” and the checksum = 0xfd, then the EEPROM information is correctly written.

OVERWRITE FPGA IMAGE

User need to update the FPGA image to support the SPI / GPIO controls for RF front end devices. The FPGA image is in below address. Notice this image is just for JESD204B usecases.

\chinfile01\TempShare\LeoChen\MaduraSC\ADS9_FPGA

Writing process:
1. Get the new FPGA image, and rename it as “system_top_204b.bin”
2. Login the Linux system of ADS9 platform. IP address: 192.168.1.10; User: root; SN: analog
3. cd /home/analog/platform/binaries/
4. Delete the original “system_top_204b.bin”, and put the new FPGA image in the folder
5. Change execution mode of “system_top_204b.bin” by “chmod 777 system_top_204b.bin”
6. Turn off and then turn on the ADS9 motherboard and Madura SC daughterboard to restart the system.

ADS9 PLATFORM QUICK START

The GUI and command server files are in the below address:

\chinfile01\TempShare\LeoChen\MaduraSC

The SW quick start sequence for first time use:
1. Make sure the clock jumpers in correct place (refer to “Clock Design” section)
2. Make sure the board is fully re-worked (refer to “SUMMARY OF WORKAROUND ON CURRENT BOARD” section)
3. Login the Linux system of ADS9 platform. IP address: 192.168.1.10; User: root; SN: analog
4. Put the command server file “Adrv9025ScCmdServer” into /home/analog/adrv9025_server/
5. Change execution mode of “Adrv9025ScCmdServer” by “chmod 777 Adrv9025ScCmdServer”.
6. Run command server by “./Adrv9025ScCmdServer &”
7. Unzip the GUI file (no need to setup), run the “TrxSoln.exe” in \release folder
8. Open the “TrxSoln.exe.Config” file in C:\Users\Public\AnalogDevices\Adrv9010Config, and switch on the debug function (Please make sure you have installed the standard GUI software otherwise you will not be able to find the configure file.)
9. Connect the GUI to board by click the “Connect” button

10. Load AD9545 config file in AD9545 – Config page. The default AD9545 configuration as below. Notice the reference clock input is 30.72MHz / 5dBm

```
AD9545 configuration for Madura based small cell board v1 20200212.txt
```

11. Then the GUI can be used as common TES test, refer to the “TRANSCEIVER EVALUATION SOFTWARE (TES) OPERATION” section of Madura user guide for details

The SW quick start sequence for normal use:
1. Login the Linux system of ADS9 platform. IP address: 192.168.1.10; User: root; SN: analog
2. cd /home/analog/adrv9025_server/
3. Run command server by “./Adrv9025ScCmdServer”, you have to leave the ssh window open all the time, once you close the SSH terminal window, the connection between ADS9 and GUI will lost.
4. Connect the GUI to board by click the “Connect” button
5. Load AD9545 config file in AD9545 – Config page. The default AD9545 configuration as below. Notice the reference clock input is 30.72MHz / 5dBm

```
AD9545 configuration for Madura based small cell board v1 20200212.txt
```

6. Then the GUI can be used as common TES test, refer to the “TRANSCEIVER EVALUATION SOFTWARE (TES) OPERATION” section of Madura user guide for details

INTEL A10 PLATFORM QUICK START
(TBD)
**Hardware Debug Summary**

**ADG3308(1.8→5V LEVEL SHIFTER) ISSUES**

**Problem Description**

We use ADG3308 to shift the 1.8V control signals/SPI signals from FPGA side to 5V output for RF front end controls. The main schematic as below.

![Schematic Diagram](image)

In fact, the ADG3308 output strength is only 20uA on datasheet. This is designed to drive CMOS-compatible loads. It may cause a drive strength issue if the load is current-driving, or there is a big capacitor on the load.

<table>
<thead>
<tr>
<th>Y Side</th>
<th>V&lt;sub&gt;LH&lt;/sub&gt;</th>
<th>V&lt;sub&gt;LY&lt;/sub&gt;</th>
<th>V&lt;sub&gt;OH&lt;/sub&gt;</th>
<th>V&lt;sub&gt;OLY&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input High Voltage&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Low Voltage&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output High Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitance&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Leakage Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

On the other hand, ADG3308 can translate logic levels in either the A→Y or the Y→A direction. It uses a one-shot accelerator architecture, that means the load (5V side) may impact the source (1.8V side) if the load is not in three-state mode.
However, the digital control signal input current requirement or the capacitance of some parts on our board is higher than ADG3308 output capability, in addition, we added some 10kohm pull up / pull down resistors as well as shunt capacitors near the loads. This makes the output voltage drop a lot. I arranged the GPIO for RFFE control signal and load information as below.
<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Function</th>
<th>Extra component on Load (5V side)</th>
<th>Extra Component on Source (1.8V side)</th>
<th>Load Current Spec</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO_RFFE_5V_0</td>
<td>ADL5611/HMC625B TX1&amp;TX2 POWER</td>
<td>10K pull up // 2</td>
<td></td>
<td>P-MOS FET*2, low current but big Capacitance</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_1</td>
<td>ADL5611/HMC625B TX3&amp;TX4 POWER</td>
<td>10K pull up // 2</td>
<td></td>
<td>P-MOS FET * 2, low current but big Capacitance</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_2</td>
<td>ADRF5545 SWCTRL_CHAB (RX12)</td>
<td>10K pull up</td>
<td></td>
<td>0.4uA</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_3</td>
<td>ADRF5545 BP_CHA (RX1)</td>
<td>10K pull down</td>
<td></td>
<td>190uA</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_4</td>
<td>ADRF5545 PD_CHAB (RX12)</td>
<td>10K pull up</td>
<td></td>
<td>190uA</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_5</td>
<td>ADRF5545 BP_CHB (RX2)</td>
<td>10K pull down</td>
<td></td>
<td>190uA</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_6</td>
<td>ADRF5549 SWCTRL_CHAB (RX34)</td>
<td>10K pull up</td>
<td></td>
<td>0.4uA</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_7</td>
<td>ADRF5549 BP_CHA (RX3)</td>
<td>10K pull up</td>
<td></td>
<td>400uA</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_8</td>
<td>ADRF5545 PD_CHAB (RX34)</td>
<td>10K pull up</td>
<td></td>
<td>200uA</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_9</td>
<td>ADRF5545 BP_CHB (RX4)</td>
<td>10K pull down</td>
<td></td>
<td>400uA</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_10</td>
<td>CONTROL HMC8038 ORX12</td>
<td>10K pull down + 100p shunt</td>
<td></td>
<td>1uA</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_11</td>
<td>CONTROL HMC8038 ORX34</td>
<td>10K pull down + 100p shunt</td>
<td></td>
<td>1uA</td>
</tr>
<tr>
<td>SPI_5V_CS0</td>
<td>HMC625B TX1&amp;TX2 SPI CS</td>
<td>100p shunt</td>
<td>10K pull up</td>
<td>1uA</td>
</tr>
<tr>
<td>SPI_5V_CS1</td>
<td>HMC625B TX3&amp;TX4 SPI CS</td>
<td>100p shunt</td>
<td>10K pull up</td>
<td>1uA</td>
</tr>
<tr>
<td>SPI_5V_DIN</td>
<td>HMC625B SPI DIN</td>
<td>100p shunt</td>
<td></td>
<td>1uA</td>
</tr>
<tr>
<td>SPI_5V_CLK</td>
<td>HMC625B SPI CLK</td>
<td>100p shunt</td>
<td></td>
<td>1uA</td>
</tr>
</tbody>
</table>

**Solution for ADRF554x**

The control signal voltage requirement of ADRF554x as below:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWCTRL-ChAB, PD-ChAB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low (V_i)</td>
<td></td>
<td>0</td>
<td>0.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>High (V_i)</td>
<td></td>
<td>1.4</td>
<td>VDD</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>BP-ChA, BP-ChB</td>
<td></td>
<td>0</td>
<td>0.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low (V_i)</td>
<td></td>
<td>1.0</td>
<td>VDD</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>High (V_i)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The tested data for GPIOs used to control ADRF554x (GPIO_RFFE_5V_2 ~ GPIO_RFFE_5V_9) as below. The items in red color cannot meet the requirement of ADRF554x, which makes the part working in abnormal status.
<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Extra component on load (5V side)</th>
<th>Load Current Spec</th>
<th>Actual level when logic high (5V side)</th>
<th>Actual level when logic low (5V side)</th>
<th>Actual level when logic high (1.8V side)</th>
<th>Actual level when logic low (1.8V side)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO_RFFE_5V_2</td>
<td>10K pull up</td>
<td>0.4μA</td>
<td>5</td>
<td>1.2</td>
<td>1.8</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_3</td>
<td>10K pull down</td>
<td>190μA</td>
<td>2.2</td>
<td>0</td>
<td>1.8</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_4</td>
<td>10K pull up</td>
<td>190μA</td>
<td>3.5</td>
<td>1.1</td>
<td>1.8</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_5</td>
<td>10K pull down</td>
<td>190μA</td>
<td>2.2</td>
<td>0</td>
<td>1.8</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_6</td>
<td>10K pull up</td>
<td>0.4μA</td>
<td>5</td>
<td>1.3</td>
<td>1.8</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_7</td>
<td>10K pull down</td>
<td>400μA</td>
<td>0.6</td>
<td>0</td>
<td>1.4</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_8</td>
<td>10K pull up</td>
<td>200μA</td>
<td>0.6</td>
<td>1.1</td>
<td>1.3</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_9</td>
<td>10K pull down</td>
<td>400μA</td>
<td>0.7</td>
<td>0</td>
<td>1.4</td>
<td>0</td>
</tr>
</tbody>
</table>

To solve this problem, we can remove the level shifter, and use 1.8V GPIO to control AD554x directly. The detail modification as below:

1) Remove U10, connect 1.8V control signals from P1~P8 to P21 directly.
2) Remove R187, R192, R189, R245, R250, R246
3) Replace R76 / R 218 with 30kohm resistor

The test result after the modifications is in below table. The control logic is ok, and the device works correctly with this control logic.
<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Extra component on load (5V side)</th>
<th>Load Current Spec</th>
<th>Power up default status</th>
<th>Actual level when logic high</th>
<th>Actual level when logic low</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO_RFFE_5V_2</td>
<td>30K pull up</td>
<td>0.4uA</td>
<td>5</td>
<td>1.8</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_3</td>
<td></td>
<td>190uA</td>
<td>0.2</td>
<td>1.8</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_4</td>
<td></td>
<td>190uA</td>
<td>0.1</td>
<td>1.8</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_5</td>
<td></td>
<td>190uA</td>
<td>0.2</td>
<td>1.8</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_6</td>
<td>30K pull up</td>
<td>0.4uA</td>
<td>5</td>
<td>1.8</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_7</td>
<td></td>
<td>400uA</td>
<td>0.2</td>
<td>1.8</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_8</td>
<td></td>
<td>200uA</td>
<td>0.1</td>
<td>1.8</td>
<td>0</td>
</tr>
<tr>
<td>GPIO_RFFE_5V_9</td>
<td></td>
<td>400uA</td>
<td>0.2</td>
<td>1.8</td>
<td>0</td>
</tr>
</tbody>
</table>

**Solution for HMC8038**

The control signal voltage requirement of HMC8038 as below:

<table>
<thead>
<tr>
<th>State</th>
<th>$V_{DD}$ = 3.3 V (±5% $V_{DD}$, $T_{CASE}$ = -40°C to +105°C)</th>
<th>$V_{DD}$ = 5 V (±5% $V_{DD}$, $T_{CASE}$ = -40°C to +105°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low ($V_{IL}$)</td>
<td>0 V to 0.85 V at $&lt;1 \mu A$, typical</td>
<td>0 V to 1.20 V at $&lt;1 \mu A$, typical</td>
</tr>
<tr>
<td>High ($V_{IH}$)</td>
<td>1.15 V to 3.3 V at $&lt;1 \mu A$, typical</td>
<td>1.55 V to 5.0 V at $&lt;1 \mu A$, typical</td>
</tr>
</tbody>
</table>

We use GPIO_RFFE_5V_10 ~ GPIO_RFFE_5V_11 to control HMC8038. Although the control signal current requirement is very low for this part, we added a 10K pull up resistor and a 100pF capacitor on the load side, this makes the control signals work abnormal.

To solve this problem, we can do below modifications:

1) Remove C231, C232
2) Replace R36 / R 39 with 30kohm resistor

The test result after the modifications as below. The control logic is ok, and the device works correctly.
### Solution for TX Power Control

We use a P-MOS FET to do the power control of ADL5611 and HMC625B. The main circuit as below.

![Circuit Diagram](image)

We use GPIO_RFFE_5V_0 ~ GPIO_RFFE_5V_1 to control the P-MOS FET. However, the control signals cannot drive this P-MOS FET correctly, and the voltage on the 5V GPIO will drop to 1.8~2.1V because of the big capacitance of this part.

![Graph](image)
A simple solution is to force GPIO_RFFE_5V_0 and GPIO_RFFE_5V_1 low by connecting them to GND. See the details below:

1) Connect P22_Pin3 to P22_Pin2
2) Connect P22_Pin4 to P21_Pin2

Solution for HMC625B SPI Bus

The ADG3308 also causes SPI issue. The SPI slaves (Madura or AD9545) cannot work correctly because of the SPI signal quality is too bad. See the below figure for the SPI CLK / CS / DIN signals measured on the Madura SC board.
Compared with the hardware of Madura CE board, there are two more SPI buses for HMC625B controls. If disconnect SPI connection of these two components, then the SPI for Madura and AD9545 can work correctly.

With further debug, we found the HMC625B is fully power off in default, which is controlled by GPIO_RFFE_5V_0 and GPIO_RFFE_5V_1. In addition, there are 100pf shunt capacitors on HMC625B SPI pins. This makes the load of SPI bus is very heavy and uncertain. Remove the shunt capacitors and force power on HMC625B can solve this problem.
However, the problem seems more complex when verifying the SPI_Dout. If the SPI_CS2 / SPI_CS3 signals are not controlled by FPGA (current SW version not support SPI_CS2/3), then the default voltage on SPI_5V_CS0/SPI_5V_CS1 is 0V, and this will make the SPI_CS2 / SPI_CS3 signals in 1.8V side drop to 0.6~0.7V (even a 10kohm pull up resistor is added in 1.8V side).

We use a logic component as below to select the SPI_Dout source. If SPI_CS2 or SPI_CS3 is 0.6V~0.7V, then the DOUT from HMC625B (a low level) will add to SPI_DOUT pin and impact the normal DOUT from AD9545 or Madura.
Although the SPI_Dout issue only occurs when SPI_CS2 and SPI_CS3 don't controlled by FPGA (three-state for FPGA IO), we need to find out a solution to avoid any potential risks. Fortunately, we don't really need 4-wire mode to control HMC625B, a simplest way is removing U13 (The DOUT output Mux for HMC625B).

The detail modifications for SPI issue as below:
1) Force TX channels power up (See Solution for TX Power Control section)
2) Remove C223, C224, C227, C225, C219, C226
3) Remove U13

With this modification we can get correct SPI operations for all SPI slaves. See the test result is below:

1.8V SPI for Madura:

5V SPI for HMC625B
LED OF POWER SUPPLY INDICTOR

The LED used for 12V power input is too dazzling because of a new part number is used instead of the previous part in Madura CE board. **Change the value of R802 from 1K to 15K** can solve this problem.

![LED Diagram]

ENABLE MADURA INTERNAL LDO

In default design, we still bypass the Madura internal LDO. As the internal LDO is fully verified currently. It’s better to re-work the board to use 1.3V power supply and enable the Madura internal LDO, this will match with current SW configuration. See the details below:

1) Remove R909, R911, R913, R919
2) Add R910, R912, R914, R920 with 0ohm resistors
POWER SUPPLY VOLTAGE TEST

Below is the power supply voltage test result. The voltage is tested in below cases:

Case 1: The board just power up, without any configurations for all the components.

Case 2: Clock and Madura initialized successfully. Madura initialized with UC51LS and all TX/RX channels on with max gain; ADRF554X LNA/SW on; HMC625 in max gain state; ADL5611 on.
I found some of the 1.8V power supply is a little low (still in the range of power supply requirement), this is mainly because of the ferrite bead. See the below comparison of the voltage before / after ferrite bead in case 3:
<table>
<thead>
<tr>
<th>Power Supply</th>
<th>Test Port</th>
<th>Target / V</th>
<th>Before Bead / V</th>
<th>After Bead / V</th>
</tr>
</thead>
<tbody>
<tr>
<td>VANA_1P8_CLK</td>
<td>TP8</td>
<td>1.800</td>
<td>1.778</td>
<td>1.716</td>
</tr>
<tr>
<td>VANA2_1P8</td>
<td>TP810</td>
<td>1.800</td>
<td>1.761</td>
<td>1.739</td>
</tr>
<tr>
<td>VANA1_1P8</td>
<td>TP809</td>
<td>1.800</td>
<td>1.780</td>
<td>1.758</td>
</tr>
<tr>
<td>VCONV1_1P8</td>
<td>TP813</td>
<td>1.800</td>
<td>1.779</td>
<td>1.763</td>
</tr>
</tbody>
</table>

As aligned with Jim and Rico, we decide to increase the 1.8V source voltage of ADP5054 by modifying the divider resistors:
- Replace R15 from 10.2K to 10K
- Replace R18 from 12.7K to 13K

Then the expected output voltage is: $0.8V \times \frac{10k+13k}{10k} = 1.84V$

Below is the 1.8V power supply voltage after this modification:

<table>
<thead>
<tr>
<th>Power Supply</th>
<th>Test Port</th>
<th>Target / V</th>
<th>Start Up / V</th>
<th>Initialized / V</th>
<th>All Channels On / V</th>
</tr>
</thead>
<tbody>
<tr>
<td>VANA_1P8_CLK</td>
<td>TP8</td>
<td>1.800</td>
<td>1.799</td>
<td>1.772</td>
<td>1.762</td>
</tr>
<tr>
<td>VANA2_1P8</td>
<td>TP810</td>
<td>1.800</td>
<td>1.839</td>
<td>1.832</td>
<td>1.784</td>
</tr>
<tr>
<td>VANA1_1P8</td>
<td>TP809</td>
<td>1.800</td>
<td>1.839</td>
<td>1.835</td>
<td>1.804</td>
</tr>
<tr>
<td>VCONV1_1P8</td>
<td>TP813</td>
<td>1.800</td>
<td>1.839</td>
<td>1.831</td>
<td>1.809</td>
</tr>
<tr>
<td>VANA3_1P8</td>
<td>TP811</td>
<td>1.800</td>
<td>1.844</td>
<td>1.842</td>
<td>1.816</td>
</tr>
<tr>
<td>VANA4_1P8</td>
<td>TP812</td>
<td>1.800</td>
<td>1.844</td>
<td>1.842</td>
<td>1.816</td>
</tr>
<tr>
<td>VCONV2_1P8</td>
<td>TP814</td>
<td>1.800</td>
<td>1.844</td>
<td>1.839</td>
<td>1.822</td>
</tr>
<tr>
<td>VJVCO_1P8</td>
<td>TP815</td>
<td>1.800</td>
<td>1.840</td>
<td>1.835</td>
<td>1.827</td>
</tr>
<tr>
<td>VIF</td>
<td>TP801</td>
<td>1.800</td>
<td>1.845</td>
<td>1.842</td>
<td>1.842</td>
</tr>
<tr>
<td>1P8V</td>
<td>TP803</td>
<td>1.800</td>
<td>1.845</td>
<td>1.844</td>
<td>1.843</td>
</tr>
</tbody>
</table>

There are some other suggestions on the PCB layout related to power supply:
1/ Strength the power supply plane of VDES_1P0 / VSER_1P0
2/ Strength the power supply plane of VANA2_1P8 / VANA1_1P8

**SUMMARY OF WORKAROUND ON CURRENT BOARD**
- Remove U10, connect 1.8V control signals from P1~P8 to P21 directly.
- Remove R187, R192, R189, R245, R250, R246
- Replace R76 / R 218 with 30kohm resistor
- Remove C231, C232
- Replace R36 / R 39 with 30kohm resistor
- Connect P22_Pin3 to P22_Pin2
- Connect P22_Pin4 to P21_Pin2
- Remove C223, C224, C227, C225, C219, C226
- Remove U13
- Replace R802 with 15kohm resistor
- Remove R909, R911, R913, R919
- Add R910, R912, R914, R920 with 0ohm resistors
- **Replace R15 from 10.2K to 10K**
- **Replace R18 from 12.7K to 13K**
SUMMARY OF UPDATE FOR NEXT DESIGN

Schematic and BOM Update

Please see the attachments for the updated schematic and BOM file based on the hardware debug result currently. The changes are about the below functions:

- Update the GPIO controls of ADRF554x, HMC8038 to solve the level shifter drive strength issue
- Modify TX channel power up / power down circuit, which cannot work correctly because of the level shifter drive strength issue
- Delete HMC625B SPI_DOUT circuit. 3-wire SPI mode is enough for HMC625B
- Set to DNI for some components / SMA connectors not in use
- Set Madura internal LDO for synthesizers in default
- Other small optimizations

Page_1:
- Update the truth table – Done

Page_2:
- Modify signal name “SPI_5V_CS0 / SPI_5V_CS1” to “SPI_5V_CS2 / SPI_5V_CS3” – Done
- Add buffer for GPIO_RFFE_5V_0 / GPIO_RFFE_5V_1 - Done
- Connect the ADRF554X pull up resistors to VIF - Done
- Add comments on the jumpers - Done
- Delete level shifter (U10), use 1.8V GPIO to control RX channels - Done
- Delete HMC625B SPI_Dout circuits (U201, U12, U13) – Done
- Update the GPIO test signals on P21 – Done
- DNI P204 (JTAG)

Page_3:
- Delete the power control circuits for TX1/4 channels (Q4,Q5) -- Done
- Modify signal name “SPI_5V_CS0 / SPI_5V_CS1” to “SPI_5V_CS2 / SPI_5V_CS3” – Done
- Delete the shunt capacitors on SPI bus - Done
- Connect HMC625B SPI_Dout to GND for debug use – Done

Page_4:
- Modify the GPIO controls to 1.8V source - Done
- Delete the pull up circuit - Done
- DNI SMA connectors on TERM ports - Done
- DNI saw filters - Done

Page_5:
- DNI SMA connectors on RX_TRX ports - Done

Page_6:
- Change HMC8038 pull up resistor to 30kohm - Done
- Remove shunt capacitors on HMC8038 control signals - Done
- Add 3dB pi attenuator for each ORX path – Done
- Modify the ORX SMA to surface mount part – To Do

Page_7:
- DNI SMA connectors on TX_TRX ports - Done
- Add low pass filters – To Do
Page 10:
- Replace R802 with 15kohm resistor - Done
- Replace R15 from 10.2K to 10K - Done
- Replace R18 from 12.7K to 13K - Done
- Use 0.1% accuracy for all ADP5054 voltage divider resistors – Done

Page 12:
- DNI the ADP1762 for 1.0V_REG - Done
- Use 1.3V power supply and enable the Madura internal LDO for synthesizers. - Done
- DNI AD7291 - Done

Page 13:
- Delete the redundant capacitors on FPGA_REF_CLK and FPGA_MMCM_CLK - Done

Other Updates on PCB
1. Strength the power supply plane of VDES_1P0 / VSER_1P0
2. Strength the power supply plane of VANA2_1P8 / VANA1_1P8
3. Make it clearer of the silk mask of test ports
4. Emphasis the silk mask of TRX SMA ports
5. It’s better to move the clock test ports to primary side of board.
RF FUNCTIONAL VERIFICATIONS

RX1/RX2 FUNCTIONAL VERIFICATION

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.5.9 debug build for Madura SC

Test Configuration:
- Use case 51 NLS
- TXLO = RXLO = LO2 = 3500MHz
- Input a CW signal at 3510MHz from signal generator

Specifications:

<table>
<thead>
<tr>
<th>Module</th>
<th>Gain</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD5545A</td>
<td>32dB</td>
<td>High Gain Mode</td>
</tr>
<tr>
<td></td>
<td>16dB</td>
<td>Low Gain Mode</td>
</tr>
<tr>
<td>PI Attenuator</td>
<td>-3dB</td>
<td></td>
</tr>
<tr>
<td>Insertion Loss of SMA and Balun</td>
<td>-1.5dB</td>
<td></td>
</tr>
<tr>
<td>Madura</td>
<td>-12dBm -&gt; -2dBfs</td>
<td>Max Gain Index</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>-39.5dBm -&gt; -2dBfs</td>
<td>AD5545A High Gain Mode</td>
</tr>
<tr>
<td></td>
<td>-23.5dBm -&gt; -2dBfs</td>
<td>AD5545A High Gain Mode</td>
</tr>
</tbody>
</table>

Test Result:
## RX3/RX4 FUNCTIONAL VERIFICATION

**Test Environment:**
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.5.9 debug build for Madura SC

**Test Configuration:**
- Use case 51 NLS
  - TXLO = RXLO = LO2 = 2600MHz
  - Input a CW signal at 2610MHz from signal generator

**Specifications:**

<table>
<thead>
<tr>
<th>Module</th>
<th>Gain</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD5549</td>
<td>35dB</td>
<td>High Gain Mode</td>
</tr>
<tr>
<td></td>
<td>17dB</td>
<td>Low Gain Mode</td>
</tr>
<tr>
<td>PI Attenuator</td>
<td>-3dB</td>
<td></td>
</tr>
<tr>
<td>Insertion Loss of SMA and Balun</td>
<td>-1.5dB</td>
<td></td>
</tr>
<tr>
<td>Madura</td>
<td>-12dBm -&gt; -2dBfs</td>
<td>Max Gain Index</td>
</tr>
</tbody>
</table>

- **Total**
  - -39.5dBm -> -2dBfs AD5545A High Gain Mode
  - -23.5dBm -> -2dBfs AD5545A High Gain Mode
Test Result:

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Target / dBFs</th>
<th>Test Result / dBFs</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX3, Input from RFFE (3510MHz, -45dBm), AD5549 high gain mode</td>
<td>-4.5</td>
<td>-6.3</td>
</tr>
<tr>
<td>RX3, Input from RFFE (3510MHz, -45dBm), AD5549 low gain mode</td>
<td>-22.5</td>
<td>-23.6</td>
</tr>
<tr>
<td>RX3, Input from RFFE (3510MHz, -20dBm), AD5549 isolation mode</td>
<td>-</td>
<td>-82.8</td>
</tr>
<tr>
<td>RX3, Input from RX_TRX (3510MHz, -20dBm), AD5549 low gain mode</td>
<td>-10</td>
<td>-10.4</td>
</tr>
<tr>
<td>RX4, Input from RFFE (3510MHz, -45dBm), AD5549 high gain mode</td>
<td>-4.5</td>
<td>-6.2</td>
</tr>
<tr>
<td>RX4, Input from RFFE (3510MHz, -45dBm), AD5549 low gain mode</td>
<td>-22.5</td>
<td>-23.4</td>
</tr>
<tr>
<td>RX4, Input from RFFE (3510MHz, -20dBm), AD5549 isolation mode</td>
<td>-</td>
<td>-83.8</td>
</tr>
<tr>
<td>RX4, Input from RX_TRX (3510MHz, -20dBm), AD5549 low gain mode</td>
<td>-10</td>
<td>-10.7</td>
</tr>
</tbody>
</table>

**ORX1/ORX2 FUNCTIONAL VERIFICATION**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.5.9 debug build for Madura SC

Test Configuration:
- Use case 51 LS

- TXLO = RXLO = LO2 = 3500MHz
- Input a CW signal at 3510MHz from signal generator

Specifications:

<table>
<thead>
<tr>
<th>Module</th>
<th>Gain</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>HMC8038</td>
<td>-0.8dB</td>
<td></td>
</tr>
<tr>
<td>Insertion Loss of SMA and Balun</td>
<td>-1.5dB</td>
<td></td>
</tr>
<tr>
<td>Madura</td>
<td>-12dBm -&gt; -2dBFS</td>
<td>Max Gain Index</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>-10.5dBm -&gt; -2dBFS</strong></td>
<td>For ORX1, bypass HMC8038</td>
</tr>
<tr>
<td></td>
<td><strong>-9.7dBm -&gt; -2dBFS</strong></td>
<td>For ORX2, include HMC8038</td>
</tr>
</tbody>
</table>
Test Result:

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Target / dBFs</th>
<th>Test Result / dBFs</th>
</tr>
</thead>
<tbody>
<tr>
<td>ORX1 (3510MHz, -20dBm), bypass HMC8038</td>
<td>-11.5</td>
<td>-14.7</td>
</tr>
<tr>
<td>ORX2 (3510MHz, -20dBm), include HMC8038</td>
<td>-12.3</td>
<td>-13.4</td>
</tr>
</tbody>
</table>

- ORX1 loss is 3dB higher than expected.

**ORX3/ORX4 FUNCTIONAL VERIFICATION**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.5.9 debug build for Madura SC

Test Configuration:
- Use case 51 LS

<table>
<thead>
<tr>
<th>USE CASE</th>
<th>TX BW</th>
<th>TX INPUT RATE</th>
<th>TX DAC RATE</th>
<th>ORX BW</th>
<th>ORX OUTPUT RATE</th>
<th>ORX ADC RATE</th>
<th>RX BW</th>
<th>RX OUTPUT RATE</th>
<th>RX ADC RATE</th>
<th>JESD NP TX / RX / ORX</th>
<th>LANE RATE TEX / RX / ORX</th>
</tr>
</thead>
<tbody>
<tr>
<td>51_linkSharing</td>
<td>450.000 MHz</td>
<td>245.760 MHz</td>
<td>1.966 GHz</td>
<td>450.000 MHz</td>
<td>245.760 MHz</td>
<td>2.458 MHz</td>
<td>200.000 MHz</td>
<td>245.760 MHz</td>
<td>4.915 MHz</td>
<td>16 / 16 / 16</td>
<td>9830.4 / 9830.4 / 9830.4</td>
</tr>
</tbody>
</table>

- TXLO = RXLO = LO2 = 2600MHz
- Input a CW signal at 2610MHz from signal generator

Specifications:

<table>
<thead>
<tr>
<th>Module</th>
<th>Gain</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>HMC8038</td>
<td>-0.8dB</td>
<td></td>
</tr>
<tr>
<td>Insertion Loss of SMA and Balun</td>
<td>-1.5dB</td>
<td></td>
</tr>
<tr>
<td>Madura</td>
<td>-12dBm -&gt; -2dBFs</td>
<td>Max Gain Index</td>
</tr>
<tr>
<td>Total</td>
<td>-10.5dBm -&gt; -2dBFs</td>
<td>For ORX4, bypass HMC8038</td>
</tr>
<tr>
<td></td>
<td>-9.7dBm -&gt; -2dBFs</td>
<td>For ORX3, include HMC8038</td>
</tr>
</tbody>
</table>

Test Result:

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Target / dBFs</th>
<th>Test Result / dBFs</th>
</tr>
</thead>
<tbody>
<tr>
<td>ORX3 (2610MHz, -20dBm), include HMC8038</td>
<td>-12.3</td>
<td>-13.9</td>
</tr>
<tr>
<td>ORX4 (2610MHz, -20dBm), bypass HMC8038</td>
<td>-11.5</td>
<td>-11.8</td>
</tr>
</tbody>
</table>

**TX1 FUNCTIONAL VERIFICATION**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.5.9 debug build for Madura SC
Test Configuration:
- Use case 51 NLS

- TXLO = RXLO = LO2 = 3500MHz
- Output a CW signal with 5MHz offset with TXLO, bb back off = -10dBFS, RF ATT=10dB

Specifications:

<table>
<thead>
<tr>
<th>Module</th>
<th>Gain</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Madura max output</td>
<td>7dBm</td>
<td>3 dB boost off</td>
</tr>
<tr>
<td>BB back off</td>
<td>-10dBFS</td>
<td></td>
</tr>
<tr>
<td>RF ATT</td>
<td>-10dB</td>
<td></td>
</tr>
<tr>
<td>Insertion Loss of SMA and Balun</td>
<td>-1.5dB</td>
<td></td>
</tr>
<tr>
<td>HMC625B Max Gain</td>
<td>13dB</td>
<td>Attenuation = 0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>-1.5dBm</strong></td>
<td><strong>HMC625B max gain</strong></td>
</tr>
</tbody>
</table>

Test Result:

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Target / dBm</th>
<th>Test Result / dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX1, Output of RFFE, DVGA ATT = 0dB</td>
<td>-1.5</td>
<td>-1.87</td>
</tr>
<tr>
<td>TX1, Output of RFFE, DVGA ATT = -16dB</td>
<td>-17.5</td>
<td>-17.2</td>
</tr>
<tr>
<td>TX1, Output of RFFE, DVGA ATT = -24dB</td>
<td>-25.5</td>
<td>-25</td>
</tr>
<tr>
<td>TX1, Output of RFFE, DVGA ATT = -28dB</td>
<td>-29.5</td>
<td>-28.92</td>
</tr>
<tr>
<td>TX1, Output of RFFE, DVGA ATT = -30dB</td>
<td>-31.5</td>
<td>-30.92</td>
</tr>
<tr>
<td>TX1, Output of RFFE, DVGA ATT = -31dB</td>
<td>-32.5</td>
<td>-31.91</td>
</tr>
<tr>
<td>TX1, Output of RFFE, DVGA ATT = -31.5dB</td>
<td>-33</td>
<td>-32.43</td>
</tr>
</tbody>
</table>

**TX2 FUNCTIONAL VERIFICATION**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.5.9 debug build for Madura SC

Test Configuration:
- Use case 51 NLS
TXLO = RXLO = LO2 = 3500MHz
Output a CW signal with 5MHz offset with TXLO, bb back off = -10dBFs, RF ATT=20dB

Specifications:

<table>
<thead>
<tr>
<th>Module</th>
<th>Gain</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Madura max output</td>
<td>7dBm</td>
<td>3 dB boost off</td>
</tr>
<tr>
<td>BB back off</td>
<td>-10dB</td>
<td></td>
</tr>
<tr>
<td>RF ATT</td>
<td>-20dB</td>
<td></td>
</tr>
<tr>
<td>Pi attenuator</td>
<td>-6dB</td>
<td></td>
</tr>
<tr>
<td>Insertion Loss of SMA and Balun</td>
<td>-1.5dB</td>
<td></td>
</tr>
<tr>
<td>ADL5611 Gain</td>
<td>20.3dB</td>
<td></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>-10.2dBm</strong></td>
<td></td>
</tr>
</tbody>
</table>

Test Result:

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Target / dBm</th>
<th>Test Result / dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX2, Output of RFFE</td>
<td>-10.2</td>
<td>-10.27</td>
</tr>
</tbody>
</table>

**TX3 FUNCTIONAL VERIFICATION**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.5.9 debug build for Madura SC

Test Configuration:
- Use case 51 NLS

TXLO = RXLO = LO2 = 2600MHz
Output a CW signal with 5MHz offset with TXLO, bb back off = -10dBFs, RF ATT=20dB

Specifications:

<table>
<thead>
<tr>
<th>Module</th>
<th>Gain</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Madura max output</td>
<td>7dBm</td>
<td>3 dB boost off</td>
</tr>
<tr>
<td>BB back off</td>
<td>-10dB</td>
<td></td>
</tr>
<tr>
<td>RF ATT</td>
<td>-20dB</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>-------</td>
<td></td>
</tr>
<tr>
<td>Pi attenuator</td>
<td>-6dB</td>
<td></td>
</tr>
<tr>
<td>Insertion Loss of SMA and Balun</td>
<td>-1.5dB</td>
<td></td>
</tr>
<tr>
<td>ADL5611 Gain</td>
<td>20.7dB</td>
<td></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>-9.8dBm</strong></td>
<td></td>
</tr>
</tbody>
</table>

Test Result:

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Target / dBm</th>
<th>Test Result / dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX2, Output of RFFE</td>
<td>-9.8</td>
<td>-9.02</td>
</tr>
</tbody>
</table>

**TX4 FUNCTIONAL VERIFICATION**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.5.9 debug build for Madura SC

Test Configuration:
- Use case 51 NLS
- TXLO = RXLO = LO2 = 2600MHz
- Output a CW signal with 5MHz offset with TXLO, BB back off = -10dBFS, RF ATT=10dB

Specifications:

<table>
<thead>
<tr>
<th>Module</th>
<th>Gain</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Madura max output</td>
<td>7dBm</td>
<td>3 dB boost off</td>
</tr>
<tr>
<td>BB back off</td>
<td>-10dBFS</td>
<td></td>
</tr>
<tr>
<td>RF ATT</td>
<td>-10dB</td>
<td></td>
</tr>
<tr>
<td>Insertion Loss of SMA and Balun</td>
<td>-1.5dB</td>
<td></td>
</tr>
<tr>
<td>HMC625B Max Gain</td>
<td>18dB</td>
<td>Attenuation = 0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>+3.5dBm</strong></td>
<td><strong>HMC625B max gain</strong></td>
</tr>
</tbody>
</table>

Test Result:

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Target / dBm</th>
<th>Test Result / dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX4, Output of RFFE, DVGA ATT = 0dB</td>
<td>3.5</td>
<td>0.22</td>
</tr>
<tr>
<td>TX4, Output of RFFE, DVGA ATT = -16dB</td>
<td>-12.5</td>
<td>-15.38</td>
</tr>
<tr>
<td>TX4, Output of RFFE, DVGA ATT = -24dB</td>
<td>-20.5</td>
<td>-23.22</td>
</tr>
<tr>
<td>TX4, Output of RFFE, DVGA ATT = -28dB</td>
<td>-24.5</td>
<td>-27.07</td>
</tr>
<tr>
<td>TX4, Output of RFFE, DVGA ATT = -30dB</td>
<td>-26.5</td>
<td>-29.02</td>
</tr>
<tr>
<td>TX4, Output of RFFE, DVGA ATT = -31dB</td>
<td>-27.5</td>
<td>-30.00</td>
</tr>
<tr>
<td>TX4, Output of RFFE, DVGA ATT = -31.5dB</td>
<td>-28.00</td>
<td>-30.52</td>
</tr>
</tbody>
</table>
RF PERFORMANCE VERIFICATIONS

TX GAIN FLATNESS WITH TXNCO SWEEP

TX1 Gain Flatness 3500MHz

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:

  ![Test Setup Table]

  - LO configuration:
    TXLO = RXLO = LO2 = 3500MHz
  - Attenuation settings:
    BB backoff: -12dBfs
    RF ATT = -10dB
    External ATT = 0dB

Test Method:
Use TX NCO (-12dBfs) to sweep the TX channel in -225MHz to 225MHz with 0.1MHz resolution. As RF ATT=-10dBm, External ATT = 0dB, the expected output power is -3.5dBm (refer to “TX1 FUNCTIONAL VERIFICATION” section)

Test Result:

![Test Result Graph]

Test Result analysis: 450MHz flatness = 0.98dB. Pass
TX2 Gain Flatness 3500MHz

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:

<table>
<thead>
<tr>
<th>USE CASE</th>
<th>TX BW</th>
<th>TX INPUT RATE</th>
<th>TX DAC RATE</th>
<th>ORX BW</th>
<th>ORX OUTPUT RATE</th>
<th>ORX ADC RATE</th>
<th>FIX BW</th>
<th>FIX OUTPUT RATE</th>
<th>FIX ADC RATE</th>
<th>JESD NP TX / ORX</th>
<th>LANE RATE TX / ORX</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 LinkSharing</td>
<td>450.000 MHz</td>
<td>491.520 MHz</td>
<td>1.066 GHz</td>
<td>450.000 MHz</td>
<td>491.520 MHz</td>
<td>4.915 GHz</td>
<td>200.000 MHz</td>
<td>245.750 MHz</td>
<td>4.915 GHz</td>
<td>12</td>
<td>12</td>
</tr>
</tbody>
</table>

- LO configuration:
  TXLO = RXLO = LO2 = 3500MHz
- Attenuation settings:
  BB backoff: -12dBFs
  RF ATT = -10dB
  External ATT = -6dB (pi attenuator)

Test Method:
Use TX NCO (-12dBFs) to sweep the TX channel in -225MHz to 225MHz with 0.1MHz resolution. As RF ATT=-10dBm, External ATT = -6dB, the expected output power is -2.2dBm (refer to “TX2 FUNCTIONAL VERIFICATION” section)

Test Result analysis: 450MHz flatness = 1.78dB. Pass
TX3 Gain Flatness 2600MHz

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:

<table>
<thead>
<tr>
<th>USE CASE</th>
<th>TX DW</th>
<th>TX INPUT RATE</th>
<th>TX DAC RATE</th>
<th>OPRX DW</th>
<th>OPRX OUTPUT RATE</th>
<th>FIX DW</th>
<th>FIX OUTPUT RATE</th>
<th>RX OPRX</th>
<th>RX INPUT RATE</th>
<th>RX DAC RATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>14_LinkSharing</td>
<td>450.000MHz</td>
<td>491.520 MHz</td>
<td>1.966 GHz</td>
<td>450.000 MHz</td>
<td>491.520 MHz</td>
<td>4.915 GHz</td>
<td>200.000 MHz</td>
<td>245.750 MHz</td>
<td>4.915 GHz</td>
<td>4.915 GHz</td>
</tr>
</tbody>
</table>

- LO configuration:
  TXLO = RXLO = LO2 = 2600MHz
- Attenuation settings:
  BB backoff: -12dBFs
  RF ATT = -10dB
  External ATT = -6dB (pi attenuator)

Test Method:
Use TX NCO (-12dBFs) to sweep the TX channel in -225MHz to 225MHz with 0.1MHz resolution. As RF ATT=-10dBm, External ATT = -6dB, the expected output power is -1.8dBm (refer to “TX3 FUNCTIONAL VERIFICATION” section)

Test Result:

Test Result analysis: 450MHz flatness = 0.60dB. Pass
TX4 Gain Flatness 2600MHz

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
  - LO configuration:
    TXLO = RXLO = LO2 = 2600MHz
  - Attenuation settings:
    BB backoff: -12dBfs
    RF ATT = -10dB
    External ATT = 0dB

Test Method:
Use TX NCO (-12dBfs) to sweep the TX channel in -225MHz to 225MHz with 0.1MHz resolution. As RF ATT=-10dBm, External ATT = 0dB, the expected output power is 1.5dBm (refer to “TX4 FUNCTIONAL VERIFICATION” section)

Test Result:

Test Result analysis:
The absolute output power is a little lower than spec, because the HMC625B cannot achieve 18dB maximum gain.

450MHz flatness = 1.28dB. **Pass**

**TX GAIN FLATNESS WITH TXLO SWEEP**

**TX1 Gain Flatness 2800~5000MHz**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
  - LO configuration: TXLO = RXLO = LO2
  - Attenuation settings:
    - BB backoff: -12dBFS
    - RF ATT = -10dB
    - External ATT = 0dB

Test Method:
Use TX NCO (-12dBFS) with 0 offset, and sweep the LO freq in 2800MHz to 5000MHz with 1MHz resolution. As RF ATT=-10dBm, External ATT = 0dB.

Test Result:
TX2 Gain Flatness 2800~5000MHz

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:

<table>
<thead>
<tr>
<th>USE CASE</th>
<th>TX BW</th>
<th>TX INPUT RATE</th>
<th>TX DAC RATE</th>
<th>ORX BW</th>
<th>ORX OUTPUT RATE</th>
<th>ORX ADC RATE</th>
<th>RX BW</th>
<th>RX OUTPUT RATE</th>
<th>RX ADC RATE</th>
<th>JESD NP Rx/Dx</th>
<th>LANE RATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>14_LinkSharing</td>
<td>490.000 MHz</td>
<td>491.520 MHz</td>
<td>1.6666 MHz</td>
<td>490.000 MHz</td>
<td>491.520 MHz</td>
<td>4.915 MHz</td>
<td>200.000 MHz</td>
<td>245.700 MHz</td>
<td>4.915 MHz</td>
<td>12 / 12</td>
<td>8 / 8</td>
</tr>
</tbody>
</table>

- LO configuration:
  TXLO = RXLO = LO2
- Attenuation settings:
  BB backoff: -12dBFS
  RF ATT = -10dB
  External ATT = 0dB

Test Method:
Use TX NCO (-12dBFS) with 0 offset, and sweep the LO freq in 2800MHz to 5000MHz with 1MHz resolution. As RF ATT=-10dBm, External ATT = 0dB.

Test Result:
TX3 Gain Flatness 650~2800MHz

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
  - LO configuration: TXLO = RXLO = LO2
  - Attenuation settings:
    - BB backoff: -12dBFS
    - RF ATT = -10dB
    - External ATT = 0dB

Test Method:
Use TX NCO (-12dBFS) with 0 offset, and sweep the LO freq in 650MHz to 2800MHz with 1MHz resolution. As RF ATT=-10dBm,
External ATT = 0dB.

Test Result:
TX4 Gain Flatness 650~2800MHz

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
- LO configuration:
  - TXLO = RXLO = LO2
- Attenuation settings:
  - BB backoff: -12dBFS
  - RF ATT = -10dB
  - External ATT = 0dB

Test Method:
Use TX NCO (-12dBFS) with 0 offset, and sweep the LO freq in 650MHz to 2800MHz with 1MHz resolution. As RF ATT=-10dBm, External ATT = 0dB.

Test Result:
TX SPURIOUS TEST

TX1 Spurious test

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case: UC14NLS
- LO configuration: TXLO=RXLO=LO2=3500M

Test Case 1: TX RF ATT=0, External DSA = 0. BB data = -100dBFS (no BB data), TXLOL/QEC tracking disabled
Test Case 2: TX RF ATT = -10 dB, External DSA = 0, BB data = -12 dBFS with 5 MHz offset, TXLOL/QEC tracking disabled
Test Case 3: TX RF ATT=-10dB, External DSA = 0, BB data = -12dBFs with 100MHz offset, TXLOL/QEC tracking disabled
TX2 Spurious test

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case: UC14NLS
- LO configuration: TXLO=RXLO=LO2=3500M

Test Case 1: TX RF ATT=0, External DSA = 0, BB data = -100dBFS (no BB data), TXLOL/QEC tracking disabled

Test Case 2: TX RF ATT=-10dB, External DSA = 0, BB data = -12dBFS with 5MHz offset, TXLOL/QEC tracking disabled
Test Case 3: TX RF ATT=-10dB, External DSA = 0, BB data = -12dBFS with 100MHz offset, TXLOL/QEC tracking disabled
TX3 Spurious test

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case: UC14NLS
- LO configuration: TXLO=RXLO=LO2=2600M

Test Case 1: TX RF ATT=0, External DSA = 0. BB data = -100dBFS (no BB data), TXLOL/QEC tracking disabled
Test Case 2: TX RF ATT=-10dB, External DSA = 0, BB data = -12dBfs with 5MHz offset, TXLOL/QEC tracking disabled
Test Case 3: TX RF ATT = -10dB, External DSA = 0, BB data = -12dBFS with 100MHz offset, TXLOL/QEC tracking disabled
TX4 Spurious test

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case: UC14NLS
- LO configuration: TXLO=RXLO=LO2=2600M

Test Case 1: TX RF ATT=0, External DSA = 0, BB data = -100dBFS (no BB data), TXLOL/QEC tracking disabled

![Frequency Sweep](image)

Test Case 2: TX RF ATT=-10dB, External DSA = 0, BB data = -12dBFS with 5MHz offset, TXLOL/QEC tracking disabled
Test Case 3: TX RF ATT = -10dB, External DSA = 0, BB data = -12dBFS with 100MHz offset, TXLOL/QEC tracking disabled
**TX OIP3 TEST**

**TX1 OIP3 test**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- **Use case:** UC14NLS
- LO configuration: TXLO=RXLO=LO2=3500M

Test Case 1: TX RF ATT=10, External DSA = 0. BB data tone1 = -12dBFS@-98MHz offset, BB data tone1 = -12dBFS@-96MHz offset. TXLOL/QEC tracking disabled.
Test Case 2: TX RF ATT=10, External DSA = 0. BB data tone1 = -12dBFS@3MHz offset, BB data tone1 = -12dBFS@5MHz offset. TXLOL/QEC tracking disabled.

Test Case 3: TX RF ATT=10, External DSA = 0. BB data tone1 = -12dBFS@96MHz offset, BB data tone1 = -12dBFS@98MHz offset. TXLOL/QEC tracking disabled.
TX2 OIP3 test

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case: UC14NLS
- LO configuration: TXLO=RXLO=LO2=3500M

Test Case 1: TX RF ATT=10, External DSA = 0. BB data tone1 = -12dBFs@-98MHz offset, BB data tone1 = -12dBFs@-96MHz offset. TXLOL/QEC tracking disabled.
Test Case 2: TX RF ATT=10, External DSA = 0. BB data tone1 = -12dBFS@3MHz offset, BB data tone1 = -12dBFS@5MHz offset. TXLOL/QEC tracking disabled.

Test Case 3: TX RF ATT=10, External DSA = 0. BB data tone1 = -12dBFS@96MHz offset, BB data tone1 = -12dBFS@98MHz offset. TXLOL/QEC tracking disabled.
TX3 OIP3 test

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case: UC14NLS
- LO configuration: TXLO=RXLO=LO2=2600M

Test Case 1: TX RF ATT=10, External DSA = 0. BB data tone1 = -12dBFS@-98MHz offset, BB data tone1 = -12dBFS@-96MHz offset. TXLOL/QEC tracking disabled.
Test Case 2: TX RF ATT=10, External DSA = 0. BB data tone1 = -12dBs@3MHz offset, BB data tone1 = -12dBs@5MHz offset. TXLOL/QEC tracking disabled.

Test Case 3: TX RF ATT=10, External DSA = 0. BB data tone1 = -12dBs@96MHz offset, BB data tone1 = -12dBs@98MHz offset. TXLOL/QEC tracking disabled.
**TX4 OIP3 test**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- **Use case:** UC14NLS
- **LO configuration:** TXLO=RXLO=LO2=2600M

Test Case 1: TX RF ATT=10, External DSA = 0. BB data tone1 = -12dBfs@-98MHz offset, BB data tone1 = -12dBFS@-96MHz offset. TXLOL/QEC tracking disabled.
Test Case 2: TX RF ATT=10, External DSA = 0. BB data tone1 = -12dBfs@3MHz offset, BB data tone1 = -12dBFS@5MHz offset. TXLOL/QEC tracking disabled.
Test Case 3: TX RF ATT=10, External DSA = 0. BB data tone1 = -12dBFS@96MHz offset, BB data tone1 = -12dBFS@98MHz offset. TXLOL/QEC tracking disabled.

<table>
<thead>
<tr>
<th>Tested TX Channel</th>
<th>Signal on TX output /dBm</th>
<th>Signal on TXN output /dBm</th>
<th>Isolation / dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX2</td>
<td>4.47</td>
<td>-75.9</td>
<td>80.37</td>
</tr>
<tr>
<td>TX3</td>
<td>4.47</td>
<td>-78.3</td>
<td>82.77</td>
</tr>
<tr>
<td>TX4</td>
<td>4.47</td>
<td>-75.6</td>
<td>80.07</td>
</tr>
</tbody>
</table>
TX2 – TXN Isolation Test

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case: UC14NLS
- LO configuration: TXLO=RXLO=LO2=3500M

Test Method: TX2 Send out a -12dBFs CW signal @ 10MHz offset from LO. TX ATT = 0, external DSA = 0. Add 50ohm load to all untested channels.

Test Result:

<table>
<thead>
<tr>
<th>Tested TX Channel</th>
<th>Signal on TX2 output /dBm</th>
<th>Signal on TXN output /dBm</th>
<th>Isolation / dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX2</td>
<td>6.72</td>
<td>-75.9</td>
<td>82.62</td>
</tr>
<tr>
<td>TX3</td>
<td>6.72</td>
<td>-63.7</td>
<td>70.42</td>
</tr>
<tr>
<td>TX4</td>
<td>6.72</td>
<td>-80.5</td>
<td>87.22</td>
</tr>
</tbody>
</table>

TX3 – TXN Isolation Test

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case: UC14NLS
- LO configuration: TXLO=RXLO=LO2=2600M

Test Method: TX3 Send out a -12dBFs CW signal @ 10MHz offset from LO. TX ATT = 0, external DSA = 0. Add 50ohm load to all untested channels.

Test Result:

<table>
<thead>
<tr>
<th>Tested TX Channel</th>
<th>Signal on TX3 output /dBm</th>
<th>Signal on TXN output /dBm</th>
<th>Isolation / dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX1</td>
<td>8.02</td>
<td>-72.9</td>
<td>80.92</td>
</tr>
<tr>
<td>TX2</td>
<td>8.02</td>
<td>-61.7</td>
<td>69.72</td>
</tr>
<tr>
<td>TX4</td>
<td>8.02</td>
<td>-71.6</td>
<td>79.62</td>
</tr>
</tbody>
</table>
TX4 – TXN Isolation Test

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case: UC14NLS
- LO configuration: TXLO=RXLO=LO2=2600M

Test Method: TX4 Send out a -12dBs CW signal @ 10MHz offset from LO. TX ATT = 0, external DSA = 0. Add 50ohm load to all untested channels.

Test Result:

<table>
<thead>
<tr>
<th>Tested TX Channel</th>
<th>Signal on TX4 output /dBm</th>
<th>Signal on TXN output /dBm</th>
<th>Isolation / dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX1</td>
<td>6.6</td>
<td>-69.8</td>
<td>76.4</td>
</tr>
<tr>
<td>TX2</td>
<td>6.6</td>
<td>-64.2</td>
<td>70.8</td>
</tr>
<tr>
<td>TX3</td>
<td>6.6</td>
<td>-62.4</td>
<td>69</td>
</tr>
</tbody>
</table>

RX GAIN FLATNESS TEST

RX1 Test Case 1

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
- LO configuration:
  TXLO = RXLO = LO2 = 3500MHz
- Attenuation settings:
  Rx Gain Index = 255
- Board ID:09

Test Method:
1. Set RXLO = TXLO = LO2 = 3500MHz
2. Set ADRF5545A to high power mode
3. Set a CW signal to -52.5dBm at Rx_ANT port
4. Sweep the CW frequency from 3400MHz to 3600MHz
5. Set ADRF5545A to low Power mode and repeat step3.
Test Result:

![Graph showing RX1 performance across different dBm levels.](image)

Test Result analysis:

1. For high power mode, the gain is around 39.88(dBFS-dBm), and the peak-peak Gain variation is 1.4dB
2. For low power mode, the gain is around 22.95(dBFS-dBm), and the peak-peak Gain variation is 0.72dB

**RX2 Test Case 1**

Test Environment:

- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:

- Use case:
  - LO configuration:
    - TXLO = RXLO = LO2 = 3500MHz
  - Attenuation settings:
    - Rx Gain Index = 255
  - Board ID:09

Test Method:

1. Set RXLO = TXLO = LO2 = 3500MHz
2. Set ADRF5545A to high power mode
3. Set a CW signal to -52.5dBm at Rx_ANT port
4. Sweep the CW frequency from 3400MHz to 3600MHz
Test Result:

![Graph showing RX2 with Low Power and High Power modes]

Test Result analysis:
1. For high power mode, the gain is around 40.59 (dBFS-dBm), and the peak-peak Gain variation is 1.24 dB
2. For low power mode, the gain is around 23.41 (dBFS-dBm), and the peak-peak Gain variation is 0.41 dB

RX3 Test Case 1

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
  
<table>
<thead>
<tr>
<th>USE CASE</th>
<th>TX DW</th>
<th>TX INPUT RATE</th>
<th>TX DAC RATE</th>
<th>OFX DW</th>
<th>OFX OUTPUT RATE</th>
<th>OFX ADC RATE</th>
<th>FX DW</th>
<th>FX OUTPUT RATE</th>
<th>FX ADC RATE</th>
<th>JESD NP TX/FX</th>
<th>FX/FX</th>
</tr>
</thead>
<tbody>
<tr>
<td>14_LinkShaping</td>
<td>450.000 MHz</td>
<td>491.520 MHz</td>
<td>1.966 GHz</td>
<td>450.000 MHz</td>
<td>491.520 MHz</td>
<td>4.915 GHz</td>
<td>200.000 MHz</td>
<td>245.750 MHz</td>
<td>4.915 GHz</td>
<td>12</td>
<td>12</td>
</tr>
</tbody>
</table>

- LO configuration:
  TXLO = RXLO = LO2 = 2600MHz
- Attenuation settings:
  Rx Gain Index = 255
- Board ID: 09

Test Method:
1. Set RXLO = TXLO = LO2 = 2600 MHz
2. Set ADRF5545A to high power mode
3. Set a CW signal to -52.5dBm at Rx_ANT port
4. Sweep the CW frequency from 2500MHz to 2700MHz
5. Set ADRF5549A to low Power mode and repeat step 3.

Test Result:

Test Result analysis:
1. For high power mode, the gain is around 40.99 (dBFS-dBm), and the peak-peak Gain variation is 1.94dB
2. For low power mode, the gain is around 23.72 (dBFS-dBm), and the peak-peak Gain variation is 1.19dB

RX4 Test Case 1

Test Configuration:
- Use case:

<table>
<thead>
<tr>
<th>USE CASE</th>
<th>TX DN</th>
<th>TX INPUT RATE</th>
<th>TX DAC RATE</th>
<th>ORX DN</th>
<th>ORX OUTPUT RATE</th>
<th>ORX ADC RATE</th>
<th>RX DN</th>
<th>RX OUTPUT RATE</th>
<th>RX ADC RATE</th>
<th>JESD NIP TX / RX</th>
<th>LANE RATE TX / RX / ORX</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 LOOP Sharing</td>
<td>495 MHz</td>
<td>495 MHz</td>
<td>1.566 GHz</td>
<td>495 MHz</td>
<td>495 MHz</td>
<td>4.915 GHz</td>
<td>200 MHz</td>
<td>245.76 MHz</td>
<td>4.915 GHz</td>
<td>12 / 12</td>
<td>54785.6 / 54785.6 / 54785.6</td>
</tr>
</tbody>
</table>

- LO configuration:
  - TXLO = RXLO = LO2 = 2600MHz
- Attenuation settings:
  - Rx Gain Index = 255
- Board ID: 09

Test Method:
1. Set RXLO = TXLO = LO2 = 2600MHz
2. Set ADRF5545A to high power mode
3. Set a CW signal to -52.5dBm at Rx_ANT port
4. Sweep the CW frequency from 2500MHz to 2700MHz
5. Set ADRF5549A to low Power mode and repeat step 3.

Test Result:

![Graph showing RX4 results for Low Power and High Power modes.]

Test Result analysis:
1. For high power mode, the gain is around 41.07 (dBFS-dBm), and the peak-peak Gain variation is 1.59dB
2. For low power mode, the gain is around 23.61 (dBFS-dBm), and the peak-peak Gain variation is 0.79dB

**RX NOISE FIGURE TEST (TBD)**

**RX1 Test Case 1**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
- LO configuration:
- Attenuation settings:

Test Method:

Test Result:
Test Result analysis:

**RX2 Test Case 1**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
- LO configuration:
- Attenuation settings:

Test Method:

Test Result:

Test Result analysis:

**RX3 Test Case 1**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
- LO configuration:
- Attenuation settings:

Test Method:

Test Result:

Test Result analysis:

**RX4 Test Case 1**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
- LO configuration:
- Attenuation settings:

Test Method:
Test Result:

Test Result analysis:

**ORX GAIN FLATNESS TEST (TBD)**

**ORX1 Test Case 1**

Test Environment:

- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:

- Use case:
- LO configuration:
- Attenuation settings:

Test Method:

Test Result:

Test Result analysis:

**ORX2 Test Case 1**

Test Environment:

- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:

- Use case:
- LO configuration:
- Attenuation settings:

Test Method:

Test Result:

Test Result analysis:

**ORX3 Test Case 1**

Test Environment:

- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:

- Use case:
- LO configuration:
- Attenuation settings:
Test Method:

Test Result:

Test Result analysis:

**ORX4 Test Case 1**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
- LO configuration:
- Attenuation settings:

Test Method:

Test Result:

Test Result analysis:

**ORX SPURIOUS TEST(TBD)**

**ORX1 Test Case 1**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
- LO configuration:
- Attenuation settings:

Test Method:

Test Result:

Test Result analysis:

**ORX2 Test Case 1**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC
Test Configuration:
- Use case:
- LO configuration:
- Attenuation settings:

Test Method:

Test Result:

Test Result analysis:

**ORX3 Test Case 1**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
- LO configuration:
- Attenuation settings:

Test Method:

Test Result:

Test Result analysis:

**ORX4 Test Case 1**

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
- LO configuration:
- Attenuation settings:

Test Method:

Test Result:

Test Result analysis:
RFPLL PHASE NOISE TEST (TBD)

Test Environment:
- Platform: ADS9 + Madura SC board
- GUI version: 0.0.0.861 debug build for Madura SC

Test Configuration:
- Use case:
- LO configuration:
- Attenuation settings:

Test Method:

Test Result:

Test Result analysis:
DPD VERIFICATION (TBD)