MMS6245
XMC form factor
User Manual
TABLE OF CONTENTS

INTRODUCTION .............................................................................................................. 6
FEATURES .......................................................................................................................... 8
SPECIFICATIONS ............................................................................................................. 9
REFERENCES ................................................................................................................... 10
SOFTWARE REQUIREMENTS ....................................................................................... 11
PCI device and vendor ID ............................................................................................... 11
Software considerations FPGA example design ......................................................... 11
Host Software Drivers .................................................................................................... 12
FPGA .............................................................................................................................. 13
FPGA – Introduction ...................................................................................................... 13
FPGA Design ................................................................................................................ 13
FPGA – IP modules ....................................................................................................... 13
FPGA – external circuits .............................................................................................. 14
FPGA ECM validation ................................................................................................... 15
FPGA Programming ...................................................................................................... 16
FPGA - Initialization - Load From Serial Flash Chip .................................................... 16
FPGA - JTAG Programming header ............................................................................ 17
JTAG connector, HDR1, pinout details ......................................................................... 17
FPGA Test Points .......................................................................................................... 19
FPGA Software register map ....................................................................................... 20
FPGA – LEDs ................................................................................................................. 20
FPGA – BGA Ball locations ......................................................................................... 21
XMC CONNECTOR ......................................................................................................... 22
Miscellaneous XMC signals .......................................................................................... 25
XMC I2C / IPMI support ............................................................................................. 25
XMC JTAG support ........................................................................................................ 25
XMC Misc. signals ......................................................................................................... 25
XMC Misc unused signals ............................................................................................ 25
SCSI FRONT PANEL CONNECTOR J1 ......................................................................... 26
SCSI connector mechanical details ............................................................................. 26
SCSI connector pins mapped to ECM I/O connectors ............................................... 27
SCSI connector wiring aids ......................................................................................... 28
POWER OVERVIEW ..................................................................................................... 29
THERMAL DESIGN ....................................................................................................... 30
Thermal coupling of ECMS to the ground planes ....................................................... 30
XMC INSTALLATION ................................................................................................... 31
Cautions .......................................................................................................................... 31
Warnings ....................................................................................................................... 31
MECHANICAL ............................................................................................................... 32
Installing ECMS ............................................................................................................. 32
APPENDIX A ORDERING INFORMATION .................................................................. 34
APPENDIX B RELEVANT SCHEMATICS .................................................................... 35
APPENDIX C TYPICAL APPLICATIONS ..................................................................... 40
APPENDIX D PRINTED CIRCUIT PLACEMENT ........................................................... 41
Table of Figures

Figure 1 Block Diagram ........................................................................................................................................................ 6
Figure 2 FPGA internal set of IP modules ...................................................................................................................... 13
Figure 3 - Functional overview of the FPGA .................................................................................................................... 14
Figure 4 FPGA with external circuitry ............................................................................................................................... 14
Figure 5 Original ECMs used on an Enhanced SITE ........................................................................................................... 15
Figure 6 JTAG header location shown in red ........................................................................................................................ 18
Figure 7 programming adapter, showing the orientation of the red stripe on the cable ...................................................... 18
Figure 8 programming adapter with the supplied male to male 10 pin adapter ................................................................ 19
Figure 9 TP1 offers eight FPGA test points shown in red .................................................................................................... 19
Figure 10 corresponding FPGA pins ................................................................................................................................ 20
Figure 11 FPGA LED locations on back side of board ........................................................................................................ 20
Figure 12 P15 pin orientation ............................................................................................................................................ 22
Figure 13 - 68-pin SCSI connector numbering .................................................................................................................... 26
Figure 14 - 68-pin SCSI with major dimensions ................................................................................................................ 26
Figure 15 PN6245 Power supply architecture .................................................................................................................. 29
Figure 16 white dot alignment features ............................................................................................................................. 32
Figure 17 Apply threadlocker to the screws or standoffs ..................................................................................................... 33
Figure 18 Abaco Systems P/N 6245 mounted on a P/N 8241 XMC carrier ........................................................................... 40
Figure 19 Printed Circuit Placement – side 1 .................................................................................................................. 41
Figure 20 Printed Circuit Placement – side 2 .................................................................................................................. 41

Table of Tables

Table 1 - Device/Vendor ID ............................................................................................................................................... 11
Table 2 Altera programmer header pinouts ........................................................................................................................ 17
Table - 3 FPGA LED function ............................................................................................................................................ 21
Table 4 JP1,2,3,4 to J1 SCSI connector ............................................................................................................................. 27

Life support statement

This Abaco Systems product is not designed, intended, specified or tested for life support use, any life support usage of this product is the responsibility of the purchaser of this product.

Static and handling precautions

Static precautions are mandatory in handling this equipment. Use a conductive wrist strap and handle the board in a static-free environment. Avoid touching components or connectors on the PCB, it is best to hold the PCB by the edges.

Warranty

Warranty information is found on the Abaco Systems website at www.abaco.com for product warranty or repairs please call or email Abaco Systems for an RMA number

Technical Support.

Please contact your sales representative for support with drivers and operating systems.

support@4dsp.com
Liability Limitation.

IN NO EVENT SHALL ABACO SYSTEMS, INC. BE LIABLE FOR SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING BUT NOT LIMITED TO LOSS OF PROFIT OR OPPORTUNITY. FOR ANY PRODUCT NOT MANUFACTURED BY ABACO SYSTEMS, INC., THE CUSTOMER’S SOLE AND EXCLUSIVE REMEDY IS STATED IN THE MANUFACTURER’S OR PUBLISHER’S END USER WARRANTY ACCOMPANYING THE PRODUCT. IN NO EVENT SHALL ABACO SYSTEMS, INC.’S LIABILITY EXCEED THE REPAIR, REPLACEMENT OR COST OF THE SPECIFIC PRODUCT PURCHASED FROM ABACO SYSTEMS, INC. SOME STATES MAY NOT RECOGNIZE A DISCLAIMER OR LIMITATION OF WARRANTIES AND/OR LIMITATION OF LIABILITY SO THE ABOVE DISCLAIMERS MAY NOT APPLY. CUSTOMER MAY ALSO HAVE DIFFERENT AND/OR ADDITIONAL RIGHTS AND REMEDIES THAT VARY FROM STATE TO STATE.

Part Numbers

P/N 6245, XMC four ECM carrier with 50K logic elements FPGA this is the base P/N.
A customer specific P/N is issued based on the mix of ECMs, see ordering section in this manual.

Manual Revision

Rev 2 – 07/21/2017 – Changed company name.

All product names and trademarks are the property of their respective owners.
CAUTION

(1) When developing designs for the ALTERA Cyclone FPGA, care must be exercised to insure that the FPGA logic design does not cause unsafe conditions in the system being controlled external to this board.

(2) The design should be simulated for marginalities and proper functioning.
Introduction

Figure 1 Block Diagram

Quad ECM XMC carrier

The Abaco Systems 6245 Quad ECM XMC carrier supports up to four Abaco Systems Electrical Conversion Modules (ECMs) in a VITA 42.3 XMC form-factor. Each ECM site connects 32 single-ended 3.3V signals to the FPGA. The specific ECM board installed on a site converts the FPGA signals to 16 I/O signals, for a total of 64 I/O signals across the four ECM sites. For this product, the 64 ECM I/Os are available on a front panel mounted 68-pin SCSI style connector, with four connections to signal ground also on this connector.

Four GEN 1 PCIe lanes, presented to the board via the XMC P15 connector, are wired to an Altera Cyclone V GX FPGA. The FPGA provides a hard-core PCIe interface, which bridges to internal FPGA IP via the Altera Avalon bus. The stocked board is populated with 5CGXFC4C6F23I7N, C4 density, providing an equivalent 50K Logic Element (LE) capacity. A second custom build option is available for C7 density at 149.5K LE. Generous SRAM, multipliers, logic, and PLLs are supplied by the Cyclone V FPGA, alleviating need for external memory and devices.

The FPGA is effectively the engine for the carrier, executing a resident IP core design and orchestrating various processing and I/O functions for the installed ECMs. The ECMs themselves have unique characteristics and capabilities that are supported by the FPGA and for which separate drivers and code are installed as needed. Each ECM site can be populated by a different module to allow considerable design flexibility.

On power up, an FPGA design image is loaded from a Quad serial flash memory (QSPI). This allows the PCIe interface and PCI configuration space to be initialized by the host processor. In this case, the user’s application is operational on power up. Alternatively, by using Altera’s Configuration via Protocol (CvP) technique, a host-initiated initialization and update of the FPGA core logic over PCIe may be accomplished later in the system bring up, which is useful for in-system FPGA code revision updates. The design also allows the QSPI device to be programmed from the host over the PCIe so that a subsequent power cycle will initialize the FPGA with new code.

External devices connected to the FPGA include Status LEDs, a temperature sensor, and a 93LC66 EEPROM.
JTAG programming with an Altera USB blaster, or equivalent, is supported using a male-to-male header (supplied), connecting the USB blaster cable to a female thru-the-board connector on the XMC. Thus, in-circuit QSPI device programming, direct programming of the FPGA, and support for Altera’s Signal Tap Logic Analyzer are realized.

The 68-pin front panel connector is compatible with standard fast/wide differential SCSI cables. Optional Abaco Systems transition panels (e.g., P/N 4988) may be used to break out the differential signals into more convenient individual connectors, such as DB9 interface connectors.

The design environment for this product is Altera’s Quartus Prime, with Qsys providing the interconnection between the Avalon bus IP components within the FPGA. Abaco Systems provides a sample design, including Altera Quartus FPGA design files, and “C” source code, for the customer’s specific complement of ECMs and XMC carrier card. A unique orderable Abaco Systems Part Number is assigned to this complement of carrier card, ECMs, and FPGA code programmed into the QSPI device. Often, the supplied sample code is tailored to a customer’s requirement by Abaco Systems, and no additional FPGA design effort on the customer’s part is needed.
Features

- Altera Cyclone V GX (standard 50KLE, optional 149.5KLE)
- Up to four ECMs
- 32 FPGA signals per ECM
- 16 I/O per ECM
- 64 I/Os total out 68-pin Front Panel SCSI style connector
- PCIe hard core built into FPGA
- 4x PCIe lanes w/Gen 1 (2.5 Gb/s) performance
- Easily configured using Quartus/Qsys
- Supports NIOS processor
- Configure FPGA by QSPI flash, PCIe (CvP), or JTAG
- Sample FPGA and “C” code provided
- FPGA controlled status LEDs
- Temperature sensor
- 93LC66 EEPROM
- Altera USB Blaster JTAG header
- Industrial temperature
- RoHS compliant
- Power required: +3.3V, +12/-12 as need by ECMs
- Patented
### Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature (Operating)</td>
<td>-40 to +85 degrees C</td>
</tr>
<tr>
<td>Temperature (Storage)</td>
<td>-55 to +105 degrees C</td>
</tr>
<tr>
<td>Altitude</td>
<td>Not Specified or Characterized. Typical similar equipment is at 15,000 ft.</td>
</tr>
<tr>
<td>Humidity (Operating/Storage)</td>
<td>5% to 90% non-condensing.</td>
</tr>
<tr>
<td>Vibration</td>
<td>Not specified or Characterized.</td>
</tr>
<tr>
<td>Shock</td>
<td>Not specified or Characterized.</td>
</tr>
<tr>
<td>MTBF</td>
<td>Available on request.</td>
</tr>
<tr>
<td>Weight</td>
<td>78 grams</td>
</tr>
<tr>
<td>Power</td>
<td>TBD</td>
</tr>
<tr>
<td>PCI express</td>
<td>4 lane, 2.5GHz Gen 1.</td>
</tr>
<tr>
<td>Voltages Required XMC</td>
<td>+3.3V</td>
</tr>
<tr>
<td>Size</td>
<td>74 mm x 149 mm.</td>
</tr>
<tr>
<td>Voltages Required ECM</td>
<td>+12V,-12V,+5V,+3.3V as per ECMs in use</td>
</tr>
</tbody>
</table>
**References**

These references should help the user to understand this product. This manual generally excludes information that is better presented in these references:

1. **IEEE 1386** Common Mezzanine Card Family: CMC. Provides mechanical for Mezzanine Card applications. IEEE P1386.1 (PMC) is a daughter of this specification. Also, provides P2 to CMC JN4 signal mapping for VMEbus rear-I/O connectivity. Maintained by the IEEE. [www.ieee.org](http://www.ieee.org).

2. **Vita 42** XMC high speed serial interface on PMC form factor, maintained by Vita [www.vita.com](http://www.vita.com).

3. **Vita 42.3** XMC PCI express on the P15 and P16 connectors, maintained by Vita [www.vita.com](http://www.vita.com).

4. **Vita 61** Improved XMC connector standard, maintained by Vita [www.vita.com](http://www.vita.com).

5. **PCI Express Card Electromechanical Specification, Revision 1.1** standard for PCI Express bus – maintained by PCI Special Interest Group. [www.pcisig.com](http://www.pcisig.com).

6. **Altera Cyclone V FPGA** Documentation can be found at [www.altera.com](http://www.altera.com).

7. **ECM Support Documents** email [support@4dsp.com](mailto:support@4dsp.com) to request MMS documents.
Software Requirements

Writing to and reading from the PCI express BARs and offsets to access the ECM control registers allows the user to write their own host program.

PCI device and vendor ID

When performing a PCI bus scan look for the Vendor, Device ID and Sub Device ID and each XMCECM4 configuration will have a unique Sub Device ID.

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00-0x01</td>
<td>0x1D61</td>
<td>Vendor ID</td>
<td>Identifies Abaco Systems.</td>
</tr>
<tr>
<td>0x02-0x03</td>
<td>0x1000</td>
<td>Device ID</td>
<td>Identifies Cyclone V designs</td>
</tr>
<tr>
<td>0x2C-0x2D</td>
<td>0x1D61</td>
<td>Sub Vendor ID</td>
<td>Identifies Abaco Systems.</td>
</tr>
<tr>
<td>0x2E-0x2F</td>
<td>0x1004</td>
<td>Sub Device ID</td>
<td>Identifies specific orderable P/N, will vary.</td>
</tr>
</tbody>
</table>

Table 1 - Device/Vendor ID

Software considerations FPGA example design

The FPGA example design, which comes programmed in the ECM carrier, provides enough functionality to access all the features of the populated ECMs.
Host Software Drivers

The Abaco Systems driver works for Linux or Windows, if your operating system has a PCI express driver then it should be possible to use it along with the BARs and offsets, but will require some programming effort.
FPGA

FPGA – Introduction

This section discusses the details of the FPGA design, an Altera Cyclone V, GX (standard 50KLE, optional 149.5KLE) with a PCIe hard core built into the FPGA.

The Cyclone V FPGA interfaces to external circuitry using Abaco Systems supplied IP modules.

FPGA Design

Abaco Systems supplies an example design in a compressed format with a QAR extension which can be extracted by the Altera software. The nature of the example design will not be examined in this document as it is better understood by exploring the design with the Altera software.

FPGA – IP modules

Internal to the FPGA are a mix of IP modules developed by Abaco Systems, Altera, third parties and users. Shown below is an example of a simple set of IP modules which could be used for an application. The IP modules are usually Verilog or AHDL code. The root of the design is a Verilog file. The NIOS processor provides local DMA control.

![FPGA internal set of IP modules](image)
FPGA – external circuits

Figure 3 - Functional overview of the FPGA

Figure 4 FPGA with external circuitry

External circuits list

four ECMs, with 32 data lines each.

Connects to the host processor via a 4 lane PCI express bus.

U90 generates clock inputs and is normally the primary clock input.

The PCI express clock can be used as the primary clock but must not be 25MHz.

Six LEDs,

A temperature sensor U88.

A 93LC66 eeprom, 4Kbit/512 bytes, U89.
**FPGA ECM validation**

The module detection IP in the FPGA confirms that the ECM matches the ECM IP in the FPGA. If it matches it enables the outputs, if not it leaves them in a high impedance state.

A special case is the use of an Original ECM used in an Enhanced ECM SITE.

**Figure 5 Original ECMs used on an Enhanced SITE**

Note that on Original ECMs bits 26 & 27 are outputs from the ECM only.
**FPGA Programming**

The FPGA is Configured by QSPI flash, PCIe (CvP), or the JTAG header.

The FPGA and serial flash can be programmed from the JTAG header. Alternately once the correct IP is loaded in the serial flash the FPGA and the serial flash can be reprogrammed over the PCI express bus.

Refer to the Altera documentation for detail on CvP including how to use and its limitations.

Refer to the Abaco Systems SW EPCS programming document for details on IP required to program the serial flash and functions to update the serial flash.

**FPGA - Initialization - Load From Serial Flash Chip**

Upon power up, the FPGA will be loaded with an image from the serial flash chip. This is the only way to load the FPGA from the flash chip it cannot be reloaded from flash after power up.

If a valid image is written from the serial flash chip, the FPGA will be initialized to that image.

If no valid image is found the FPGA will be un-initialized and all lines will be tri-stated, this condition is also indicated by LED D10 not illuminating.
**FPGA - JTAG Programming header**

The header for programming the Altera FPGA is connected to from the top side of the board as pictured below.

The board connector or the carrier card connector allows use of Altera Signal Tap for debugging FPGA designs. Altera Signal Tap feature is not available when programming over the PCI express bus. When using SignalTap Applications, set the Mode to JTAG.

Since the JTAG pins are not connected on the VPX connectors, the FPGA cannot be programmed from the backplane JTAG.

**JTAG connector, HDR1, pinout details**

<table>
<thead>
<tr>
<th>Function</th>
<th>Header Pin Number</th>
<th>Function</th>
<th>Header Pin Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>10</td>
<td>TDI</td>
<td>9</td>
</tr>
<tr>
<td>NC</td>
<td>8</td>
<td>NC</td>
<td>7</td>
</tr>
<tr>
<td>NC</td>
<td>6</td>
<td>TMS</td>
<td>5</td>
</tr>
<tr>
<td>+3.3V</td>
<td>4</td>
<td>TDO</td>
<td>3</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>TCK</td>
<td>1</td>
</tr>
</tbody>
</table>

*Table 2 Altera programmer header pinouts*

TDO output from the VPX card, TDI input to the VPX card. NC no connection.
Figure 6 JTAG header location shown in red

Figure 7 programming adapter, showing the orientation of the red stripe on the cable.
FPGA Test Points

There are eight test points on the back of the PCB for probing or soldering wires which can be driven or read from the FPGA.

The default signals in Abaco Systems supplied design are. TP1-1..TP1 –5 are the Altera PCIe hardcore HIP_STATUS_LTSSM state which represents what the lanes are doing. TP1-6..TP1-8 are HIP_STATUS_LANE_ACT which indicates how many lanes are active.
**FPGA Software register map**

The Altera design software generates a C language header file ending in “.top.h” which provides the addresses for the ECM control registers, data registers and BAR locations. This is useful for customer application programs.

**FPGA – LEDs**

![Figure 11 FPGA LED locations on back side of board](image)
The six LEDs connected to the FPGA provide an indication of certain conditions.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Function</th>
<th>Ref. Des.</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>LED0</td>
<td>low turns on User LED</td>
<td>D5</td>
<td>Output</td>
</tr>
<tr>
<td>LED1</td>
<td>low turns on User LED</td>
<td>D6</td>
<td>Output</td>
</tr>
<tr>
<td>LED2</td>
<td>low turns on User LED</td>
<td>D7</td>
<td>Output</td>
</tr>
<tr>
<td>LED3</td>
<td>low turns on User LED</td>
<td>D8</td>
<td>Output</td>
</tr>
<tr>
<td>Lane Active</td>
<td>LED full on 4 lanes PCI express connected</td>
<td>D9</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td>LED blinks less than 4 lanes connected</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LED off no PCI express connection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Config Done</td>
<td>LED full on FPGA has configured</td>
<td>D10</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td>LED full on FPGA has not configured</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3 FPGA LED function

Note that depending on the FPGA design any of the LEDs can serve as a PCI express status LED. The config done LED is hardwired to a dedicated FPGA output and is not programmable.

**FPGA – BGA Ball locations**

The ball locations of the FPGA signals are documented in the example FPGA design supplied by Abaco Systems. They are contained in a QSF file. From this design the EEPROM U89, ball locations are as in the four bolded lines.

- `set_location_assignment PIN_AC9 -to eecs`
- `set_location_assignment PIN_AC8 -to eeclk`
- `set_location_assignment PIN_AB10 -to eedi`
- `set_location_assignment PIN_AC10 -to eedo`
**XMC connector**

This XMC uses P15 only..

P15 allows up to 8 lanes of PCI express however P/N 6245 uses lanes 0 thru 3 and does not connect to lanes 4 thru 7.

P16 is not populated..

![Figure 12 P15 pin orientation](image-url)
P15 Male connector.

PCI express and XMC signals shown, top view looking into male pins of the connector.

<table>
<thead>
<tr>
<th></th>
<th>F</th>
<th>E</th>
<th>D</th>
<th>C</th>
<th>B</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VPWR</td>
<td>TX1-</td>
<td>TX1+</td>
<td>3.3V</td>
<td>TX0-</td>
<td>TX0+</td>
</tr>
<tr>
<td>2</td>
<td>MRSTI</td>
<td>GND</td>
<td>GND</td>
<td>TRST</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>VPWR</td>
<td>TX3-</td>
<td>TX3+</td>
<td>3.3V</td>
<td>TX2-</td>
<td>TX2+</td>
</tr>
<tr>
<td>4</td>
<td>MRSTO</td>
<td>GND</td>
<td>GND</td>
<td>TCK</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>VPWR</td>
<td>TX5-</td>
<td>TX5+</td>
<td>3.3V</td>
<td>TX4-</td>
<td>TX4+</td>
</tr>
<tr>
<td>6</td>
<td>+12V</td>
<td>GND</td>
<td>GND</td>
<td>TMS</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>VPWR</td>
<td>TX7-</td>
<td>TX7+</td>
<td>3.3V</td>
<td>TX6-</td>
<td>TX6+</td>
</tr>
<tr>
<td>8</td>
<td>-12V</td>
<td>GND</td>
<td>GND</td>
<td>TDI</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>VPWR</td>
<td>RFS</td>
<td>RFS</td>
<td>RFS</td>
<td>RFS</td>
<td>RFS</td>
</tr>
<tr>
<td>10</td>
<td>GA0</td>
<td>GND</td>
<td>GND</td>
<td>TDO</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>11</td>
<td>VPWR</td>
<td>RX1-</td>
<td>RX1+</td>
<td>MBIST</td>
<td>RX0-</td>
<td>RX0+</td>
</tr>
<tr>
<td>12</td>
<td>MPRESENT</td>
<td>GND</td>
<td>GND</td>
<td>GA1</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>13</td>
<td>VPWR</td>
<td>RX3-</td>
<td>RX3+</td>
<td>3.3V AUX</td>
<td>RX2-</td>
<td>RX2+</td>
</tr>
<tr>
<td>14</td>
<td>MSDA</td>
<td>GND</td>
<td>GND</td>
<td>GA2</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>15</td>
<td>VPWR</td>
<td>RX5-</td>
<td>RX5+</td>
<td>RPS</td>
<td>RX4-</td>
<td>RX4+</td>
</tr>
<tr>
<td>16</td>
<td>MSCL</td>
<td>GND</td>
<td>GND</td>
<td>MVMRO</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>17</td>
<td>RFU</td>
<td>RX7-</td>
<td>RX7+</td>
<td>RFU</td>
<td>RX6-</td>
<td>RX6+</td>
</tr>
<tr>
<td>18</td>
<td>RFS</td>
<td>GND</td>
<td>GND</td>
<td>RFS</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>19</td>
<td>RFS</td>
<td>ROOT0</td>
<td>WAKE</td>
<td>RFS</td>
<td>REFCLK0-</td>
<td>REFCLK0+</td>
</tr>
</tbody>
</table>

**3.3V** italic signals belong to VITA 42.0

*RFU* Reserved for use, reserved by VITA 42.0

All non-underlined signals belong to VITA 42.3

*RFS* Reserved for standard, reserved by VITA 42.3

*RX7-* etc. signals in red are not connected on 4 lane XMC cards.

*TX3-* etc. signals in blue are not connected on 1 lane XMC cards.
Pin numbering XMC Male connector

Top view looking into male pins. Notice that the large notch is near ROW 1 for orientation.
**Miscellaneous XMC signals**

**XMC I2C / IPMI support**

This XMC provides an I2C bus EEPROM for hardware definition storage. This EEPROM is readable by the host processor via IPMI commands. The IPMI commands are defined in PICMG2.9

The XMC signals used for this EEPROM include the following.

MVMRO is an active high memory protection signal set by the host processor which prevents writing to the eeprom.

Ga0, GA1 and GA2 are signals driven by the host processor which set the base address of the eeprom on the I2C bus. The MVMRO and Ga0-2 signals are XMC specific.

Note that there are no I2C devices, other than the EEPROM, accessible from the host on this XMC.

**XMC JTAG support**

There are no on board JTAG devices on this XMC accessible with the P15 JTAG signals, the JTAG data in and data out are connected together however.

**XMC Misc. signals**

MPRESENT tied to ground on this XMC signals to the host that an XMC is present.

**XMC Misc unused signals**

ROOT0 is an input to the XMC which when held low by the host allows the XMC to function as a root complex and assign base addresses to other devices on the PCI express buses.

MRSTO is an output from XMCs which resets other PCI express devices when the XMC is operating as a root complex.

WAKE is an output from XMCs which signals to the host to turn power back on and reinitiate PCI express communications.

BIST is an output from an XMC signaling to the host that the built in self-test has been performed.
**SCSI front panel connector J1**

The sixty four pin front panel connector provides a standard and versatile way to connect to system wiring.

**SCSI connector mechanical details**

The view from the front panel showing pin numbering scheme for a SCSI 68-pin “HDCI” style connector also known as a “SCSI-III” connector.

![68-pin SCSI connector numbering](image)

**Figure 13 - 68-pin SCSI connector numbering**

![68-pin SCSI with major dimensions](image)

**Figure 14 - 68-pin SCSI with major dimensions**

Refer to Tyco/AMP part number 5787394-7 SCSI III connector datasheet for more detailed dimensions.
**SCSI connector pins mapped to ECM I/O connectors**

<table>
<thead>
<tr>
<th>ECM carrier pin</th>
<th>IO</th>
<th>J1 68-pin#</th>
<th>ECM carrier pin</th>
<th>IO</th>
<th>J1 68-pin#</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal GND</td>
<td>1</td>
<td>35</td>
<td>Signal GND</td>
<td>1</td>
<td>35</td>
</tr>
<tr>
<td><strong>SITE A</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP1 pin 16</td>
<td>IO0</td>
<td>2</td>
<td>JP1 pin 18</td>
<td>IO1</td>
<td>36</td>
</tr>
<tr>
<td>JP1 pin 28</td>
<td>IO2</td>
<td>3</td>
<td>JP1 pin 30</td>
<td>IO3</td>
<td>37</td>
</tr>
<tr>
<td>JP1 pin 52</td>
<td>IO4</td>
<td>4</td>
<td>JP1 pin 54</td>
<td>IO5</td>
<td>38</td>
</tr>
<tr>
<td>JP1 pin 64</td>
<td>IO6</td>
<td>5</td>
<td>JP1 pin 66</td>
<td>IO7</td>
<td>39</td>
</tr>
<tr>
<td>JP1 pin 65</td>
<td>IO8</td>
<td>6</td>
<td>JP1 pin 63</td>
<td>IO9</td>
<td>40</td>
</tr>
<tr>
<td>JP1 pin 53</td>
<td>IO10</td>
<td>7</td>
<td></td>
<td>IO1</td>
<td>41</td>
</tr>
<tr>
<td>JP1 pin 29</td>
<td>IO12</td>
<td>8</td>
<td>JP1 pin 51</td>
<td>IO13</td>
<td>42</td>
</tr>
<tr>
<td>JP1 pin 17</td>
<td>IO14</td>
<td>9</td>
<td>JP1 pin 27</td>
<td>IO15</td>
<td>43</td>
</tr>
<tr>
<td><strong>SITE B</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP2 pin 16</td>
<td>IO0</td>
<td>10</td>
<td>JP2 pin 18</td>
<td>IO1</td>
<td>44</td>
</tr>
<tr>
<td>JP2 pin 28</td>
<td>IO2</td>
<td>11</td>
<td>JP2 pin 30</td>
<td>IO3</td>
<td>45</td>
</tr>
<tr>
<td>JP2 pin 52</td>
<td>IO4</td>
<td>12</td>
<td>JP2 pin 54</td>
<td>IO5</td>
<td>46</td>
</tr>
<tr>
<td>JP2 pin 64</td>
<td>IO6</td>
<td>13</td>
<td>JP2 pin 66</td>
<td>IO7</td>
<td>47</td>
</tr>
<tr>
<td>JP2 pin 65</td>
<td>IO8</td>
<td>14</td>
<td>JP2 pin 63</td>
<td>IO9</td>
<td>48</td>
</tr>
<tr>
<td>JP2 pin 53</td>
<td>IO10</td>
<td>15</td>
<td>JP2 pin 51</td>
<td>IO1</td>
<td>49</td>
</tr>
<tr>
<td>JP2 pin 29</td>
<td>IO12</td>
<td>16</td>
<td>JP2 pin 27</td>
<td>IO13</td>
<td>50</td>
</tr>
<tr>
<td>JP2 pin 17</td>
<td>IO14</td>
<td>17</td>
<td>JP2 pin 15</td>
<td>IO15</td>
<td>51</td>
</tr>
<tr>
<td><strong>SITE C</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP3 pin 16</td>
<td>IO0</td>
<td>18</td>
<td>JP3 pin 18</td>
<td>IO1</td>
<td>52</td>
</tr>
<tr>
<td>JP3 pin 28</td>
<td>IO2</td>
<td>19</td>
<td>JP3 pin 30</td>
<td>IO3</td>
<td>53</td>
</tr>
<tr>
<td>JP3 pin 52</td>
<td>IO4</td>
<td>20</td>
<td>JP3 pin 54</td>
<td>IO5</td>
<td>54</td>
</tr>
<tr>
<td>JP3 pin 64</td>
<td>IO6</td>
<td>21</td>
<td>JP3 pin 66</td>
<td>IO7</td>
<td>55</td>
</tr>
<tr>
<td>JP3 pin 65</td>
<td>IO8</td>
<td>22</td>
<td>JP3 pin 63</td>
<td>IO9</td>
<td>56</td>
</tr>
<tr>
<td>JP3 pin 53</td>
<td>IO10</td>
<td>23</td>
<td>JP3 pin 51</td>
<td>IO1</td>
<td>57</td>
</tr>
<tr>
<td>JP3 pin 29</td>
<td>IO12</td>
<td>24</td>
<td>JP3 pin 27</td>
<td>IO13</td>
<td>58</td>
</tr>
<tr>
<td>JP3 pin 17</td>
<td>IO14</td>
<td>25</td>
<td>JP3 pin 15</td>
<td>IO15</td>
<td>59</td>
</tr>
<tr>
<td><strong>SITE D</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP4 pin 16</td>
<td>IO0</td>
<td>26</td>
<td>JP4 pin 18</td>
<td>IO1</td>
<td>60</td>
</tr>
<tr>
<td>JP4 pin 28</td>
<td>IO2</td>
<td>27</td>
<td>JP4 pin 30</td>
<td>IO3</td>
<td>61</td>
</tr>
<tr>
<td>JP4 pin 52</td>
<td>IO4</td>
<td>28</td>
<td>JP4 pin 54</td>
<td>IO5</td>
<td>62</td>
</tr>
<tr>
<td>JP4 pin 64</td>
<td>IO6</td>
<td>29</td>
<td>JP4 pin 66</td>
<td>IO7</td>
<td>63</td>
</tr>
<tr>
<td>JP4 pin 65</td>
<td>IO8</td>
<td>30</td>
<td>JP4 pin 63</td>
<td>IO9</td>
<td>64</td>
</tr>
<tr>
<td>JP4 pin 53</td>
<td>IO10</td>
<td>31</td>
<td>JP4 pin 51</td>
<td>IO11</td>
<td>65</td>
</tr>
<tr>
<td>JP4 pin 29</td>
<td>IO12</td>
<td>32</td>
<td>JP4 pin 27</td>
<td>IO13</td>
<td>66</td>
</tr>
<tr>
<td>JP4 pin 17</td>
<td>IO14</td>
<td>33</td>
<td>JP4 pin 15</td>
<td>IO15</td>
<td>67</td>
</tr>
<tr>
<td>Signal GND</td>
<td>34</td>
<td>68</td>
<td>Signal GND</td>
<td>1</td>
<td>35</td>
</tr>
</tbody>
</table>

Table 4 JP1,2,3,4 to J1 SCSI connector
**SCSI connector wiring aids**

<table>
<thead>
<tr>
<th>P/N 5121</th>
<th>metal work allows mounting of P/N 4988 in a 6U chassis.</th>
</tr>
</thead>
<tbody>
<tr>
<td>P/N 1866</td>
<td>Allows breakout of 68 pin parallel cable signals into 16 RJ11 connectors.</td>
</tr>
<tr>
<td>P/N 1868</td>
<td>Allows breakout of 68 pin parallel cable signals into discrete terminal block connectors.</td>
</tr>
<tr>
<td>P/N 4988</td>
<td>Allows breakout of 68 pin parallel cable signals into eight 9 pin D-sub connectors.</td>
</tr>
<tr>
<td>P/N 5100</td>
<td>Allows additional breakout of signals by providing a 2nd SCSI connector.</td>
</tr>
<tr>
<td>P/N 5814</td>
<td>Allows breakout of 68 pin parallel cable signals into sixteen RJ45 jacks.</td>
</tr>
<tr>
<td>P/N 5909, 5910, 5911-5912</td>
<td>Cable, 68-pin SCSI-style connector termination with jackscrews on each end 125 ohm differential impedance</td>
</tr>
</tbody>
</table>

| PN/5909 1.5 ft. | PN/5910 3 ft. | PN/5911 6 ft. | PN/5912 10 ft. |
**Power Overview**

Abaco Systems P/N 6245 requires only +3.3V from the XMC carrier for the FPGA and local logic. This is supplied by XMC connector P15.

+12V and -12V power to the ECM sites is supplied directly from P15.

Some combination of +3.3V, +5V, +12V and -12V is also required by the ECMs. The voltages in use by each site will vary depending on the specific ECM populated.

Voltages VPWR and +3.3Vaux are supplied by the XMC carrier, but not connected on this XMC.

Ground is carried on the P15 and J15 connectors and is common throughout the board.

There is no power sequencing circuitry.

![Figure 15 PN6245 Power supply architecture](image-url)
**Thermal Design**

*Thermal coupling of ECMs to the ground planes*

The ECMs, shown in yellow, thermally couples to the top signal ground plane through the optional thermally conductive pads, the pads are shown in blue.

This thermal feature is usually not needed for systems with adequate air flow, but may be advantageous for systems with poor air flow and high power ECMs.

The ECM standoffs are electrically isolated, and are not a significant thermal dissipation path.

The thermal pads, shown as blue, are 0.875” x 0.375 inch strips of Bergquist GPVOUS-0.080-AC-0816 which are 0.080” thick. Other materials could be used as well.
XMC Installation

Place the XMC carrier on a static-safe flat surface.

Seat the front panel bezel with EMI gasket in the carrier card front panel opening.

Position the XMC rear connectors so they engage the corresponding carrier connectors. Since the XMC connectors are easy to damage, please make certain that the alignment features on the connectors are engaged properly.

Press down evenly on the XMC close to the P15/P16 connectors to fully engage the rear connectors.

Finally, use the four M2.5 machine screws, supplied in a plastic bag shipped with the XMC, to secure the XMC from the back side of the carrier board. Two fasteners for the front panel and two for the standoffs.

Cautions

Avoid ‘pinching’ the EMI gasket in the space between the XMC front panel and the carrier card front panel opening, as this may damage the EMI gasket.

Warnings

Static precautions are mandatory in handling this assembly. Use a conductive wrist strap and handle the card in a static-free environment. Avoid touching components on the XMC card or the carrier card. When transporting the board use the ESD protective bag it was shipped in or other protective wrapping.
Mechanical

Installing ECMs

Step 1. Observe that the mounting holes line up with the mounting standoffs on the carrier card. The connector is not symmetric and the mounting holes will not line up if the module is rotated 180 degrees.

Step 2. Also observe that the white dot on the carrier card and the white dot on the ECM are aligned. In the drawing the white dots are indicated by red arrows.

![Figure 16 white dot alignment features](image)

Step 3. Apply Loctite 222MS thread-locker or similar to the male threads, see red arrows. Alternately it can be applied to the standoff threads, see white arrows.

Step 4. Screw each ECM down with two 2.5mm x 0.45mm screws.
Figure 17 Apply threadlocker to the screws or standoffs.
Appendix A Ordering information

1) Choose from zero to four ECMs. A few of the P/Ns are listed below, there are many others.

RS232 ECM. P/N 3508
8 channel digital I/O ECM. P/N 3512
RS422/RS485 ECM. P/N 5041

2) Choose FPGA design, this is the example design.

3) Choose custom options, see below.

4) Get a custom orderable P/N from Abaco Systems, based on choices 1 thru. 3.

Custom part numbers derived from the base design.

Custom part numbers derived from the baseline design are possible, however order minimums, longer lead times and higher prices may apply. Call Abaco Systems for help in choosing and ordering your specific options and to get an orderable part number. Options include:

- Conformal coating, many customers order Acrylic conformal coating.
- Higher density FPGAs can be substituted.
- For other customer requirements please contact Abaco Systems.
**APPENDIX B relevant schematics**

The first schematic, **ROOT**, contains the connections between the individual detailed schematic sheets, and the 68 pin I/O connector.

The second schematic, **FPGA**, contains the FPGA connections to the PCI express bus and misc. **FPGA support circuitry**. The third schematic, **XMC P15** contains the XMC P15 connector which provides power and the PCI express bus to the board.

The fourth schematic, **ECM sites A and B**, is one of two similar schematics which show the connections between the FPGA and two ECM sites. The other schematic is not shown.

Note that because of the large number of balls and distributed nature of the FPGA control it has been broken up into multiple schematic symbols.
FPGA, PCIe interface, misc. external circuits associated with the FPGA.
XMC P15 connector, 4 lanes PCIe, power source, IMPI EEPROM.
ECM sites A and B, the FPGA, center symbol, connections to ECM sites A and B, there is 1 other virtually identical schematics to this one not shown.
Appendix C Typical applications

Figure 18 Abaco Systems P/N 6245 mounted on a P/N 8241 XMC carrier.
APPENDIX D  Printed circuit placement

Figure 19 Printed Circuit Placement – side 1

Figure 20 Printed Circuit Placement – side 2