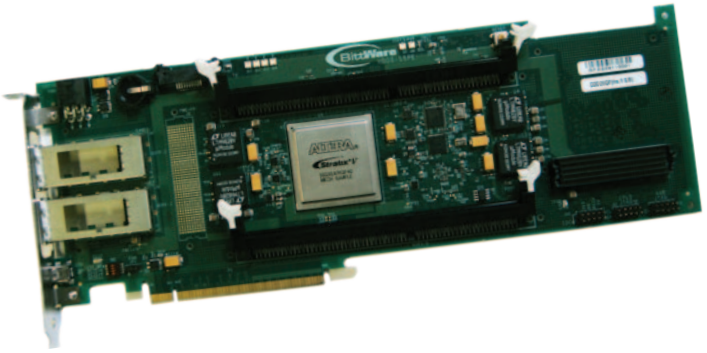
S5-PCIe

Altera Stratix® V GX/GS PCIe Board with Dual QSFP+

- High density Altera Stratix V GX/GS
- PCIe x8 interface supporting Gen1, Gen2, or Gen3
- 2 QSFP+ cages allows dual 40GigE or 8 10GigE interfaces direct to the FPGA for lowest possible latency
- Expansion site for I/O
- Up to 16 GB of DDR3 SDRAM with optional ECC
- Board Management Controller for Intelligent Platform Management
- Utility I/O includes: USB 2.0, RS-232, and JTAG



Configuration via Protocol (CvP) Supported

BittWare's S5-PCIe (S5PE) is a PCIe x8 card based on the high-bandwidth, power-efficient Altera Stratix V GX or GS FPGA. Designed for high-end applications, the Stratix V provides a high level of system integration and flexibility for I/O, routing, and processing. The S5PE is a flexible and efficient solution for high-performance network and signal processing. The board provides up to 16 GB of DDR3 SDRAM with optional error-correcting codes (ECC). It also provides two front-panel QSFP+ cages for serial I/O, which support 10G per lane direct to the FPGA for reduced latency, making it ideal for high frequency trading and networking applications. The S5PE also features a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform management.

Altera Stratix V GX/GS FPGA

The Altera Stratix V FPGA is optimized for high-performance, high-bandwidth applications with integrated transceivers (up to 14.1 Gbps) supporting backplanes and optical modules. It supports 1.6 Tbps of serial switching capability and up to 3,926 18 x 18 variable precision multipliers. The Stratix V also provides PCI Express x8 via a hard IP block and supports configuration by PCI Express using the existing PCI Express link in your application. For additional flexibility, the Stratix V supports transceiver and core reconfiguration on-the-fly while other portions of the design are running. The FPGA is supported by BittWare's FPGA Development Kit, which provides board support IP and integration.

Expansion Site

The S5PE features an expansion site, which provides 48 LVDS signals to the Stratix V along with clocks, I^2C, JTAG, and reset. The site can be used for board-to-board communication, general-purpose I/O, or additional optical links.

I/O Interfaces

The S5PE provides interfaces for high-speed serial I/O as well as debug support. Two QSFP+ cages on the front panel provide support for virtually any serial communication standard, including: Fibre Channel, 40GigE, 10GigE, SONET, CPRI, OBSAI, Serial RapidIO, and SerialLite. The eight QSFP+ SerDes channels are connected directly to the Stratix V FPGA, thus removing the latency of external PHYs.

The x8 PCIe interface provides 8 SerDes lanes to the Stratix V FPGA. USB 2.0, RS-232, and JTAG interfaces are available for debug and programming support.

Board Management Controller

BittWare's S5 boards feature an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I^2C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe, USB, or serial port. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

Development Tools

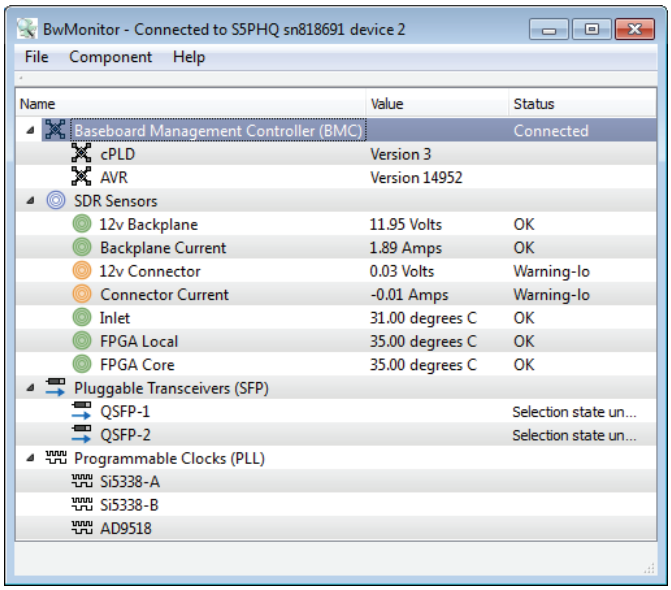
BittWorks II Toolkit

BittWare offers complete software support for the S5PE with its BittWorks II software tools. Designed to make developing and debugging applications for BittWare's boards easy and efficient, the Toolkit is a collection of libraries and applications that provides the glue between the host application and the hardware. A variety of features allow developers to take full advantage of the Stratix V FPGA capabilities on the BittWare board, including FPGA control via PCIe, Flash programming, custom ISR scripts, and convenient control of FPGA loads. The Toolkit supports 32-bit, and 64-bit Windows and Linux platforms and can connect to the board via PCIe, Ethernet, or USB, providing a common API no matter the connection method.

FPGA Development Kit

BittWare's FPGA Development Kit (FDK) provides FPGA board support IP and integration for BittWare's Altera FPGA-based COTS boards. The FDK includes FPGA components that provide preconfigured physical interfaces, infrastructure, and examples, drastically cutting development time and easily integrating into existing FPGA development environments.

Working example projects are available for each board which illustrate how to move data between the board's different interfaces. Supported interfaces include DDR3, DDR2, QDR2/+, PCIe, 10GigE, LVDS, SerDes, and Double Data Rate I/O. All example projects are available on BittWare's Developer Site.



BwMonitor in the BittWorks II Toolkit provides a view into the board management capabilities of your BittWare hardware.

BittWare Firmware and Financial Solutions Partners

BittWare offers firmware for the Stratix V FPGA on the S5 family PCIe boards, targeted specifically for high frequency trading applications. BittWare's FPGA Development Kit provides a solid base for your financial application, including the following:

- 10GigE MAC
- PCIe multi-channel DMA engines
- DDR3 SDRAM and QDRII/II+ controllers

BittWare has also partnered with several companies to offer solutions for financial acceleration:

- Algo-Logic: Market feed handler and low latency gateway libraries
- Argon Design: Design services specializing in multimedia and FPGA-based high performance trading
- Atomic Rules: Custom IP development, example UDP, precision timestamping, PCIe, networking
- Enyx: UOE, TOE, book building IP, order management IP, Market Feed Handler
- InDeLabs: Market Data Feed Handler and custom services
- Intilop: Ultra low latency TOE, UOE, and MAC
- LeWiz: Ultra low latency, multi-session TOE IP cores
- PolyBus: Infiniband link layer and transport layer
- Tamba Networks: Ultra low latency Ethernet and Interlaken cores

S5PE Specifications

Board Specifications

FPGA

- Altera® Stratix® V GX/GS FPGA
- 16 full-duplex, high-performance, multi-gigabit SerDes transceivers @ up to 14.1 GHz
- Up to 952,000 logic elements (LEs) available
- Up to 62 Mb of embedded memory
- 1.4 Gbps LVDS performance
- Up to 3,926 18x18 variable-precision multipliers
- Embedded HardCopy Blocks

Memory

- Two banks of up to 8 GByte DDR3 SDRAM x 72 with optional ECC*
- 128 MBytes of Flash memory for booting FPGA

PCIe Interface

- x8 Gen1, Gen2, Gen3 direct to FPGA

USB Header

- USB 2.0 interface for debug and programming FPGA and Flash

Debug Utility Header

- RS-232 port to Stratix V
- JTAG debug interface to Stratix V

QSFP+ Cages

- 2 QSFP+ cages on front panel connected directly to FPGA via 8 SerDes (no external PHY)
- Supports 8 10GigE or 2 40GigE

Expansion Site

- 48 LVDS
- Clocks, I²C, JTAG, and reset

Board Management Controller

- Voltage, current, temperature monitoring
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0 and JTAG access
- Voltage overrides

Size

- Full-length, standard-height PCIe slot card
- 312mm x 111.15mm
- Max. component height: 34mm

Development Tools

System Development

- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware; source code porting kit also available

FPGA Development Kit

- Physical interface components
- Board, I/O, and timing constraints
- Example Quartus projects
- Software components and drivers

FPGA Development

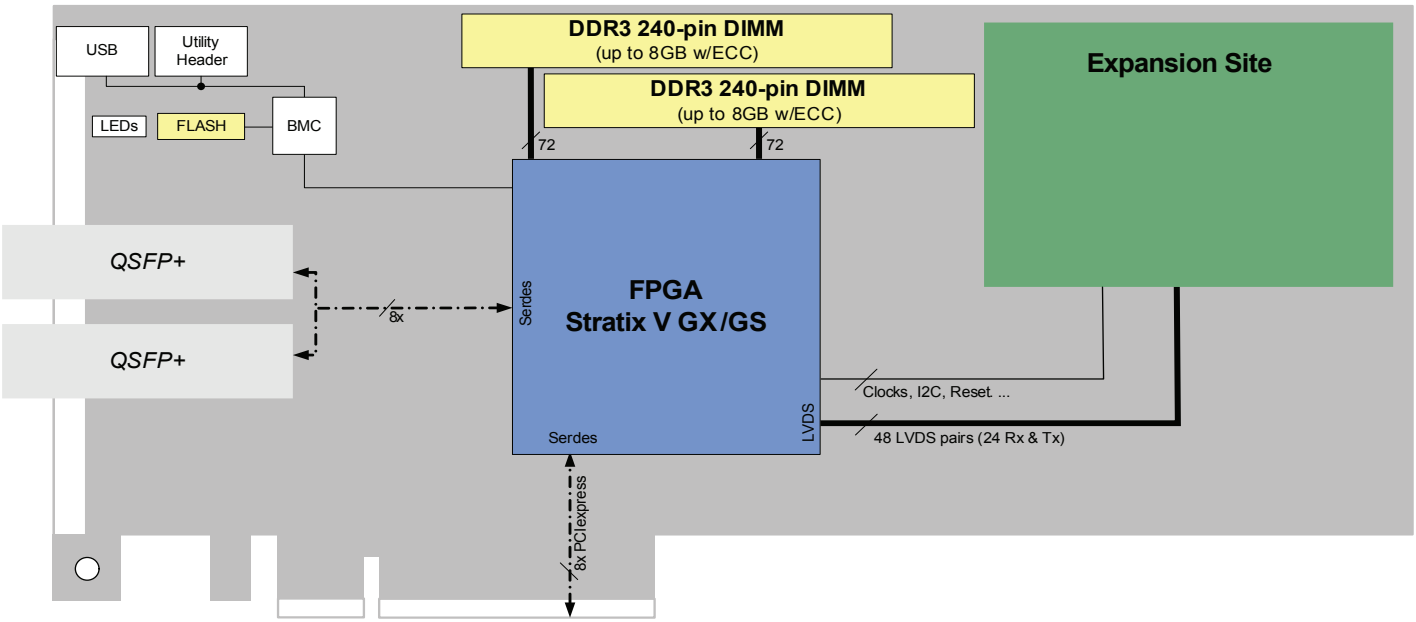
- Altera Quartus® II software

Accessory Boards

- BittWare GXBO breakout board for JTAG and RS-232 access

* DDR3 speed is 400 MHz.

Figure 2: S5PE System Block Diagram



S5PE Ordering Options

S5PE-RW-AABCCDEE-FFGG-HI-JKLMN

RW	**Ruggedization** 0U = Commercial (0C to 50 C)*
AABCC	**Altera Stratix V Family, HardIP, and Size** GXEA3 = Stratix V GXEA3 GXEA4 = Stratix V GXEA4 GXEA5 = Stratix V GXEA5 GXEA7 = Stratix V GXEA7* GSMD4 = Stratix V GSMD4 GSMD5 = Stratix V GSMD5 GSED6 = Stratix V GSED6† GSED8 = Stratix V GSED8†
D	**Altera Stratix V Transceiver Speed Grade** 1 = 14.1 Gbps transceivers † 2 = 12.5 Gbps transceivers *‡ 3 = 8.5 Gbps transceivers
EE	**Altera Stratix V Temperature Range & Speed Grade** C2 = Commercial temp. range/speed grade 2 * C3 = Commercial temp. range/speed grade 3 C4 = Commercial temp. range/speed grade 4 †
FF	**DDR3 Bank A Size**** 00 = None A9 = 2 GB (x72)* B9 = 4 GB (x72)† C9 = 8 GB (x72)
GG	**DDR3 Bank B Size**** 00 = None A9 = 2 GB (x72)* B9 = 4 GB (x72)† C9 = 8 GB (x72)
HI	**Expansion Site** 00 = Empty* 1T = 4 AN104s, typical speed (600 MHz)
J	**Misc. Configuration** 0 = Standard
K	**Front Panel Configuration** Q = QSFP x2
L	**Oscillator Configuration** 0 = 156MHz 1 = 125MHz*
M	**Heatsink** 0 = None 1 = Active* 2 = Passive
N	**Envelope Assembly** 6 = RoHS 6/6

* Default
† Contact BittWare for availability.
‡ On GXEAB devices, the Stratix V GXB speed is 11.2 Gbps.
** DDR3 speed is 400 MHz

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