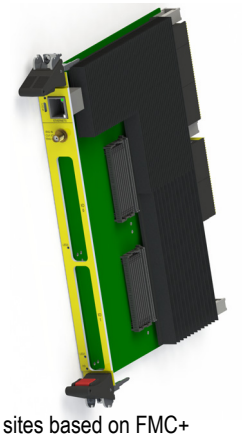
Annapolis Micro Systems, Inc.

WILDSTAR A10 3PE for OpenVPX 6U



General Features

- Three Altera Arria10 GX900, GX1150, GT1150 FPGAs
  - Up to 9,108 18x19 Multipliers per board
  - Up to 3,450,000 logic elements per board
  - GTH transceivers operating up to 15 Gbps
  - Hard 8x PCIe Gen3 endpoint for DMA and register access
  - FPGAs programmable from attached flash or Annapolis provided software API
  - 20-nm copper CMOS process
  - DDR4 DRAM ports running up to 2666 MT/s
    - Two 72-bit ports per FPGA
    - Up to 32 GB/FPGA, up to 96 GB/board
    - Up to about 44 GB/s per FPGA
    - ECC optional
  - QDR-IV SRAM ports running up to 2132 MT/s (optional for IOPEs)
    - Replaces IOPE DDR4 DRAM
    - Two 72-bit ports per IOPE
    - Up to 32 MB/FPGA, up to 64 MB/board
    - Up to about 38.4 GB/s per FPGA
    - ECC optional
- Dual Core ARM Cortex-A9 Processor (Cyclone V SoC)
  - Host Software: Linux API and Device Drivers
  - Each core runs up to 925 MHz
  - 1 GB of DDR3 DRAM
  - 8GB eMMC and 16MB NOR Boot Flash
  - 4x PCIe Gen1 connection to on-board PCIe Switch
- PLX PCI Express Gen3 Switch
  - Allows data plane "chaining" of PCIe bus between adjacent slots. No dedicated PCIe switch slot needed.
  - Allows access from a single PCIe connection to both SoC CPU and FPGA

Backplane I/O

- 24x High Speed Serial IO lanes to VPX Backplane (P1/P4) for 60 GB/s of Full Duplex Bandwidth
- Two PCIe Gen3 4x Connections to VPX Backplane (P1)
- 32 LVDS and 8 Single Ended lines to P3
- Backplane Protocol Agnostic connections support 10/40Gb Ethernet, IB capable, AnnapMicro protocol and user designed protocols
- External clock and IRIG-B Support via Backplane
- Radial Backplane Clock Support for OpenVPX backplane signals AUXCLK and REFCLK
  - Allows points-to-point, very high quality backplane connections to payload cards
  - Allows 10MHz clock and trigger from backplane to synchronize and clock compatible ADC/DAC mezzanine cards without front panel connections needed
  - Allows 1000s of analog channels across many backplanes/chassis to be synchronized via backplane

Front Panel I/O

- Two Wild FMC+ (WFMC+) next generation IO sites based on FMC+ specification
  - Accepts standard FMC and FMC+ cards (complies to FMC+ specification)
  - Allows larger form factor Annapolis cards for higher IO density
  - Supports additional LVDS IO for higher density ADC and DAC solutions
  - Supports stacking (2 IO cards per site) when at least one card is WFMC+
  - Up to 32 High Speed Serial and 100 LVDS connections to FPGA
  - Support for double wide cards
- Simultaneous Optics and ADC/DAC use with two slots
- Protocol Agnostic HSS connections support 10/40/100 Gb Ethernet, IB capable, AnnapMicro protocol and user designed protocols
- SMA for clock in, clock out or IRIG-B in supporting multiple IO standards and terminations.
- Micro USB connector for CPU serial port (uses USB to UART bridge chip)

Application Development

- Open Project Builder Application Design Suite
  - Full Board Support Package for Fast and Easy Application Development
  - Computational, DSP and Data Flow Control Cores (FFTs, FIR, Math, etc)
  - Develop in GUI environment or create VHDL and use HDL environment
  - Built-in Debugger for Hardware in the loop Debugging
  - Communication Cores Included (10/40Gb Ethernet and AnnapMicro Protocol cores)
  - VHDL Model includes Source Code for Hardware Interfaces
  - Supports High-Level Synthesis (HLS) Design Flow
- JTAG Access through RTM, Ethernet, or PCIe
- Board control and status monitoring can be local (stand alone), remote (via Ethernet or PCIe) or hybrid (both local and remote)

System Management

- System Management using Intelligent Platform Management Interface (IPMI)
- Diagnostic monitoring and configuration
- Current, Voltage and Temperature Monitoring Sensors
- Hot Swappable (exclusive to WILDSTAR OpenVPX EcoSystem)

Mechanical and Environmental

- 6U OpenVPX (VITA 65) Compliant, 1" VITA 48.1 spacing
- Supports OpenVPX payload profile: MOD6-PAY-4F1Q2U2T-12.2.1-n
- Integrated Heat Sink and Board Stiffener
- Available in Extended Temperature Grades
- Air or Conduction Cooled path
- RTM available for additional I/O

OpenCL

Fully Integrated and Qualified with WILDSTAR OpenVPX EcoSystem
Reduce Risk, Save Time and Effort

OpenVPX EcoSystem

190 Admiral Cochrane Drive, Suite 130
Annapolis, MD 21401-7386
Phone: (410) 841-2514
www.annapmicro.com

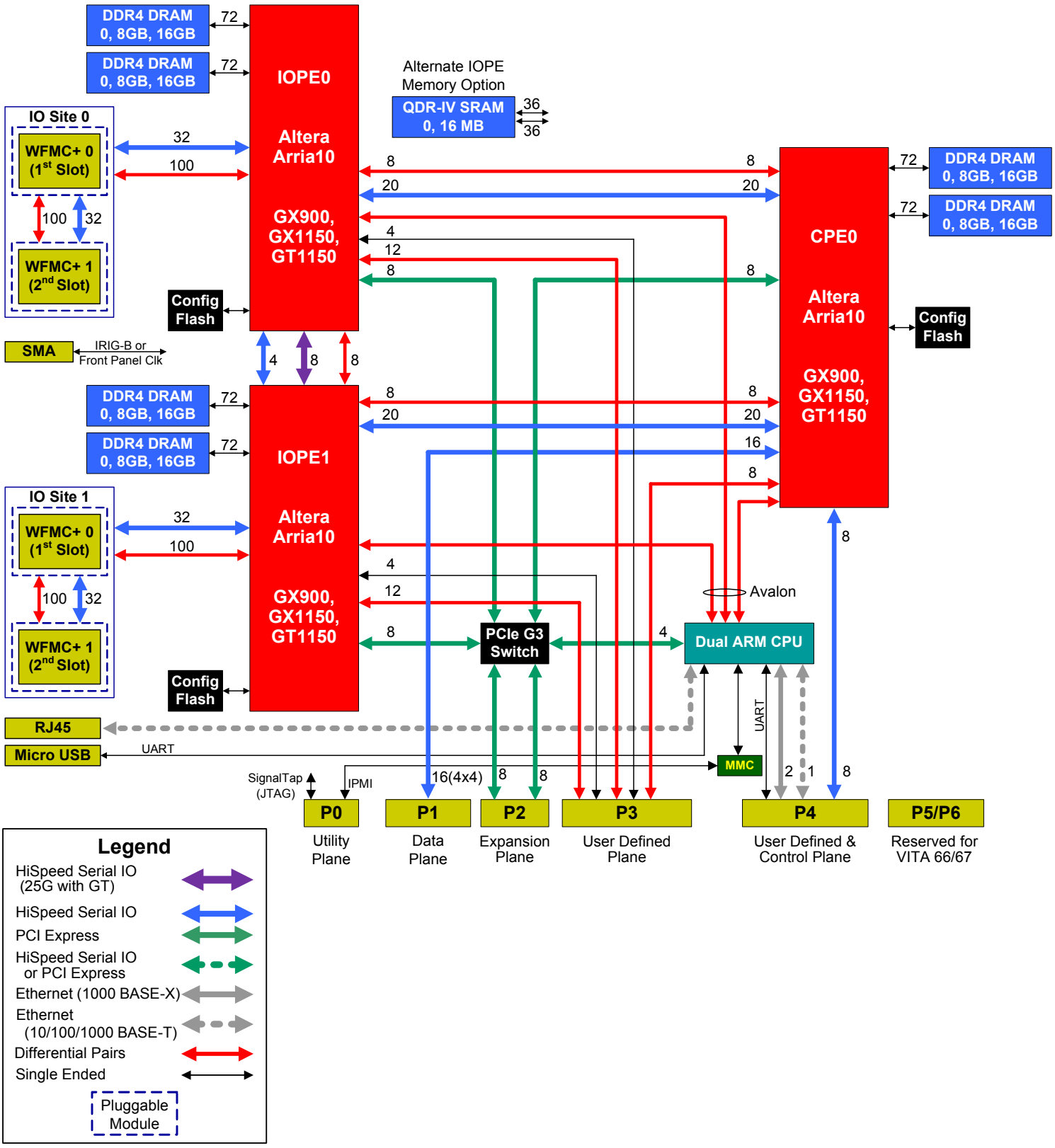
Made in the USA

OpenVPX™

Arria®10

Data Sheet
Document Number
15460-0000, Revision 1.4

System Architecture



190 Admiral Cochrane Drive, Suite 130
Annapolis, MD 21401-7386
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