

eUSB3.0 Development Board

Reference Manual



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Introduction

This manual provides component details of the eUSB 3.0 development board.

Table below shows the revision history of the manual.

Version	Date	Description
1.0	August 2014	• First Publication

How to Find Information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Use Ctrl + F to open the Find dialog box. Use Shift + Ctrl + N to open to the Go To Page dialog box.
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Typographic Conventions

This reference manual uses the typographic conventions as shown below:

Visual Cue	Meaning
Bold Type with Initial Capital letters	All headings and Sub headings Titles in a document are displayed in bold type with initial capital letters; Example: Board Components, Featured Device.
Bold Type with Italic Letters	All Definitions, Figure and Table Headings are displayed in Italics. Examples: <i>Figure 1-1. eUSB 3.0 Development Board Angle View, Table 1-1. eUSB 3.0 Board Development Component and Interfaces</i>
1., 2.	Numbered steps are used in a list of items, when the sequence of items is important. such as steps listed in procedure.
•	Bullets are used in a list of items when the sequence of items is not important.
	The hand points to special information that requires special attention
 CAUTION	The caution sign indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
 WARNING	The warning sign indicates information that should be read prior to starting or continuing the procedure or processes.
	The feet direct you to more information on a particular topic.

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General Description

eUSB3.0 Development board provides hardware and software support for implementation of USB3.0 Device functionality with Altera Cyclone V GT FPGA without the need for a USB3.0 PHY Chip. SuperSpeed link implementation using 5Gbps speed transceiver I/O of Cyclone V GT FPGA replaces the use of any external PHY chip for USB 3.0 communication. Also the board is having memory components like DDR2 SDRAM, SDRAM, CFI Flash, EPCS and SD Card for external storage.

The board functionality can be expanded through an Altera High Speed Custom Mezzanine Card (HSMC). This interface is specifically design for SLS Camera interface module. This will give a better way to interface the camera module to the board for image application. For more information about Image Acquisition Application, refer to [Image Acquisition Application](#).

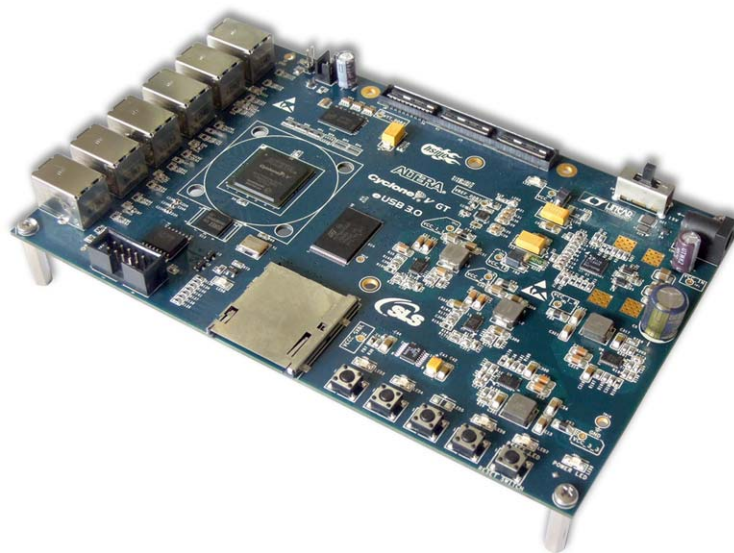
Hence, the board is a perfect embedded solution on which any eUSB 3.0 development can be carried out. [Figure 1-1](#). shows the eUSB 3.0 development board angle view.

Features

The main features of the eUSB 3.0 development board are:

- Cyclone V GT FPGA 5CGTFD5C5U19A7 in 484-pin UBGA package
- 64 Mb EEPROM configuration device configurable via JTAG interface
- Multiple clock sources: 2 x 48 MHz, 2 x 125 MHz
- Six USB 3.0 Connector directly connected to Altera Transceiver
- Huge memory sub-system comprising of CFI Flash, DDR2 SDRAM and SDRAM
- Push-button switches and LEDs
- Supports for JTAG programming mode
- Custom HSMC interface
- SD card interface

Figure 1-1. eUSB 3.0 Development Board Angle View



Component Blocks

The board features the following major component blocks:

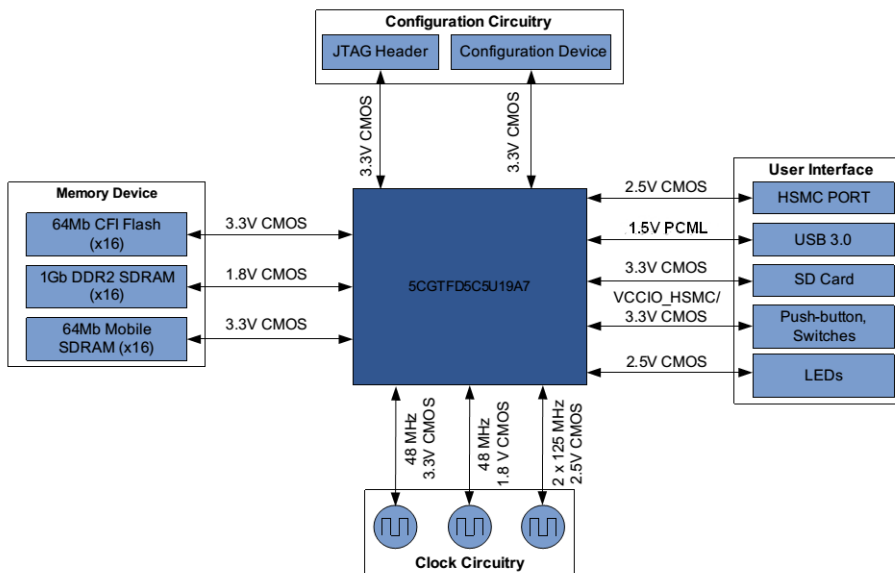
- Cyclone V GT FPGA 5CGTFD5C5U19A7 in the 484-pin UBGA Package
 - 77K LEs
 - 5Mb size on-chip memory
 - 6PLLs
 - 300 18x18 multipliers
- FPGA Configuration
 - JTAG Header for FPGA Programming
 - 64 Mbit Serial Configuration (EPCS64) EEPROM
- On-board Clocking Circuitry
 - 2 x 48MHz oscillator
 - 2 x 125MHz oscillator

- Memory Devices
 - 64 (4M x 16) Mb CFI Flash with 16-bit data bus
 - 1 (64M x 16) Gb DDR2 with 16-bit data bus
 - 256 (16M x 16) Mb SDRAM with 16-bit data bus
- USB 3.0 Interface
 - 6.144 Gbps Altera FPGA Transceiver
- Peripheral Expansion & GPIO
 - Custom High Speed Mezzanine Card (HSMC) interface
- LEDs
 - Three user LEDs
 - Power LED
 - Reset LED
- Switches
 - Four user push-button switches
 - Reset push-button switch
 - Power ON/OFF switch
- Power
 - 15VDC - 20VDC @ 3A
- Mechanical
 - PCB size is 7.0" X 4.5"

Block Diagram

Figure 1-2. below shows functional block diagram of the eUSB 3.0 development board.

Figure 1-2. eUSB 3.0 Development Board Functional Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:



Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Next Section explains overview of all the eUSB 3.0 development board components.

2. Board Component

This chapter provides operational and connectivity details for the board's major components and interfaces. [Figure 2-1.](#) shows the available components on the eUSB 3.0 development board.

Figure 2-1. eUSB 3.0 Development Board - Components

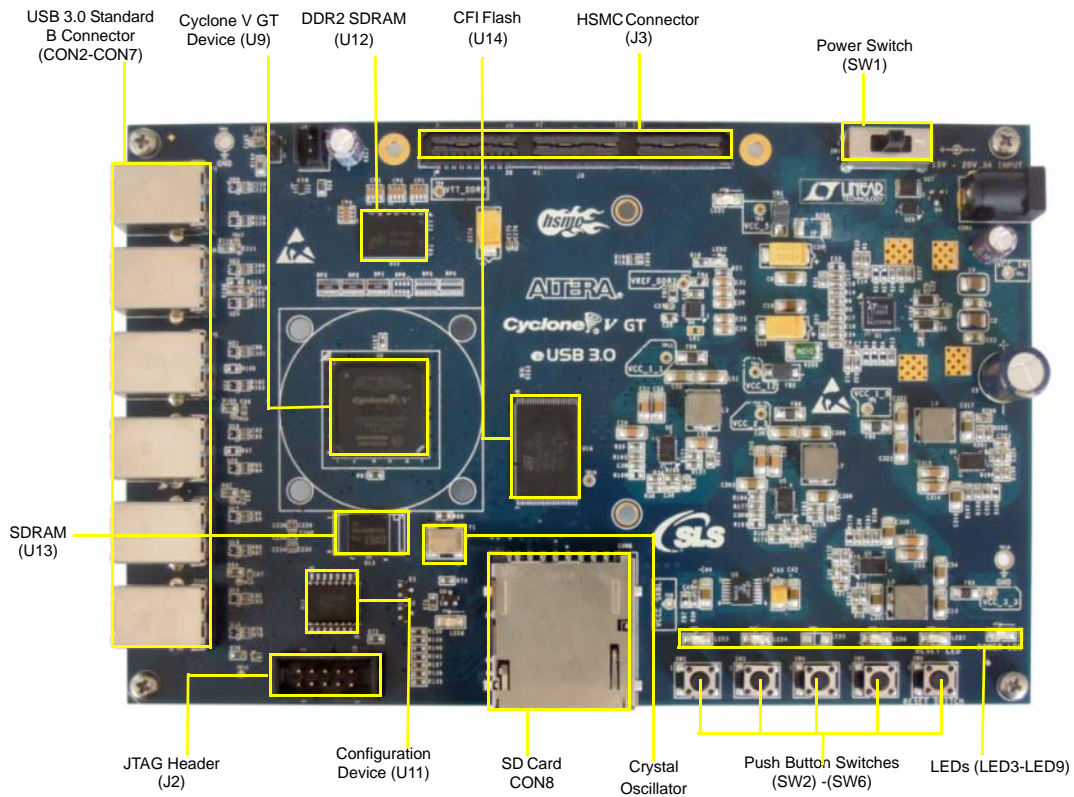


Table 2-1 describes the components and lists their corresponding board references.

<i>Table 2-1. eUSB 3.0 Development Board Components & Interfaces</i>			
Board Reference	Name	Description	Page
Featured Device			
U9	Cyclone V GT FPGA	Altera, 5CGTFD5C5U19A7, Cyclone V GT FPGA	7
Configuration Circuitry			
J2	JTAG Header	JTAG Header used for FPGA programming	9
U11	Configuration Device	Altera, EPCS64 serial configuration device	9
Memory Device			
U12	DDR2 SDRAM	Micron, MT47H64M16HR-25, 64 Meg x 16 (8 Meg x 16 x 8 banks) (1Gbits) DDR2 SDRAM	10
U13	SDRAM	Eorex, EM48AM1684VBE-TFPGA54, 4M x16 X4 banks (256 Mb) SDRAM	12
U14	CFI Flash	Numonyx, M29W640GB70NA6E, 64-Mbit (8 Mbit x8 or 4 Mbit x16) CFI Flash	14
General User Input and Output			
LED3, LED4, LED6	LEDs	Three user-defined LEDs	16
SW6	Reset Switch	User-defined reset push-button switch	18
SW2, SW3, SW4, SW5	Push-button Switches	Four user-defined push-button switches	18
CON2, CON3, CON4, CON5, CON6, CON7	USB 3.0 Standard B-Type Connectors	Six B-Type USB 3.0 connectors	18
CON8	SD Card Connector	SD card connector	22
Expansion Interface			
J3	HSMC Connector	Connector for interfacing HSMC card	23
Power Supply			
SW1	Power Switch	Power ON-OFF Switch	27
Clock Circularity			

Table 2-1. eUSB 3.0 Development Board Components & Interfaces

Board Reference	Name	Description	Page
Y1, Y2	Crystal Oscillator	48 MHz crystal for FPGA	27
Y3, Y4	Crystal Oscillator	125 MHz crystal for FPGA	27

Featured Device Cyclone V GT Device (U9)

The eUSB 3.0 development board features the Cyclone V GT 5CGTFD5C5U19A7 device (U9) in 484-pin Ultra FineLine BGA (UBGA) package.



For more information about Cyclone V GT device, refer to [Cyclone V Device Hand Book](#).

[Table 2-2](#) lists Cyclone V GT device 5CGTFD5C5U19A7N features.

Table 2-2. Cyclone V GT 5CGTFD5C5U19A7N Device Features

Architectural Feature	Value
Logic Elements	77000
RAM	5001216
User I/Os	336
PLLs and Banks	6 PLLs and 8 banks
Embedded 18 × 18 Multipliers	300

[Table 2-3](#) lists the Cyclone V GT 5CGTFD5C5U19A7N device pin I/Os.

Table 2-3. Cyclone V GT Device I/Os Pin Count

Function	IO Type	IO Count
DDR2 SDRAM	VCC_1_8	44
SDRAM	VCC_3_3	38
CFI Flash	VCC_3_3	41
USB 3.0	1.5V PCML	30
SD Card Connector	VCC_3_3	8
Push-button (User IO + Reset)	VCC_3_3	5

Table 2-3. Cyclone V GT Device I/Os Pin Count

Function	IO Type	IO Count
User LEDs	VCC_2_5 VCC_3_3 VCC_1_8	3
HSMC Connector	VCC_3_3	41
GPIO Header	VCC_3_3	4
Clock	VCC_3_3	6
Configuration	VCC_3_3	4
Total I/Os Used	-	224
Unused I/Os	-	40
VCC & GND	-	182
VREF	-	7
Unused Pins	-	31
Total 5CGTFD5 Pins		484

Configuration Circuitry

Configuring the Cyclone V GT FPGA

A serial EEPROM chip (EPCS64) that stores configuration data for the Cyclone V GT FPGA in eUSB 3.0 development board. This configuration data loads automatically from the EEPROM chip into the FPGA each time power is applied to the board.

Using the Quartus II software, it is possible to reprogram the FPGA at any time and it is also possible to change the nonvolatile data stored in the serial EEPROM chip.

JTAG Programming

In this method of programming, named after the IEEE standards Joint Test Action Group. A SRAM Object File (.sof) file can be used to configure FPGA directly which will be volatile, so configuration will be retained as long as power is applied to the board. A JTAG Indirect Configuration File (.jic) can be used to configure EPCS64 so that each time board powers up it loads FPGA configuration from serial EEPROM-EPCS64. Both SRAM Object file and JTAG Indirect Configuration file uses JTAG programming method.

JTAG Header (J2)

JTAG header, J2 is used to configure FPGA device on the eUSB 3.0 development board.

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

[Table 2-4](#) shows the JTAG header signal name, type and board reference pin.

<i>Table 2-4. JTAG Header (J2) Pinout</i>				
Board Reference	Signal Name	Direction (FPGA)	Type	FPGA (U9) Pin
J2 . 1	JTAG_TCK	Input	VCC_3_3	V5
J2 . 3	JTAG_TDO	Output	VCC_3_3	V3
J2 . 5	JTAG_TMS	Input	VCC_3_3	R4
J2 . 9	JTAG_TDI	Input	VCC_3_3	P5

Serial Configuration Device - EPCS64 (U11)

U11 is a Serial Configuration Device (EPCS64) for the Cyclone V GT FPGA on eUSB 3.0 development board. Serial Configuration Devices are Flash memory devices with a serial interface that can store configuration data for a Cyclone V GT device and reload the data into the device upon power up or re-configuration.

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

Table 2-5 shows the serial configuration device signal name, type and board reference pin.

Device Reference	Signal Name	Direction (FPGA)	Type	U11 Pin	FPGA (U9) Pin
DATA	AS_DATA1	Bi-directional	VCC_3_3	8	W5
NCS	AS_NCS0	Output	VCC_3_3	7	AB6
ASDI	AS_ASDO	Output	VCC_3_3	15	AB4
DCLK	AS_DCLK	Input	VCC_3_3	16	M5

Memory Device

This section describes the board's memory interface support, signal names, types, and connectivity relative to the Cyclone V GT device. The board has the following memories interfaces:

- DDR2 SDRAM
- SDRAM
- CFI Flash

DDR2 SDRAM (U12)

There is a 1Gb of DDR2 SDRAM MT47H64M16HR-25:H TR- WBGA84 pin WBGA package, device provided. Device interface has 16-bit data bus. DDR2 device is pinned out to FPGA bank 7A with 1.8V I/O voltage level.

DDR2 SDRAM organized as 8,388,608 words x 8banks x 16 bits. This device achieves high speed transfer rates up to 1066/Mb/sec/pin (DDR2-1066) for general application. All of the control and address inputs are synchronized with a pair of differential clocks. Inputs are latched at the cross point of differential clocks (CLK rising and CLK_n falling). All I/Os are synchronized with a single ended DQS or differential DQS-DQS pair in a source synchronous fashion.

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

Table 2-6 shows U12 DDR2 SDRAM signal name, type and board reference pin respectively.

Device Reference	Signal Name	Direction (FPGA)	Type	U12 Pin	FPGA (U9) Pin
CLK_N	DDR2_CK_N	Output	VCC_1_8	K8	A14
CLK_P	DDR2_CK_P	Output	VCC_1_8	J8	A15
LDM	DDR2_SD_LDM	Output	VCC_1_8	F3	C18
UDM	DDR2_SD_UDM	Output	VCC_1_8	B3	C21
LDQS	DDR2_SD_LDQS	Output	VCC_1_8	F7	G12
UDQS	DDR2_SD_UDQS	Output	VCC_1_8	B7	G15
RAS_N	DDR2_SD_RAS_N	Output	VCC_1_8	K7	A19
WE_N	DDR2_SD_WE_N	Output	VCC_1_8	K3	B22
CAS_N	DDR2_SD_CAS_N	Output	VCC_1_8	L7	E16
CS_N	DDR2_SD_CS_N	Output	VCC_1_8	L8	G14
ODT	DDR2_SD_ODT	Output	VCC_1_8	K9	B17
A0	DDR2_SD_ADDR0	Output	VCC_1_8	M8	D13
A1	DDR2_SD_ADDR1	Output	VCC_1_8	M3	D14
A2	DDR2_SD_ADDR2	Output	VCC_1_8	M7	C14
A3	DDR2_SD_ADDR3	Output	VCC_1_8	N2	C13
A4	DDR2_SD_ADDR4	Output	VCC_1_8	N8	H12
A5	DDR2_SD_ADDR5	Output	VCC_1_8	N3	A13
CKE	DDR2_SD_CLKEN	-	VCC_1_8	K2	-
A6	DDR2_SD_ADDR6	Output	VCC_1_8	N7	B13
A7	DDR2_SD_ADDR7	Output	VCC_1_8	P2	F12
A8	DDR2_SD_ADDR8	Output	VCC_1_8	P8	H9
A9	DDR2_SD_ADDR9	Output	VCC_1_8	P3	E12
A10	DDR2_SD_ADDR10	Output	VCC_1_8	M2	E14

Table 2-6. DDR2 SDRAM (U12) Pinout

Device Reference	Signal Name	Direction (FPGA)	Type	U12 Pin	FPGA (U9) Pin
A11	DDR2_SD_ADDR11	Output	VCC_1_8	P7	B12
A12	DDR2_SD_ADDR12	Output	VCC_1_8	R2	G8
D0	DDR2_SD_DATA0	Bidirectional	VCC_1_8	G8	C16
D1	DDR2_SD_DATA1	Bidirectional	VCC_1_8	G2	A17
D2	DDR2_SD_DATA2	Bidirectional	VCC_1_8	H7	B15
D3	DDR2_SD_DATA3	Bidirectional	VCC_1_8	H3	C15
D4	DDR2_SD_DATA4	Bidirectional	VCC_1_8	H1	B16
D5	DDR2_SD_DATA5	Bidirectional	VCC_1_8	H9	F15
D6	DDR2_SD_DATA6	Bidirectional	VCC_1_8	F1	C19
D7	DDR2_SD_DATA7	Bidirectional	VCC_1_8	F9	B18
D8	DDR2_SD_DATA8	Bidirectional	VCC_1_8	C8	B20
D9	DDR2_SD_DATA9	Bidirectional	VCC_1_8	C2	C20
D10	DDR2_SD_DATA10	Bidirectional	VCC_1_8	D7	E17
D11	DDR2_SD_DATA11	Bidirectional	VCC_1_8	D3	D18
D12	DDR2_SD_DATA12	Bidirectional	VCC_1_8	D1	A20
D13	DDR2_SD_DATA13	Bidirectional	VCC_1_8	D9	D17
D14	DDR2_SD_DATA14	Bidirectional	VCC_1_8	B1	A22
D15	DDR2_SD_DATA15	Bidirectional	VCC_1_8	B9	B21
BA0	DDR2_SD_BA0	Output	VCC_1_8	L2	H16
BA1	DDR2_SD_BA1	Output	VCC_1_8	L3	G16
BA2	DDR2_SD_BA2	Output	VCC_1_8	L1	A18

SDRAM (U13)

The EM48AM1684VBE is Synchronous Dynamic Random Access Memory (SDRAM) organized as 4Meg words x 4 banks by 16 bits. All inputs and outputs are synchronized with the positive edge of the clock. The 256Mb

SDRAM uses synchronized pipelined architecture to achieve high speed data transfer rates and is designed to operate at 3.3V low power memory system. It also provides auto refresh with power saving / down mode. All inputs and outputs voltage levels are compatible with LVTTTL. Available packages: FBGA 54B 8mm x 8mm. SDRAM device is pinned out to FPGA bank 3A and 3B with 3.3V I/O voltage level.

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

Table 2-7 shows the SDRAM signal name, type and board reference pin.

Device Reference	Signal Name	Direction (FPGA)	Type	U13 Pin	FPGA (U9) Pin
CLK	SDR_CLK	Output	VCC_3_3	F2	AB11
CAS_N	SDR_CAS_N	Output	VCC_3_3	F7	T8
CS_N	SDR_CS_N	Output	VCC_3_3	G9	AB7
BA0	SDR_BA0	Output	VCC_3_3	G7	Y7
BA1	SDR_BA1	Output	VCC_3_3	G8	AA7
LDQM	sdr_be_n0	Output	VCC_3_3	E8	AA8
RAS_N	SDR_RAS_N	Output	VCC_3_3	F8	U8
UDQM	sdr_be_n1	Output	VCC_3_3	F1	N8
WE_N	SDR_RD_WR_N	Output	VCC_3_3	F9	V8
A0	SDR_ADDR0	Output	VCC_3_3	H7	M7
A1	SDR_ADDR1	Output	VCC_3_3	H8	P7
A2	SDR_ADDR2	Output	VCC_3_3	J8	P6
A3	SDR_ADDR3	Output	VCC_3_3	J7	N6
A4	SDR_ADDR4	Output	VCC_3_3	J3	M6
A5	SDR_ADDR5	Output	VCC_3_3	J2	R5
A6	SDR_ADDR6	Output	VCC_3_3	H3	L7
A7	SDR_ADDR7	Output	VCC_3_3	H2	U6
A8	SDR_ADDR8	Output	VCC_3_3	H1	R6
A9	SDR_ADDR9	Output	VCC_3_3	G3	W7

Table 2-7. SDRAM (U13) Pinout

Device Reference	Signal Name	Direction (FPGA)	Type	U13 Pin	FPGA (U9) Pin
A10	SDR_ADDR10	Output	VCC_3_3	H9	R7
A11	SDR_ADDR11	Output	VCC_3_3	G2	U7
A12	SDR_ADDR12	Output	VCC_3_3	G1	T7
D0	SDR_DATA0	Bidirectional	VCC_3_3	A8	P12
D1	SDR_DATA1	Bidirectional	VCC_3_3	B9	W11
D2	SDR_DATA2	Bidirectional	VCC_3_3	B8	U11
D3	SDR_DATA3	Bidirectional	VCC_3_3	C9	Y10
D4	SDR_DATA4	Bidirectional	VCC_3_3	C8	U10
D5	SDR_DATA5	Bidirectional	VCC_3_3	D9	Y9
D6	SDR_DATA6	Bidirectional	VCC_3_3	D8	V9
D7	SDR_DATA7	Bidirectional	VCC_3_3	E9	AB8
D8	SDR_DATA8	Bidirectional	VCC_3_3	E1	W8
D9	SDR_DATA9	Bidirectional	VCC_3_3	D2	T9
D10	SDR_DATA10	Bidirectional	VCC_3_3	D1	N9
D11	SDR_DATA11	Bidirectional	VCC_3_3	C2	N10
D12	SDR_DATA12	Bidirectional	VCC_3_3	C1	AA9
D13	SDR_DATA13	Bidirectional	VCC_3_3	B2	R11
D14	SDR_DATA14	Bidirectional	VCC_3_3	B1	AA10
D15	SDR_DATA15	Bidirectional	VCC_3_3	A2	Y11

CFI Flash (U14)

CFI device M29W640GB70NA6E, 48 pin TSSOP package, providing 64Mb of memory. Device interface has 16-bit data bus. This device is pinned out to FPGA bank 4A with 3.3V I/O voltage level.

The M29W640GH and M29W640GL memory array is organized into 128 uniform blocks of 64 Kbytes each (or 32 Kwords each). The M29W640GT

and M29W640GB feature asymmetric block architecture. The devices have an array of 135 blocks, divided into 8 parameter blocks of 8 Kbytes each (or 4K words each) and 127 main blocks of 64 Kbytes each (or 32K words each).

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

Table 2-8 shows the CFI Flash signal name, type and board reference pin.

Device Reference	Signal Name	Direction (FPGA)	Type	U14 Pin	FPGA (U9) Pin
A0	CFI_FL_A0	Output	VCC_3_3	25	AA17
A1	CFI_FL_A1	Output	VCC_3_3	24	AB17
A2	CFI_FL_A2	Output	VCC_3_3	23	U16
A3	CFI_FL_A3	Output	VCC_3_3	22	W16
A4	CFI_FL_A4	Output	VCC_3_3	21	Y16
A5	CFI_FL_A5	Output	VCC_3_3	20	AB16
A6	CFI_FL_A6	Output	VCC_3_3	19	U15
A7	CFI_FL_A7	Output	VCC_3_3	18	V15
A8	CFI_FL_A8	Output	VCC_3_3	8	T12
A9	CFI_FL_A9	Output	VCC_3_3	7	AB13
A10	CFI_FL_A10	Output	VCC_3_3	6	AA13
A11	CFI_FL_A11	Output	VCC_3_3	5	W13
A12	CFI_FL_A12	Output	VCC_3_3	4	V13
A13	CFI_FL_A13	Output	VCC_3_3	3	T13
A14	CFI_FL_A14	Output	VCC_3_3	2	Y14
A15	CFI_FL_A15	Output	VCC_3_3	1	W14
A16	CFI_FL_A16	Output	VCC_3_3	48	W22
A17	CFI_FL_A17	Output	VCC_3_3	17	Y15
A18	CFI_FL_A18	Output	VCC_3_3	16	AA15
A19	CFI_FL_A19	Output	VCC_3_3	9	U12
A20	CFI_FL_A20	Output	VCC_3_3	10	W12

Table 2-8. CFI Flash (U14) Pinout

Device Reference	Signal Name	Direction (FPGA)	Type	U14 Pin	FPGA (U9) Pin
A21	CFI_FL_A21	Output	VCC_3_3	13	AB15
CE_N	CFI_FL_CE_N	Output	VCC_3_3	26	Y17
OE_N	CFI_FL_OE_N	Output	VCC_3_3	28	W17
WE_N	CFI_FL_WE_N	Output	VCC_3_3	11	Y12
DQ0	CFI_FL_DQ0	Bidirectional	VCC_3_3	29	U17
DQ1	CFI_FL_DQ1	Bidirectional	VCC_3_3	31	AA18
DQ2	CFI_FL_DQ2	Bidirectional	VCC_3_3	33	V18
DQ3	CFI_FL_DQ3	Bidirectional	VCC_3_3	35	Y19
DQ4	CFI_FL_DQ4	Bidirectional	VCC_3_3	38	AA20
DQ5	CFI_FL_DQ5	Bidirectional	VCC_3_3	40	AB21
DQ6	CFI_FL_DQ6	Bidirectional	VCC_3_3	42	W21
DQ7	CFI_FL_DQ7	Bidirectional	VCC_3_3	44	AA22
DQ8	CFI_FL_DQ8	Bidirectional	VCC_3_3	30	AB18
DQ9	CFI_FL_DQ9	Bidirectional	VCC_3_3	32	W18
DQ10	CFI_FL_DQ10	Bidirectional	VCC_3_3	34	AA19
DQ11	CFI_FL_DQ11	Bidirectional	VCC_3_3	36	AB20
DQ12	CFI_FL_DQ12	Bidirectional	VCC_3_3	39	Y20
DQ13	CFI_FL_DQ13	Bidirectional	VCC_3_3	41	Y21
DQ14	CFI_FL_DQ14	Bidirectional	VCC_3_3	43	AB22
DQ15	CFI_FL_DQ15	Bidirectional	VCC_3_3	45	Y22

General User Input and Output

LEDs

The board includes four board specific LED and three user programmable LEDs. [Table 2-9](#) lists LEDs and its description.

User LEDs (LED3, LED4, LED6)

Status and debugging signals are driven to the user LEDs from FPGA designs loaded into the Cyclone V GT device.

Board Specific LEDs (LED1-LED4 & LED6-LED9)

The power LED illuminates when board is turn ON and working. The configuration done LED illuminates when the FPGA is programmed. The reset LED illuminates when the board is in reset state. The user programmable LEDs are connected in common anode configuration. Hence driving a low signal (logic “0”) on LED pin will turn ON the corresponding LED. Signal directions are relative to the FPGA (Cyclone V GT device - U9).

[Table 2-9](#) lists LEDs pinout.

Board Reference	Signal Name	Direction (FPGA)	Type	Description	FPGA (U9) Pin
LED3	STATUS_LED1	Output	VCC_2_5	User LEDs - User Programmable LED	V19
LED4	STATUS_LED2	Output	VCC_2_5	User LEDs - User Programmable LED	V20
LED6	STATUS_LED4	Output	VCC_2_5	User LEDs - User Programmable LED	U22
LED7	SYS_RESET_N	Input	VCC_3_3	Reset LED - Illuminates when the board is in reset condition	T10
LED8	CONF_DONE	Bidirectional	VCC_3_3	FPGA Config. Done LED - Illuminates when the FPGA is configured through JTAG header successfully	J6
LED1	HSMC_PSNTN	-	VCC_3_3_HSMC	Illuminates when the HSMC is present	U21
LED9	VCC_3_3_ps	-	VCC_3_3	Illuminates when board is turn ON.	-

Reset Switch (SW6)

User-defined reset push-button (SW6) is acts as Global Reset switch. On pressing the switch an active low (logic “0”) reset signal is generated. Signal directions are relative to the FPGA (Cyclone V GT device - U9). [Table 2-10](#) shows the reset switch pinout.

Table 2-10. Reset Switch (SW6) Pinout

Board Reference	Signal Name	Direction (FPGA)	Type	Description	FPGA (U9) Pin
SW6	SYS_RESET_N	Input	VCC_3_3	System Reset	T10

Push-button Switches (SW2-SW5)

SW2 to SW5 are push-button switches and are used to provide to designs in the Cyclone V GT device. Each switch is connected to the Cyclone V GT general-purpose I/O pin with pull-up resistor. On pressing the switch, an active low (logic “0”) signal is generated.

Signal directions are relative to the FPGA (Cyclone V GT device - U9). [Table 2-11](#) shows the push-button switches pinout.

Table 2-11. Push-button (SW2-SW5) Switches Pinout

Board Reference	Signal Name	Direction (FPGA)	Type	Description	FPGA (U9) Pin
SW2	PB1	Input	VCC_3_3	User defined switch	U13
SW3	PB2	Input	VCC_3_3	User defined switch	T14
SW4	PB3	Input	VCC_3_3	User defined switch	T15
SW5	PB4	Input	VCC_3_3	User defined switch	R15

USB 3.0 Connectors (CON2-CON7)

The eUSB 3.0 development board having six B-Type USB 3.0 Connectors directly connected to Altera Transceiver.

These connectors are used for the USB 3.0 interface to the board. All these connectors are connected to the FPGA Transceiver pins from which we can use at a time only 3 Transceiver at a time. Hence, from connectors at a time only 3 can be used.



For more information, please refer to [Cyclone V Device Hand Book](#).

CON2

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

[Table 2-12](#) shows the USB 3.0 connector (CON2) signal name, signal direction, type and board reference pin.

Table 2-12. USB 3.0 Connector (CON2) Pinout

Connector Reference	Signal Name	Direction FPGA	Type	CON2 Pin	FPGA (U9) Pin
V_Bus	u30_vbus1	Input	VCC_1_8	1	C10
SSTXN	u30_device_sstxn1	Output	1.5 V PCML	5	Y3
SSTXP	u30_device_sstxp1	Output	1.5 V PCML	6	Y4
SSRXN	u30_device_ssrxn1	Input	1.5 V PCML	8	AA1
SSRXP	u30_device_ssrxp1	Input	1.5 V PCML	9	AA2

CON3

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

[Table 2-13](#) shows the USB 3.0 connector (CON3) signal name, signal direction, type and board reference pin.

Table 2-13. USB 3.0 Connector (CON3) Pinout

Connector Reference	Signal Name	Direction FPGA	Type	CON3 Pin	FPGA (U9) Pin
V_Bus	u30_vbus2	Input	VCC_1_8	1	A10
SSTXN	u30_device_sstxn2	Output	1.5 V PCML	5	U1
SSTXP	u30_device_sstxp2	Output	1.5 V PCML	6	U2

Table 2-13. USB 3.0 Connector (CON3) Pinout

Connector Reference	Signal Name	Direction FPGA	Type	CON3 Pin	FPGA (U9) Pin
SSRXN	u30_device_ssrnx2	Input	1.5 V PCML	8	W1
SSRXP	u30_device_ssrxp2	Input	1.5 V PCML	9	W2

CON4

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

[Table 2-14](#) shows the USB 3.0 connector (CON4) signal name, signal direction, type and board reference pin.

Table 2-14. USB 3.0 Connector (CON4) Pinout

Connector Reference	Signal Name	Direction FPGA	Type	CO4 Pin	FPGA (U9) Pin
V_Bus	u30_vbus3	Input	VCC_1_8	1	E11
SSTXN	u30_device_sstxn3	Output	1.5 V PCML	5	N1
SSTXP	u30_device_sstxp3	Output	1.5 V PCML	6	N2
SSRXN	u30_device_ssrnx3	Input	1.5 V PCML	8	R1
SSRXP	u30_device_ssrxp3	Input	1.5 V PCML	9	R2

CON5

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

[Table 2-15](#) shows the USB 3.0 connector (CON5) signal name, signal direction, type and board reference pin.

Table 2-15. USB 3.0 Connector (CON5) Pinout

Connector Reference	Signal Name	Direction FPGA	Type	CON5 Pin	FPGA (U9) Pin
V_Bus	u30_vbus4	Input	VCC_1_8	1	D11
SSTXN	u30_device_sstxn4	Output	1.5 V PCML	5	J1
SSTXP	u30_device_sstxp4	Output	1.5 V PCML	6	J2

Table 2-15. USB 3.0 Connector (CON5) Pinout

Connector Reference	Signal Name	Direction FPGA	Type	CON5 Pin	FPGA (U9) Pin
SSRXN	u30_device_ssrnx4	Input	1.5 V PCML	8	L1
SSRXP	u30_device_ssrxp4	Input	1.5 V PCML	9	L2

CON6

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

[Table 2-16](#) shows the USB 3.0 connector (CON6) signal name, signal direction, type and board reference pin.

Table 2-16. USB 3.0 Connector (CON6) Pinout

Connector Reference	Signal Name	Direction FPGA	Type	CON6 Pin	FPGA (U9) Pin
V_Bus	u30_vbus5	Input	VCC_1_8	1	C11
SSTXN	u30_device_sstxn5	Output	1.5 V PCML	5	E1
SSTXP	u30_device_sstxp5	Output	1.5 V PCML	6	E2
SSRXN	u30_device_ssrnx5	Input	1.5 V PCML	8	G1
SSRXP	u30_device_ssrxp5	Input	1.5 V PCML	9	G2

CON7

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

[Table 2-17](#) shows the USB 3.0 connector (CON7) signal name, signal direction, type and board reference pin.

Table 2-17. USB 3.0 Connector (CON7) Pinout

Connector Reference	Signal Name	Direction FPGA	Type	CON7 Pin	FPGA (U9) Pin
V_Bus	u30_vbus6	Input	VCC_1_8	1	B11
SSTXN	u30_device_sstxn6	Output	1.5 V PCML	5	D3
SSTXP	u30_device_sstxp6	Output	1.5 V PCML	6	D4

Table 2-17. USB 3.0 Connector (CON7) Pinout

Connector Reference	Signal Name	Direction FPGA	Type	CON7 Pin	FPGA (U9) Pin
SSRXN	u30_device_ssrnx6	Input	1.5 V PCML	8	C1
SSRXP	u30_device_ssrxp6	Input	1.5 V PCML	9	C2

SD Card Connector (CON8)

The board includes a SD card connector. Features of the SD card connector is listed below:

1. Withstands higher force of card insertion
Metal cover extends over the back of the connector allowing it to withstand force of up to 400 N (static load) when dropped or accidentally hit.
2. No damage to the card when accidentally pulled-out
The connectors will release the card when a moderate pull-out force of about 4 N is applied. There will be no damage to the lock components and all connector functions will not be affected.
3. Accidental card fall-out prevention
Built-in lock feature holds the card securely in place.
4. Reliable Card Insertion and Withdrawal
Built-in Push-in / Push-out ejection mechanism assures simple and reliable card insertion and withdrawal.
5. Designed to accept Secure Digital I/O card (Built-in Ground Contact)
The connector allows use of various expansion modules, including the Bluetooth communication modules.

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

Table 2-18 shows the SD card connector signal name, signal direction, type and board reference pin.

Connector Reference	Signal Name	Direction (FPGA)	Type	CON8 Pin	FPGA (U9) Pin
DATA0	MEM_SDC1_D0	Bidirectional	VCC_3_3	7	L9
DATA1	MEM_SDC1_D1	Bidirectional	VCC_3_3	8	L8
DATA2	MEM_SDC1_D2	Bidirectional	VCC_3_3	9	M8
DATA3	MEM_SDC1_D3	Bidirectional	VCC_3_3	1	M10
CMD	MEM_SDC1_CMD	Output	VCC_3_3	2	R12
CLK	MEM_SDC1_CLK	Output	VCC_3_3	5	AB10
CRD_DT	MEM_SDC1_CD_N	Input	VCC_3_3	10	P14
WP	MEM_SDC1_WP_N	Input	VCC_3_3	11	R14

Expansion Interface

HSMC Connector (J3)

The Altera High Speed Mezzanine Card (HSMC) specification defines the electrical and mechanical properties of a high speed mezzanine card adapter interface for FPGA-based motherboards. HSMC connector is pinned out to FPGA bank 5A and 5B with VCC_2_5 I/O voltage level.

The HSMC connectors provide the interface between a host board and a mezzanine card. The 'header' part is on a mezzanine card and plugs into the 'socket' part on a host board. Mezzanine cards are daughter cards which feature electrical components and/or interfaces. The mezzanine cards may come in several different sizes, interfaces and IO standard support, but all share some common attributes. When installed onto a host board, the mezzanine cards are oriented parallel to the host board PCB plane and are installed onto the HSMC connector.

This specification should allow for the design of interoperable motherboards and add-on cards by different manufacturers that can inter operate and utilize the high performance I/O features found in today's FPGA devices. The

connector is based on the Samtec 0.5mm pitch, surface-mount QTH/QSH family of connectors. Compatible versions with this spec vary from 132 to 192 physical pins. The highest frequency signals are the clock-data-recovery differential signals found in bank 1. Outputs from the FPGA are intended to be A/C coupled and the inputs to the FPGA are intended to be DC coupled. Also in bank 1, there are dedicated JTAG, SMBus and clock signals. The main CMOS/LVDS interface signals, including LVDS/CMOS clocks, are found in banks 2 and 3. Both 12V and 3.3V power pins are also found in banks 2 and 3 in HSMC Card.

This HSMC interface is specifically designed for using with Camera interface daughter cards. Hence, the HSMC interface on the board does not follow the standard HSMC pin-outs. It only allows to use the daughter board developed by SLS for camera interface.

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

[Table 2-19](#) shows the HSMC connector's I/O signal name, signal direction, type and board reference pin.

Connector Reference	Signal Name	Direction (FPGA)	Type	J3 Pin	FPGA (U9) Pin
CLKIN	HSMC_CLK_IN	Input	VCC_2_5	40	M16
CLKOUT	S_HSMC_CLK_OUT	Output	VCC_2_5	39	A8
DOUT0	AP_DOUT0	Input	VCC_2_5	47	D22
DOUT1	AP_DOUT1	Input	VCC_2_5	49	E20
DOUT2	AP_DOUT2	Input	VCC_2_5	53	E21
DOUT3	AP_DOUT3	Input	VCC_2_5	55	F18
DOUT4	AP_DOUT4	Input	VCC_2_5	59	F19
DOUT5	AP_DOUT5	Input	VCC_2_5	61	F20
DOUT6	AP_DOUT6	Input	VCC_2_5	65	G20
DOUT7	AP_DOUT7	Input	VCC_2_5	67	G21
DOUT8	AP_DOUT8	Input	VCC_2_5	71	H19
DOUT9	AP_DOUT9	Input	VCC_2_5	73	H20

Table 2-19. HSMC Connector (J3) Pinout

Connector Reference	Signal Name	Direction (FPGA)	Type	J3 Pin	FPGA (U9) Pin
DOUT10	AP_DOUT10	Input	VCC_2_5	77	J16
DOUT11	AP_DOUT11	Input	VCC_2_5	79	J17
LINE_VALID	AP_LINE_VALID	Input	VCC_2_5	83	J19
FRAME_VALID	AP_FRAME_VALID	Input	VCC_2_5	85	J21
SHUTTER	AP_SHUTTER	Input	VCC_2_5	89	K16
SDA	AP_SDA	Input	VCC_2_5	91	K19
RESET	AP_RESET	Output	VCC_2_5	72	G22
TRIGGER	AP_TRIGGER	Output	VCC_2_5	74	H18
EXT_CLKIN	AP_EXT_CLKIN	Output	VCC_2_5	78	H21
PIXCLK	AP_PIXCLK	Input	VCC_2_5	84	J18
SCL	AP_SCL	Output	VCC_2_5	90	K15
OV_DOUT0	OV_DOUT0	Input	VCC_2_5	101	K21
OV_DOUT1	OV_DOUT1	Input	VCC_2_5	103	L15
OV_DOUT2	OV_DOUT2	Input	VCC_2_5	107	L18
OV_DOUT3	OV_DOUT3	Input	VCC_2_5	109	L19
OV_DOUT4	OV_DOUT4	Input	VCC_2_5	113	L20
OV_DOUT5	OV_DOUT5	Input	VCC_2_5	115	P19
OV_DOUT6	OV_DOUT6	Input	VCC_2_5	119	R16
OV_DOUT7	OV_DOUT7	Input	VCC_2_5	121	R17
OV_DOUT8	OV_DOUT8	Input	VCC_2_5	125	R19
OV_DOUT9	OV_DOUT9	Input	VCC_2_5	127	R20
OV_HRF	OV_HREF	Input	VCC_2_5	131	R21
OV_VSYNC	OV_VSYNC	Input	VCC_2_5	133	R22
OV_PCLK	OV_PCLK	Input	VCC_2_5	137	T17
OV_PWDN	OV_PWDN	Output	VCC_2_5	143	T18
OV_XCLK	OV_XCLK	Output	VCC_2_5	145	T19

Table 2-19. HSMC Connector (J3) Pinout

Connector Reference	Signal Name	Direction (FPGA)	Type	J3 Pin	FPGA (U9) Pin
OV_SCL	OV_SCL	Output	VCC_2_5	149	T20
CLKOUT_P	HSMC_CLKOUT_P	-	VCC_2_5	155	-
CLKOUT_N	HSMC_CLKOUT_N	-	VCC_2_5	157	-
OV_SDA	OV_SDA	Bidirectional	VCC_2_5	150	T22
CLKIN_P	HSMC_CLKIN_P	-	VCC_2_5	156	-
CLKIN_N	HSMC_CLKIN_N	-	VCC_2_5	158	-
PSNTN	HSMC_PSNTN	Input	VCC_2_5	160	U21

Power Supply

The eUSB 3.0 development board powered by external 15V-20V, 3A DC power supply at right-angle 2.5 mm power jack. This input power is regulated down to different power rails using power supply.

There are three types of voltage regulators on the power supply to control the different voltage rails available on the eUSB 3.0 development board.

Termination voltage regulators provide +0.9V, +1.1V, +1.2V, +1.8V, +2.5V, +3.3V, +5V and +12V on the board. [Table 2-20](#) below describes each voltage regulator.

Table 2-20. Power Supply Components

Board Reference	Part Number	Manufacturer	Type	Current Output	Voltage Output	Connected to
U1	LTC3855EUJ #PBF	Linear Technology	Step-Down (Buck)	7A	VCC_5	• CH # 1 Provided to other regulators
				3A	VCC_12	• CH # 2 HSMC & FAN
U2	LTC3616 EUDD #PBF	Linear Technology	Step-Down (Buck)	6A	VCC_1_1	• VCC (Core supply of FPGA)

Board Reference	Part Number	Manufacturer	Type	Current Output	Voltage Output	Connected to
U3	LTC3614EUDD #PBF	Linear Technology	Step-Down (Buck)	4A	VCC_3_3	<ul style="list-style-type: none"> • HSMC • CFI FLASH • SD CARD • SDRAM • VCC IO • VCC PD • EPCS
U4	RT9040G QWWDFN-10	Richtek	DDR2 Termination Regulator	-	-	<ul style="list-style-type: none"> • DDR2 Termination
U5	LTC3614EUDD #PBF	Linear Technology	Step-Down (Buck)	4A	VCC_2_5	<ul style="list-style-type: none"> • HSMC IO • VCC IO • VCC PGM • VCCPD • VCC_AUX • VCC_FPLL • VCCH_GXBL
U6	LT3083EFE #PB- TSSOP16	Linear Technology	LDO Regulator	3A	VCC_5	<ul style="list-style-type: none"> • VCCE_GXBL • VCCL_GXBL
U8	LTC3614EUDD #PBF	Linear Technology	Step-Down (Buck)	4A	VCC_1_8	<ul style="list-style-type: none"> • DDR2 SDRAM • VCC IO

Power Switch (SW1)

Power switch is used for **ON** and **OFF** the board when the power is supplied from the DC input jack.

Clock Circuitry

Crystal Oscillator (Y1- Y4)

The development board supports various clock frequencies for IP Core running on FPGA transceiver and for system clock. It has on board crystal

oscillators for the clock inputs which can be directly used in the design by various IP Cores, memories and other devices.

Signal directions are relative to the FPGA (Cyclone V GT device - U9).

[Table 2-21](#) shows the crystal oscillator pinout.

<i>Table 2-21. Crystal Oscillator (Y1-Y4) Pinout</i>				
Board Reference	Signal Name	Direction	Type	FPGA Pin
Y1 . 3	OSC_CLK	Input	VCC_3_3	P9
Y2 . 3	48MHZ_CLK	Input	VCC_1_8	K7
Y3 . 4	REFCLK_125_P0	Input	VCC_2_5	V4
Y3 . 5	REFCLK_125_N0	Input	VCC_2_5	U4
Y4 . 4	REFCLK_125_P1	Input	VCC_2_5	F5
Y4 . 5	REFCLK_125_N1	Input	VCC_2_5	G4