

The Efficiency of the DDR & DDR2 SDRAM Controller Compiler

Introduction

This white paper on the efficiency of the Altera® DDR & DDR2 SDRAM Controller Compiler discusses the following topics:

- “Bandwidth” on page 1
- “Efficiency—Worst-Case Scenario” on page 1
- “Efficiency—Best-Case Scenario” on page 1
- “The Effect of Refresh” on page 2
- “Read Latency” on page 2
- “An Application Example” on page 2
- “Increase the Efficiency” on page 3

Bandwidth

Improving the efficiency of either the DDR or DDR2 SDRAM controller improves the bandwidth. The maximum bandwidth for a desired situation is given by:

$$\text{Bandwidth} = \text{DDR SDRAM bus width} \times 2 \times \text{frequency of operation} \times \text{efficiency}$$

For example, running a 16-bit DDR SDRAM interface at a frequency of 100 MHz:

$$\text{Bandwidth} = 16 \text{ bits} \times 2 \text{ clock edges} \times 100 \text{ MHz} \times \text{efficiency}$$

The Altera DDR or DDR2 SDRAM controller can be up to 90% efficient depending on the conditions—it can be as low as 10%. Therefore the maximum bandwidth is given by:

$$\text{bandwidth} = 3.2 \text{ Gbps} \times 0.9 = 2.88 \text{ Gbps}$$

Efficiency—Worst-Case Scenario

The worst-case scenario arises when the DDR or DDR2 SDRAM controller is swapping between writes and reads and simultaneously addressing is forcing a row to be opened and closed on every transaction. Assuming that the address bus is in the default order—chip select, bank, row, column—so 4,096 is above bit 10, the column boundary, write to address 0, read from address 4,096, then write to address 1, and read from address 4,097 etc.

The efficiency for this worst-case scenario is around 10%. A write followed by read in the same column has an efficiency of around 25%.

Such reading and writing a large proportion of the time from a system perspective means that the use of DDR SDRAM memory should be reviewed. It is likely that other memory types (e.g., SRAM) may provide a more economical system solution.

Efficiency—Best-Case Scenario

The best-case scenario arises with long bursts of writes followed by long bursts of reads. For example, in the case of back-to-back writes of length 4 (local side), the efficiency (ignoring refresh) is approaching 100%. However, that is clearly an unrealistic use of the memory. A more typical best case scenario is 10 writes (burst of 4 local side) to the same column followed by 10 reads.

The efficiency in this best-case scenario is around 92%.

The Effect of Refresh

A refresh, in terms of cycles, is constructed of two components: the precharge command then waiting for the auto-refresh period. Both of these components are given on the specific memory device data sheet. However, the following example uses the following user guide values:

precharge command = 3

auto-refresh period = 10

For these values a refresh pauses read/write operations for 13 cycles. i.e., a refresh consumes approximately 13 cycles every 7.6 μ s.

At 100 MHz this equates to $13 \times 10\text{ns} / 7.6\mu\text{s} = 1.7\%$.

At 133 MHz this equates to 1.3%.

Subtract these percentages from the efficiency calculated earlier.

Note: following a refresh all the banks are closed, so any activity following a refresh takes longer than an activity occurring in an already open column.

Read Latency

Read latency depends upon system and DDR or DDR2 SDRAM controller parameters. Assuming the DDR or DDR2 SDRAM controller is idle and the read command is issued at exactly the same time as the refresh is about to start, Table 1 shows the worst case read latency, which depends on system and DDR or DDR2 SDRAM controller settings e.g., CAS latency in use and the MegaCore® function configuration.

Table 1. Worst Case Read Latency

Action		Cycles	
		Minimum	Maximum
Precharge Time		2	3
Refresh Period		10	14
Open (Activate)		2	3
Read		1	1
CAS Latency		2 (3 for DDR2 SDRAM)	3 (5 for DDR2 SDRAM)
RTD		0	2
Resynchronization	Resynchronization register	1	1
	Re-clock to positive edge	1	1

Note: if the controller is not idle, but has commands in its command FIFO buffer (up to 4), it must first execute the other (up to 3) commands.

An Application Example

Using ATM cells of 56 bytes and assuming the DDR SDRAM data width is 16 bits (32 bits local side). Then 14 cycles of 32 bits are required for each cell to be written ($14 \text{ cycles} \times 4 \text{ bytes/cycle} = 56 \text{ bytes}$). Is it better to use 7 bursts of 2 or 2 bursts of 8 (with the last 2 bytes masked off).

For 7 writes, 7 reads, and bursts of 2 (DDR SDRAM side) random addresses, the efficiency is 60%.

For 2 writes, 2 reads, and bursts of 8 (DDR SDRAM side) random addresses, the efficiency is 52%.

Note: these efficiencies are from simulation measurements, do not include the effect of refresh, and have one chip select.

Increase the Efficiency

Examine the following questions about the system, to determine if the system can achieve higher efficiency:

- Are you going to use random addresses? If no, efficiencies can be expected to improve because most of the overhead is the bank management.
- Can the row, bank, and column address order be swapped to give longer contiguous spaces? Or spaces that better fit the application?
- Can you control the position of the refresh?
- Can you insert a small buffer to get a group of writes, say 4 cells rather than 1?



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