Synchronous Ethernet Solutions with Altera FPGAs and Silicon Labs Jitter-Attenuating PLLs

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Introduction

Synchronous clock signals are required for proper operation of voice communications, cellular wireless networks, passive optical networks (PONs), and a variety of other time-critical networking applications. Traditional time division multiplexed (TDM) telecom equipment—to support standards like Synchonous Optical Networking (SONET) and Synchronous Digital Hierarchy (SDH)—operate with synchronized clock signals. Nodes in these networks are synchronized to a primary reference clock (PRC) or primary reference source (PRS) with long-term frequency accuracy better than 1 part in 10^{11}.

The PRS/PRC clocks in TDM networks are provided by highly accurate and stable atomic clocks, or signals from the global positioning system (GPS). The clocks are then distributed to all the nodes in the network over the same connections that transport clients' voice and data. The network nodes then synchronize their locally generated clocks to the PRS/PRC clock.

Ethernet has become the network interface of choice in enterprise, metro, and some core networks. Ethernet networks can be used to transport voice, data, and video at high data rates for substantially lower equipment and service costs than traditional networks. Large capital savings can be realized by using Ethernet for synchronizing network nodes instead of using a more expensive specialized synchronous network.

The IEEE 802.3 Ethernet standard is not specified to accurately transfer a clock from the transmitter to the receiver. To make synchronous operation possible on Ethernet networks, the ITU-T G.8262 standard specifies Synchronous-Ethernet (SyncE). SyncE is similar to SDH clock synchronization feature, but it runs over an Ethernet physical link. For more information on SyncE, refer to the ITU-T G.8262 website (www.itu.int/rec/T-REC-G.8262).

This paper describes a multiple-port 1G/10 Gbps Ethernet SyncE synchronization solution jointly developed by Altera and Silicon Labs, with a complete stable clock loop.

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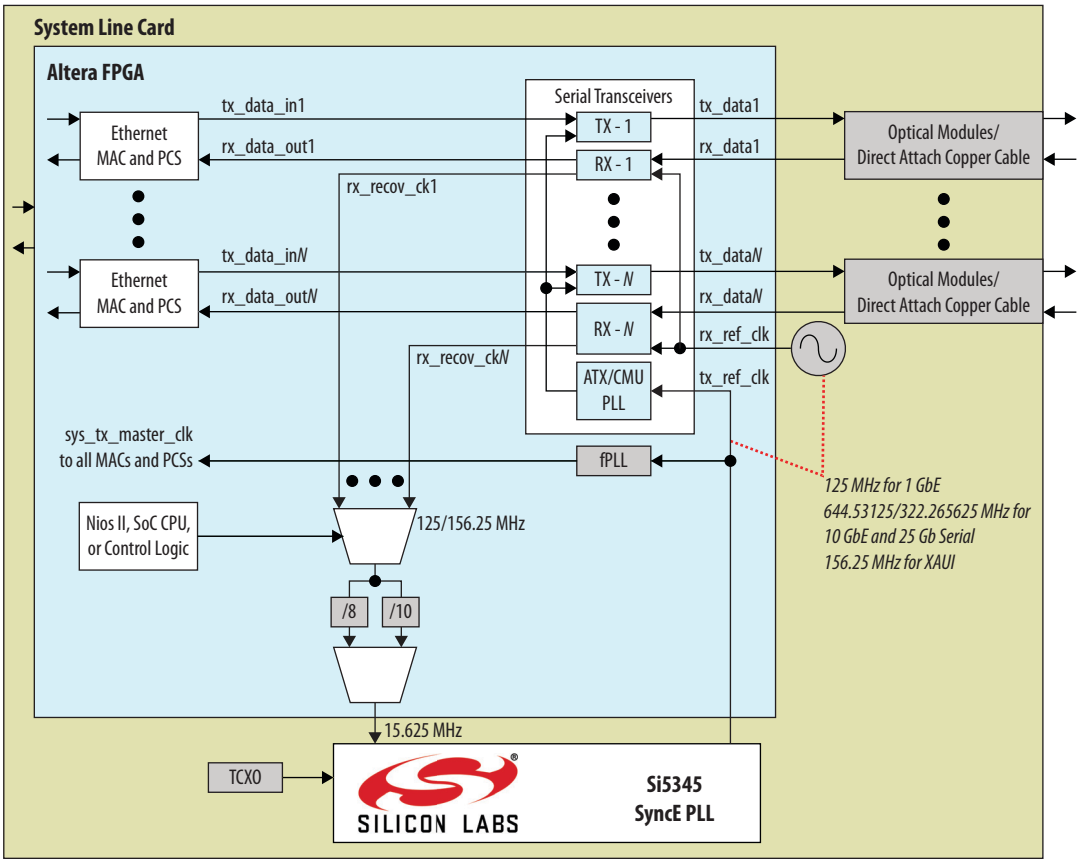
The Altera and Silicon Labs' SyncE Solution

Altera and Silicon Labs have developed a high-performance SyncE solution based on the two companies' products. A high-level system diagram is shown in Figure 1. This solution consists of an Altera® SyncE reference design implementing up to ten 1G/10 Gbps Ethernet (1G/10GbE) ports in Altera's Stratix® V FPGA interoperating with Silicon Labs' Si5345 jitter-attenuating phase-locked loop (PLL) to provide a complete SyncE clock recovery, clock selection, and synchronization sub-system. This solution can be used in wireless or wireline networking equipment to realize an accurate SyncE clock synchronization.

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



Timing Requirements for Synchronous Ethernet

Networks utilizing SyncE benefit from high reliability, which is essential for telecommunications data transmission. However, designers must pay careful attention to their timing architecture to ensure systems meet all of the performance requirements for SyncE as defined by ITU-T G.8262.

A timing subsystem supporting SyncE typically must support the following functions:

- Clock recovery from one or more fiber or copper Ethernet receive ports
- Ability to detect the loss of signal or excessive frequency drift from each clock source and select another source with minimal or no interruption of the system timing
- Ability to support holdover if all of the reference clocks are lost
- Jitter and wander filtering of the recovered clock
- Generation of all system clock frequencies from a single recovered clock frequency
- Ability for the TCXO or OCXO reference oscillator and PLL to maintain stability and accuracy
  - ±4.6 ppm frequency accuracy
  - Limited phase wander as measured by time deviation (TDEV) and maximum time interval error (MTIE) measurements

Altera's SyncE Reference Design

Figure 1 illustrates an Altera Stratix V FPGA SyncE reference design that consists of multiple 1G/10Gb Ethernet media access control (MAC) and physical coding sublayer (PCS) and physical medium attachment (PMA) (PHY) intellectual property (IP) instances. These PHY IP cores recover the receiver (RX) clocks from their respective 1G/10 Gbps Ethernet ports. The reference design selects one clock as a master system clock based on the SyncE management software control and sends it to an FPGA output. Under the standard, a SyncE clock system has only one primary master clock traceable to a carrier atomic or GPS-driven PRC, similar to the clock configuration of an SDH network. The FPGA core is filled with instances of a digital noise-maker design to create a real world scenario for measuring the clock parameters.

The Si5345 ITU-T G.8262 SyncE standard-compliant PLL from Silicon Labs then attenuates the selected clock signal's wander and jitter to within the SyncE specification. This stabilized clock is used to feed the FPGA's serial transmitter (TX) PLL in sync with the master Ethernet port's clock frequency to realize a complete synchronization loop. This reference design can support multiple reconfigurable serial transceiver channels in SyncE mode at 1 Gbps or 10 Gbps line rate using Altera's Stratix V GX FPGA Transceiver Signal Integrity Development Kit. The design can be modified to support 40Gb and 100Gb Ethernet MAC and PHY IP, and clocks as well. For the Si5345 G.8262 synchronous Ethernet full compliance test results, refer to the Si5345 Synchronous Ethernet G.8262 Compliance Test Results document on the Silicon Labs website (www.silabs.com).

In addition to providing G.8262-compliant timing, the Si5345 PLL helps to minimize system cost and complexity. The Si5345 requires no external VCXO, which keeps bill of materials cost to a minimum. In addition, the Si5345 contains on-chip power supply regulation, which allows it to be connected directly to switching power supplies with no need for expensive power supply filtering to achieve high performance.

Jitter and Wander Performance Requirements

To supply a clean reference clock for the serial transceivers' TX PLLs synchronous to the RX recovered clock, the RX clocks from multiple Ethernet ports are multiplexed in the FPGA fabric to the external jitter-attenuating PLL. Maintaining a clean clock in this process can be challenging because the FPGA clock network resources are limited and the logic-based multiplexers for clock signals can be jittery and may cause duty cycle distortion in clock signals. Altera's SyncE reference design manages and limits this phase noise and Silicon Labs Si5345 PLL does the rest to create a clean clock frequency.

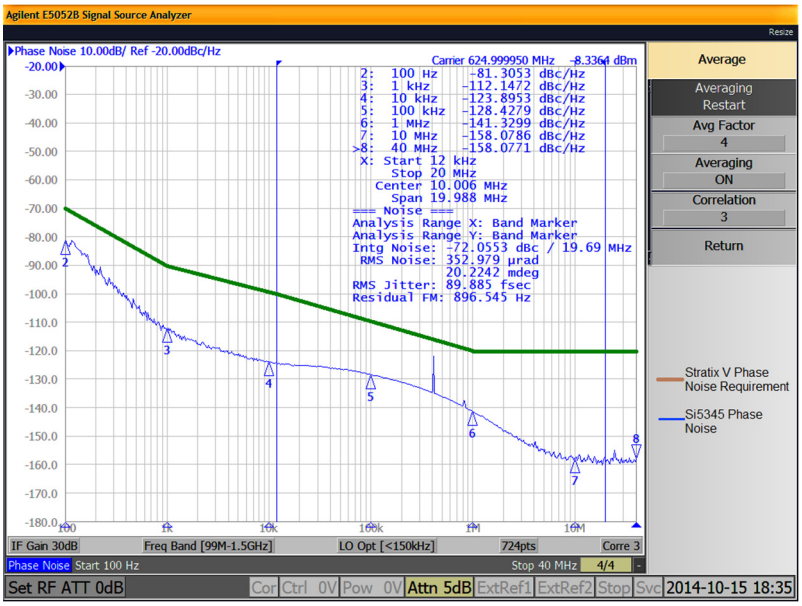
G.8262-compliant designs for high-bandwidth Ethernet require very low jitter from the clock driving the Ethernet PHYs or optical modules. The requirements are summarized in Table 1:

Table 1. G.8262 Jitter Requirements

Application	Jitter Requirements per IEEE 802.3
1 Gigabit Ethernet	13.91ps RMS
10 Gigabit Ethernet	1.91ps RMS

Additional margin beyond the standards requirement is usually necessary from the output of the clock PLL, since clock routing and SERDES transmitters each add an incremental amount of additive jitter. For these reasons, it is beneficial to choose a PLL with very low output jitter. As shown in Figure 2, the Si5345 device offers <100 fs typical jitter from 12 kHz -20 MHz and very low phase noise, which allows designers to have more flexibility in their clock tree and ensures support for up to 100 Gigabit applications.

Figure 2. Si5345 Phase Noise vs. Stratix V FPGA Requirements for 10G Ethernet



The wander tolerance of the PLL must also be considered. A PLL loop bandwidth below 10 Hz is required for the PLL to adequately filter wander for SyncE. G.8262 specifies two options for Ethernet Equipment Clocks (EEC). EEC Option 1 requires a loop bandwidth between 1-10Hz. EEC Option 2 is more stringent and requires a loop bandwidth of 0.1Hz. Achieving low loop bandwidths can be difficult for PLLs that need external loop filter components. In addition, the external components and traces are susceptible to noise coupling from other PCB signals.

To alleviate these concerns, the Si5345 uses Silicon Labs' patented DSPLL technology that supports loop bandwidths as low as 0.1 Hz without the need for external loop filter components. This, combined with the low 100fs jitter performance, allows the Si5345 to provide a single-chip PLL solution that is fully compliant with G.8262.

Redundant Clock Switching and Holdover

SyncE systems require redundant clock sources to maintain operation in cases where one or more clock sources fail. The Si5345 supports up to four clock inputs with automatic input switching in case of failure. If multiple SyncE recovered clock sources are available, these may be routed to the Si5345 clock inputs. When transitioning from one input clock to another, the PLL maintains the integrity of the output clock without any glitch, undesired frequency, or phase transients. If multiple input clocks in a SyncE system are locked in frequency but not in phase, the Si5345 provides "hitless" switching where the phase of the output clock does not change when the PLL switches between input clocks with different phases.

In a failure condition where the input clock sources are lost, the Si5345 switches to holdover operation using its reference oscillator. In this mode, the Si5345 averages up to 120 seconds of valid historical frequency data to ensure a smooth transition into holdover. The stability requirements of the design will dictate the type of reference oscillator required. Typically TCXOs are suitable for Stratum 3 stability, while OCXOs are required for Stratum 3E.

Tests Performed at Altera

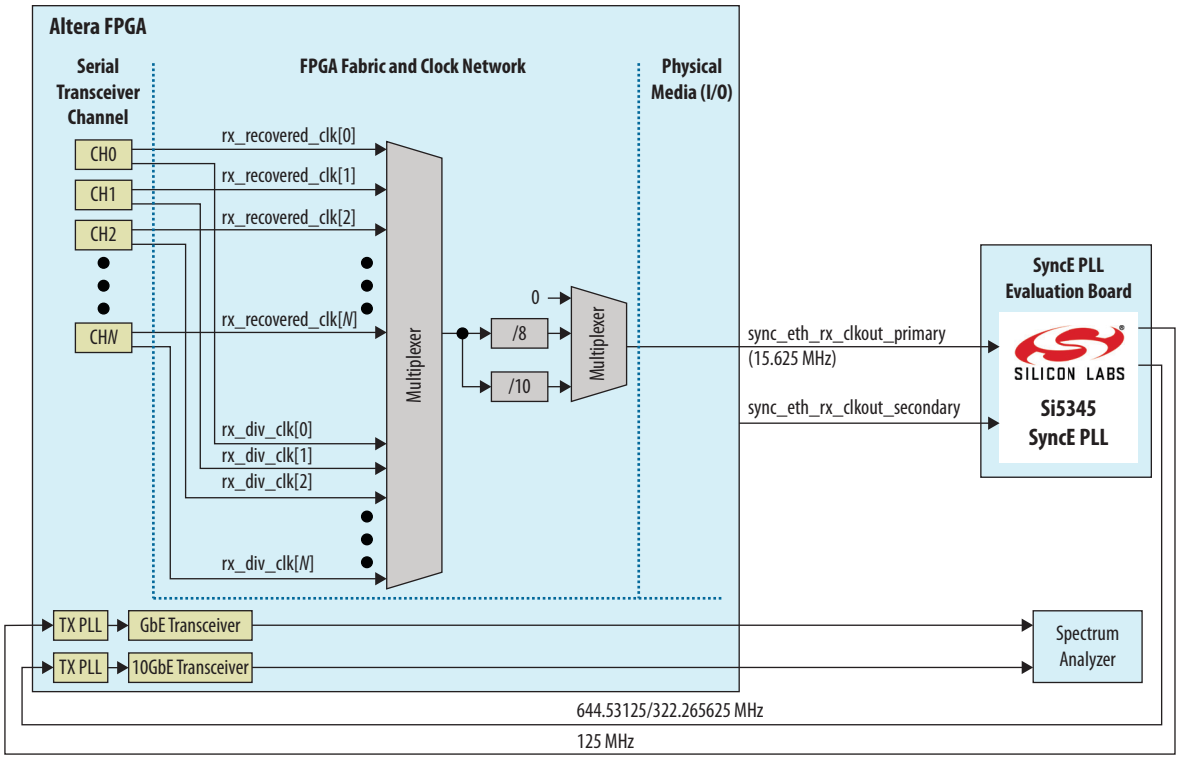
The Altera-Silicon Labs SyncE interoperability and jitter hardware test setup is shown in Figure 3. Each 1G/10GbE port can be configured dynamically by the user to operate at 1G or 10G data rate.

The 1G ports' respective `rx_recovered_clk` outputs' frequency is 125 MHz and their respective `rx_div_clk` outputs are not used. The 10G ports' respective `rx_recovered_clk` output signals are not used and their respective `rx_div_clk` outputs' frequency is 156.25 MHz.

The first multiplexer shown in the diagram after transceiver channels 0 to N selects one receiver recovered clock as the master clock source from among all the Ethernet ports. The ÷8 and ÷10 frequency dividers each generate a 15.625 MHz clock respectively for 1G and 10G Ethernet port groups. The second multiplexer selects the 15.625 MHz clock from among these two clocks as the system master clock or a zero to disable the clock output.

In many systems, two clock outputs feed the SyncE PLL as primary and secondary master clocks for clock redundancy and high availability. Therefore, two copies of the complete multiplexer and clock selector design are implemented in the FPGA, and output `sync_eth_rx_clkout_primary` and `sync_eth_rx_clkout_secondary` 15.625 MHz clock signals to the SyncE PLL.

Figure 3. Altera and Silicon Labs SyncE Jitter Test Setup



With this setup, Altera and Silicon Labs have validated that the jitter performance of Silicon Labs' Si5345 PLL meets the requirement of Altera's Stratix V FPGA input reference clock and that the serial transceiver output jitter meets G.8262 requirements. The test includes Silicon Labs' Si5345 PLL output jitter, phase noise tolerance at the PLL input, the clock synchronization loop's phase noise filtering capability, and the ability of the loop to withstand short-term and long-term input interruptions and discontinuities.

These are important performance metrics to distribute traceable and stable clock frequency over packet networks and enable network nodes to synchronize to the master clock, which ultimately enables the interoperability of carrier Ethernet and legacy networks.

Altera and Silicon Labs have jointly demonstrated a high-performance and flexible solution for frequency synchronization of telecom and data communication networks based on the SyncE standard using the Ethernet infrastructure.

Conclusion

Designing systems for ITU-T G.8262-compliant Synchronous Ethernet requires careful consideration of the timing architecture. Using a Stratix V FPGA, Altera's SyncE reference design handles all clock recovery, clock selection, and synchronization. Wander and jitter attenuation, holdover and optional clock input selection are solved by a Silicon Labs Si5345 PLL. Together, these devices have demonstrated a standards-compliant line card reference design for 1G and 10G SyncE with sufficient performance that is scalable to 100G applications.

Document Revision History

Table 2 shows the revision history for this document.

Table 2. Document Revision History

Date	Version	Changes
November 2015	1.0	Initial release.