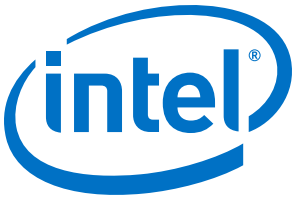

Intel® Quartus® Prime Design Suite Update Release Notes

Updated for Intel® Quartus® Prime Design Suite: **18.0.1**

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Contents

1. Intel® Quartus® Prime Design Suite Version 18.0 Update Release Notes

The *Intel® Quartus® Prime Design Suite Update Release Notes* describe the contents of Intel Quartus Prime Design Suite Version 18.0 software updates.

The Intel Quartus Prime Design Suite Version 18.0 updates apply only to Intel Quartus Prime Pro Edition.

Related Information

- Intel Quartus Prime Standard Edition Software and Device Support Release Notes Version 18.0
- Intel Quartus Prime Pro Edition Software and Device Support Release Notes Version 18.0

2. Issues Addressed in Update 1

2.1. Intel Quartus Prime Pro Edition Software

Intel Quartus Prime Software

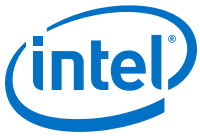
- Fixed an issue where unquoted service paths could allow a local attacker to potentially execute arbitrary code.
- Updated Python software and libraries.
- Enable Intel Quartus Prime to run on SUSE 11.
- Fixed an issue that caused the error message `error while loading shared libraries` when starting the `alterad` license software.

Intel Quartus Prime Software GUI

- Resolved issue that caused the **File ➤ Create/Update** menu command to be missing.
- Removed message the occurred when changing devices families from the **Assignments ➤ Device** menu.
- Removed unsupported **HPS Boot source** options from the Hard Processor System Intel Stratix® 10 FPGA IP GUI.

Intel Quartus Prime Device Support

- Added support for the following Intel Stratix 10 device families:
  - 1SG280HHF55
  - 1SX280H-S3
- Added support for Intel Arria® 10 SX family Smart Voltage ID (Smart VID) speed grade 3 device variants.
- Updated SERDES firmware to update algorithms and reduce calibration run time.
- For remote system upgrade (RSU) on Intel Stratix 10 devices, enabled the device to detect changes to the available images when nCONFIG is toggled.
- Added **Cold reset and trigger a remote Update** to HPS watchdog reset options.
- Enhanced JTAG connection stability for Intel Stratix 10 E-Tile devices.
- Enabled SOF support for Intel Stratix 10 L-Tile devices (1SX280L/1SX250L).
- Fixed an issue affecting Intel Stratix 10 devices where configuration with Avalon®-MM interfaces succeeds but the design is nonfunctional.
- Fixed an issue where the JTAG usercode reported by Intel Quartus Prime is incorrect, instead showing all Fs or a checksum value.



- Fixed an issue where reconfiguration would fail after a few mailbox messages had been sent from the FPGA design.
- Updated the mailbox client to return read data to write only unused registers.
- Fixed the following issues:
  - Fixes a problem in which, if an Intel Stratix 10 device was configured in VID slave mode, and the VID master timed out during reconfiguration, the Intel Stratix 10 device would fail to reconfigure.
  - For RSU, fixes a pin-conflict that prevented SDMIO16 from being used as the "load factory image" pin.
  - Fixed an issue that could cause unexpected CvP configuration errors, especially at data rates approximately 46 Mbps.
- Added more handling/recovery from bitstream errors over JTAG.
- Fixed the following issues:
  - If a configuration failure occurs, the CONFIG_STATUS from the target shows an incorrect status of all zeroes.
  - When using RSU and sending an RSU_STATUS query, the response might contain error-location values (LAST_FAIL_IMAGE_0, LAST_FAIL_IMAGE_1, ERROR_LOCATION, ERROR_DETAILS) that are incorrectly zero.
  - When using RSU, if theCPB0 or CPB1 fields become corrupted, the system might fail to boot to a factory image or application image.
  - Reads from QSPI unexpectedly fail.
- Fixed an intermittent issue where firmware would become unresponsive. NCONFIG is not toggled faster than once every 50 ms.
- Fixed a pin-conflict that prevented SDMIO16 from being used as the "load factory image" pin for RSU.
- Fixed an issue that could cause unexpected CvP configuration errors, especially at data rates approximately 46 Mbps.
- Fixed a problem in which CONFIG_STATUS from the target shows an incorrect status of all zeroes in event of a configuration failure.
- Fixed the following issues:
  - Added a feature in which HPS can use the RSU flow on upon triggering the watchdog timer.
  - Added support for the CANCEL mailbox command.
  - Fixes handling for several cases of corruption of parts of the bitstream, including correct use of nStatus, INIT_DONE, and CONF_DONE.
  - Adjusted the handling of RSU-update to make sure that HPS is wiped and access to QSPI is correctly configured during RSU.
  - Fixed handling of certain cases of warm-reset triggered from the HPS.
  - Fixed the handling of FAILACK state when using AVST configuration source.
  - Fixed an error in which reconfiguration of some non-HPS designs would erroneously attempt to perform HPS actions.
- Fixed issues that prevented the successful compilation of designs that instantiated the Intel Stratix 10 logic_module WYSIWYG.

- Fixed an issue where Intel Quartus Prime did not properly enable the Intel Stratix 10 HPS EMAC0 when the interface is exposed to the FPGA routing fabric.
- Unused transceiver tiles in Intel Stratix 10 devices are now powered-down.
- Updated transceiver calibration firmware for Intel Stratix 10 L-tile devices.
- Fixed the following issues:
  - When JTAG configuration interrupts QSPI configuration, QSPI is now disabled as the crypto input source.
  - HPS reconfiguration FPGA case now reports an error if phase2 bitstream CMF does not match with phase1 bitstream.
  - A configuration failure while RSU is enabled now causes a CNT warm reset to ensure next image load properly.
- The IBIS model status for Intel Stratix 10 is now set to Final.

Intel Quartus Prime Compilation and Design Flows

- Fixed a bug that occurred with port names that have periods but no brackets.
- Added a design check to verify that imported partitions do not share a rowclock region. This fix addresses an issue in hierarchical flows that use imported partitions.
- Fixed an issue when running Rapid Recompile from the Intel Quartus Prime GUI.
- Fixed an issue that caused the following error:

```
Internal Error: Sub-system: RTM,
File: /quartus/tsm/rtm/rtm_timing_analysis_iterator.cpp, Line: 610
```

- For incremental compilation flows, added a warning on export of a partition that contains a preserved global signal.
- Fixed an issue that caused the following error:

```
Internal Error: Sub-system: CDB_ATOM,
File: /quartus/db/cdb_atom/cdb_atom_sys.cpp, Line: 2735
```

Fitter

- For Intel Stratix 10 devices, enhanced algorithm to handle circuits with too many hold violations without attempting to fix all hold violations.
- For Intel Stratix 10 devices, fixed the following assertion failure that might occur during the Finalize phase:

```
Internal Error: Sub-system: TDC,
File: /quartus/tsm/tdc/tdc_accessories_delay_budget.cpp, Line: 1381
```

- For devices, fixed the following error that can occur when a core FF drives a multisector-level gated clock:

```
Internal Error: Sub-system: FMAIN,
File: /quartus/fitter/fmain/fmain_location_constraint.cpp, Line: 339
```

- Fixed a bug where clustering can incorrectly calculate the region of a carry-chain. The bug appears as a user error with an impossible region boundary.
- Added support for physically aware set MAX_FANOUT duplication.

- Fixed the following error during report generation for Intel Stratix 10 compilations that failed to route a clock signal with sector-level clock gates:

```
Internal Error: Sub-system: CCLK,
File: /quartus/periph/cclk/cclk_gen7_promoted_clock_tree.cpp, Line: 191
```

- Enabled a clock signal to feed UIB interfaces or ESRAM interfaces at the top and bottom of a chip simultaneously.
- Fixed a crash in Intel Stratix 10 bottom-up preservation flows that can happen when logic is preserved near HSSI or I/O interfaces that perform dedicated optimizations for P2C and C2P transfers.
- Improved recoverable logic computation to provide more accurate logic utilization resource reporting.
- Fixed the following error that can occur in Intel Stratix 10 designs that have MLAB RAMs driven by local clocks:

```
Internal Error: Sub-system: LCHIP,
File: /quartus/legality/lchip/lchip_rowclock_router.cpp
```

- Fixed an error that can occur in Intel Stratix 10 compilations with high RAM usage that include simple quad port memories.
- Fixed a clock routing error that can occur in some Intel Stratix 10 Partial Reconfiguration designs.
- Improved error messages for periphery placement failures that are related to conflicting location assignments.
- Fixed an issue that can cause non-deterministic results in compilation for Intel Stratix 10 designs.
- Fixed the following error that can occur Intel Stratix 10 Partial Reconfiguration compilations if all clock usage is removed from a sector following retiming or fix-up operations:

```
Internal Error: Sub-system: FITCC,
File: /quartus/fitter/fitcc/fitcc_pr_routing_network_analyzer_common.cpp,
Line: 389
```

- Fixed an issue where the Fitter, in rare circumstances, would erroneously report `Critical Warning: Detected large hold constraints`. In those circumstances, the Fitter would report a warning but later determine that it was innocuous. This change fixes the false positive in the reporting.
- Fixed a no-route (hang) issue in Intel Stratix 10 devices that can happen if you connect RAM/DSP output directly to HBM/ESRAM.
- Fixed an issue where the Fitter did not power up VCCH_GXB when IO_STANDARD 3.0V LVTTL was applied. When checking the 3VIO, the Fitter now checks for 3.0 V LVTLL.
- For Intel Stratix 10 devices, corrected invalid error messages that occurred when ATX PLL is used in non-GT mode.
- Fixed the following error by checking if IO_STANDARD exists for an I/O before retrieving the value. This fix affects HBM designs that use UIB.

```
Internal Error: Sub-system: FPP,
File: /quartus/periph/fpp/fpp_cell.cpp, Line: 655
```

Interface Planner

- Fixed a problem where Interface Planner does not work when launched from the Intel Quartus Prime GUI.

Partial Reconfiguration

- Added new error message that displays when generating Partial Reconfiguration flow scripts to indicate that script-based Partial Reconfiguration flow is no longer supported.

Platform Designer (formerly QSys)

- Fixed an issue where Platform Designer produced over-constrained timing constraints resulting in timing violations in designs that use `altera_avalon_st_handshake_clock_crosser` IP.
- Fixed missing synchronous resets in burst adapter.
- For Intel Stratix 10 devices, corrected a ready latency setting.
- Added sync reset support for additional interconnect components.

Power Analyzer

- Updated power model for Intel Stratix 10 E-Tile and L-Tile transceivers.
- Set final power model attributes for the following Intel Stratix 10 device families:
  - 1GX250L
  - 1GX280L
  - 1SX250L
  - 1SX280L
- Added support for new power attributes for power modeling.
- Added support for new Intel Arria 10 devices.
- Updated static power models for Intel Arria 10 devices.
- Updated power models for Intel Stratix 10 devices.
- Updated HPS system power model for Intel Stratix 10 devices.
- Updated clock signals power model for Intel Stratix 10 devices.
- Updated static power models for Intel Cyclone® 10 GX devices.

Programmer

- Fixed an issue where unquoted service paths could allow a local attacker to potentially execute arbitrary code.
- Fixed a JTAG device numbering issue that occurred when trying to perform JIC file programming when an Intel Stratix 10 device was already configured with the HPS Debug Access Port SDM Pins option.
- Removed the INI requirement for MT25QU02G flash support from programmer. This includes the fix for the internal error during JIC programming when the option **Unprotect EPCS/EPCQ devices selected for the erase/program operation** is enabled at the **Programmer Options** menu.

- Fixed the following string parsing error in JAM file template filtering in Windows:

```
Internal Error: Sub-system: PGMIO,
File: /quartus/pgm/pgmio/pgmio_jam.cpp, Line: 2655
```

- Fixed possible configuration bitstream corruption in multithreaded scenarios.
- Added SFL image files that were missing for the following Intel Arria 10 part numbers:
  - 10AS057K1F40E1HGJZ
  - 10AS066K1F40E1HGJZ
  - 10AX057K1F40E1HGJZ
  - 10AX066K1F40E1HGJZ

Signal Probe

- Fixed an issue that can result in the following error when using Signal Probe:

```
Internal Error: Sub-system: PTI,
File: /quartus/tsm/pti/pti_tdb_builder.cpp, Line: 4646
TIMING CHECK FAILED
```

Signal Tap

- Fixed the following error when using Postfit Signaltap:

```
RE Network failed consistency check
U2B2_RE_NETWORK_CHECKER::work(bool) const + (db_u2b2_cdb) next at
u2b2_re_network_checker.cpp:169
U2B2_CHECK_OP::work(CDB_CHIP_DB_ENTRY const*) const + (db_u2b2_core) next
at u2b2_check_op.cpp:82
FDRGN_EXPERT::do_post_finalize_ops(bool) + (fitter_fdrgn) next at
fdrgn_expert.cpp:3981
FDRGN_EXPERT::finalize() + (fitter_fdrgn) next at fdrgn_expert.cpp:1538
fit2_fit_finalize_auto + (comp_fit2) next at fit2_placement_tcl.cpp:1123
```

- Fixed an issue where temporary files used for compilation were not being cleaned up, which resulted in error messages similar to the following message:

```
Error: Unable to create project database files because the encrypted
source file cannot be located
```

- Fixed an internal error that occurred when you opened a Signal Tap file (`.stp`) that contained a state-based trigger flow control.

Synthesis

- In SystemVerilog, signed components of a user-defined type UT now properly retain their signedness when instantiating an array of UTs.

Timing Closure

- Fixed an issue that can cause hold time violation with clock signals driving ESRAM interfaces in some Intel Stratix 10 devices.

Timing Models

- Updated timing models for Intel Stratix 10 devices.
- Set timing model status to Final for the following Intel Stratix 10 L-Tile device families:
  - 1GX250L
  - 1GX280L
  - 1SX250L
  - 1SX280L
- Updated SDM timing model for Intel Stratix 10 devices.
- Increased the clock uncertainty of I/O PLLs with non-dedicated reference clock connections (from another PLL, or from a reference clock that is routed through the fabric).
- Finalized timing models for Intel Arria 10 Military parts.
- Fixed timing model issues for designs that instantiate the Intel Stratix 10 logic_module WYSIWYG.
- Added the final HPS F2SDARM timing library updates for the Intel Stratix 10 SX-family devices.
- Updated SDM timing models.

Timing Analyzer (formerly TimeQuest Timing Analyzer)

- Provided updated Synopsys Design Constraint (SDC) data for Intel Stratix 10 devices.
- Improved how Timing Analyzer identifies synchronizer instance assignments.

Transceiver Toolkit

- Improved the accuracy of bit error rate (BER) calculation method for PRBS testing Intel Stratix 10 E-Tile devices in Transceiver Toolkit.
- Added messages to help explain constraints that are associated with running calibration in parallel with pseudo-random binary sequence (PRBS) testing for Intel Stratix 10 E-Tile devices.
- Improved default NRZ Eye Sweep time for Intel Stratix 10 E-Tile devices.
- Fixed handling of PAM4 Single Width mode for Intel Stratix 10 E-Tile devices.
- Updated expected firmware revision for Intel Stratix 10 E-Tile devices to prevent invalid warning messages.

2.2. IP and IP Cores

100G Ethernet IP Core

- Enabled 100G-KR networking for Intel Stratix 10 devices.
- Enhanced I/O PLL calibration sequence to make forward error correction (FEC) more robust.
- Fixes an issue where sometimes after a reset release, PHY is not stable and PEMPTY has issue that affects `rx_pcs_ready` and causes some packets to be dropped during traffic.
- Enabled the handling of skews larger than 160 ns (64 clock cycles).

40G Ethernet IP Core

- Added 1.1 V board voltage support for Intel Stratix 10 40GE in Intel Quartus Prime. The default voltage is 1.0 V.
- Fixed an issue in the clock monitor where tx and rx clock orders were swapped.

DisplayPort IP Core

- Fixed bug where DisplayPort 1.3 RX DPCD register offset `'h2200-22FF` (Extended Receiver Capability Field) always read out as "`0`". When DPRX connected to DP1.3/1.4 GPU source, this caused link training failure as DP RX Extended Receiver Capability Register Field return "`0`".

External Memory Interface IP Core

- Fixed an issue that caused Intel Quartus Prime to crash when the Slew Rate is 0 and pre-emphasis is 0.
- For Intel Stratix 10 EMIF on-chip debug toolkit, solved an intermittent race condition after FPGA programming where the soft Nios processor would start executing invalid code and hang EMIF calibration.
- Updated some Intel Stratix 10 and Intel Arria 10 EMIF IP parameter descriptions.
- Enabled compilation of EMIF and HPS-EMIF for Intel Stratix 10

  1SG110/085 ES and 1SX110/085 ES device families.

Fractional Phase-Locked Loop (fPLL) IP Core

- Fixed an issue for Intel Stratix 10 L- and H-Tile devices where instance names containing a backslash character ("\") were handled incorrectly which led to clocks not being defined.

HDMI IP Core

- Improved timing on the long path clock signal.
- Fixed an issue to prevent register from renaming when there is name collision.
- Added support for Bitec HDMI Daughter Care Rev 11.
- For the Intel Stratix 10 design example, added soft alignment to achieve fast locking for HDMI 2.0.

High Speed Serial Interface (HSSI) IP Core

- Fixed an incremental compilation issue for Intel Stratix 10 devices when the design includes HSSI IP.

Intel Stratix 10 Hard IP for Ethernet IP Core

- For Intel Stratix 10 E-Tile devices, fixed the following ELANE issues:
  - ELANE PTP 10G/25G design faced a problem when RX XCVR Interface is released after EHIP RX. The reset controller is updated, transceiver RX interface is released before EHIP RX.
  - The ELANE RX RSFEC reset is stuck.
- Fixed the following issues:
  - Fixed an issue with RSFEC rx reset where rx reset was not working as expected when RSFEC is enabled and the link was not coming up after applying `i_rx_rst_n` or `soft_rx_rst` (CSR bit).
  - Fixed an issue affecting the RX side where `o_rx_pcs_ready` was affected when only `i_tx_rst_n` or `soft_tx_reset` was applied.
  - Fixed an issue where RX - PCS does not regain a lock and `o_rx_pcs_ready` never goes "1" when `tx_rst_n`/`soft_tx_rst` and `rx_rst_n`/`soft_tx_rst` when TX and RX resets are applied at the same time.
- Updated the Ethernet 10/25G hardware example design to be similar and consistent with other Ethernet hardware example designs.
- Made the following changes to support Intel Stratix 10 E-Tile devices:
  - Added 156.25 MHz refclk support for 10G/25G
  - Fixed TX timestamp >1 second accuracy error
  - Added to change to assert `o_sl_tx_ready` signal only when TX gearbox realignment is completed and stable
  - Fixed CSR soft reset
  - Improved timing performance
  - Added `i_sl_aib_rxfifo_rd_en` port for PMA direct mode
- Fixed a bug in the Intel Stratix 10 100GE hardware example design for RS-FEC mode.
- Enabled support for 4-channel 25G+PTP+RSFEC variant on Intel Stratix 10 E-Tile devices.

Intel Stratix 10 E-Tile Transceiver Native PHY IP Core

- Changed default settings for the following parameters:
  - Transceiver Configuration Rules: from PMA direct to PMA direct high data rate PAM4
  - Enable TX double width transfer: from 0 to 1
  - Enable RX double width transfer: from 0 to 1
  - TX PMA Interface width: from 16 to 64
  - RX PMA Interface width: from 16 to 64
  - TX PMA modulation type: from NRZ to PAM4
  - RX PMA modulation type: from NRZ to PAM4
  - Selected `tx_clkout` clock source: from full-rate to half-rate
  - Selected `rx_clkout` clock source: from full-rate to half-rate
  - TX Core Interface FIFO partially full threshold: from 5 to 10
  - RX Core Interface FIFO partially full threshold: from 5 to 10
- Enabled instantiation of an ELANE design with a topology that does not include RSFEC, but permits configuration later to turn RSFEC on.
- Due to bit setting changes, you must upgrade this IP core. Upgrading is not optional.
- Corrected an issue that prevented `set_max_skew` from working as expected. Also, corrected an issue where only specific clocks were used as the targets to set_false_path for the asynchronous resets (to adapter and xcvrif). Now, all source and targets are covered.

Intel Stratix 10 PCIe Hard IP Core

- Fixed an issue where certain BAR sizes set by the user were overwritten with a default BAR size during the example design generation flow.
- Fixed an issue that prevented example PCIe G3x16 design generations using the BAR address width set in the GUI.
- Corrected synthesis warnings related to `generate block`.
- Enabled the GUI control of the loopback master enable feature for the root port.
- Added additional calibration port to the IOPLL instantiated in the 64-bit Avalon -MM Intel Stratix 10 Hard IP+ for PCI Express.
- Fixed an issue in the 64-bit Avalon -MM Intel Stratix 10 Hard IP+ for PCI Express where TLP packets were processed incorrectly.
- Fixed an issue where the Gen3 x18 Avalon-ST example design hangs in simulation.
- Fixed an issue with multifunction-related parameters in the Gen3 x18 Avalon -MM Intel Stratix 10 Hard IP+ for PCI Express.
- Fixed an issue that could cause missing ports in Avalon-MM interfaces when you upgrade the IP core.

Interlaken IP Core

- Added support for Intel Stratix 10 E-Tile devices.
- Fixed an issue that caused incorrect packet count when using the `loop_on` (internal loopback) command.

I/O Phase-Locked Loop (IOPLL) IP Core

- Improved the usability of the Intel Stratix 10 calibration process for I/O PLLs.
- Enabled specifying IOPLL Reconfig IP MIF file location using a relative path, and added the option to create new copy of the MIF file during IP generation.
- Updated the IOPLL frequency legality checks to match values in the Intel Stratix 10 datasheet.
- Updated IOPLL IP core to make the 40G Ethernet IP core more robust.
- Fixed an issue to correctly set the IOPLL compensation mode during an IOPLL IP upgrade.

IP for Multi-Rate Ethernet PHY function (formerly 1G/2.5G/5G/10G Multi-Rate Ethernet PHY MegaCore Function)

- Corrected an IEEE 1588 timestamp inaccuracy issue.

PCIe IP Core

- Fixed an issue that caused failures for smaller DW transactions with the write data mover.
- Fixed an issue that occurred when MaxRead Request Size (MRRS) is set to 128 bytes. A large read burst at an address that is not a multiple of 128 causes 5 MRd TLPs to be created at once. If this happens when the number of outstanding read request is close to the allowed maximum, the counter keeping track of the number of available tags can underflow.
- Fixed an issue where the I/O PLL in the Gen3x16 PCIe IP core faced issues with locking.
- Fixed an issue where incorrect data might be returned on the `readdata` bus when the IP core receives the completions for two different MRd requests using the same tag with no other completion with different tags received between them.
- Fixed an issue where completions for MRd requests issued by the Read Data Mover and the Bursting Avalon-MM Slave modules can get corrupted when they are received interleaved with each other.
- Added Intel Arria 10 Root Port example design `.qsys` files. These files can be used to run static regression.
- Fixed an issue with the G3x16 Avalon-MM DMA example.
- Fixed an issue where, when the Bursting Master (BAM) received a mix of short and long burst read TLPs., the completion TLPs could contain data with X values causing the PCIe link to enter Recovery state.

- Fixed a PCIe DMA simulation issue where the address is driven with unknown values (Xs).
- Set `VISIBLE=false` for the `enable_sriov_hwtcl` in parameters `hwtcl`, and added new GUI tabs containing new parameters (`pf*_sriov_vf_device_id_hwtcl`), and associated mappings to HDL parameters (`pf*_sriov_vf_device_id`).
- Fixed a missing MSI control bus for Intel Arria 10 Avalaon-MM interfaces.

PHY Lite for Parallel Interfaces IP Core

- For the PHY Lite for Parallel Interfaces for Intel Stratix 10 FPGA IP, corrected a typo in an instance name used for the Tile Ctrl block (atom).
- For the PHY Lite for Parallel Interfaces for Intel Arria 10 FPGA IP and the PHY Lite for Parallel Interfaces for Intel Cyclone 10 FPGA IP, updated the PLL division factor to align with EMIF IP rules.

Serial Data Interface (SDI) IP Core

- Removed the global assignment of preserving unused transceiver channels for Intel Arria 10 and Intel Cyclone 10 design examples that have a Tx-Rx physical pair with only Rx used due to an Rx simplex calibration issue. Set the preserved unused transceiver channels assignment to all unused Rx pins only.

Turbo IP Core

- Reduced use of M20K memory blocks when implementing LTE turbo decoders.

Video and Image Processing Suite IP Cores

- Fixed an issue in the Deinterlacer II IP core where in Motion Adaptive configurations (excluding Video Over Film configurations), suboptimal motion tracking was exhibited, which resulted in weave artifacts appearing in video sequences with different motion over different parts of the frame.

2.4. DSP Builder for Intel FPGAs

- Added example design associated the new HDL Import (beta) functionality that is documented in the *DSP Builder Advanced Blockset handbook*.
- For Intel Stratix 10 devices, added option to allow you to choose to generate individual 18-bit multipliers as RTL, which allows Intel Quartus Prime to place two 18-bit multipliers in a single DSP block instead of having one 18-bit mulitplier consume the entire DSP block.
- Fixed an issue where the DSP Builder command `SystemConsole.refreshMasters` failed to detect any master connections.

- Fixed an issue where the creation of fully-parallel FFTs with 512 (or more) wires failed because the graphical coordinates of an internal block exceed the maximum values permitted by Simulink.
- Fixed a functional issue where incorrect RTL was generated for SharedMems greater than 2K deep that are targeted to Intel Stratix 10 devices. The issue manifested as a data mismatch of 1 cycle, for example when running a simulation via the automated testbench for the design. However, the issue was not limited to being a simulation failure but would also cause incorrect system behavior.
- Fixed an issue where not all enables were correctly identified, leading to some logic undergoing reset-minimization inappropriately. This inappropriate reset-minimization might have lead to spurious enables driving logic during the reset period. In particular, initialized and writable memories might have experienced a spurious write-enable which might have led to corruption of the memory data.

2.5. Intel High Level Synthesis Compiler

- Reduced the compilation time for some Intel HLS Compiler designs that contain loops that do not contain memory accesses or that do not contain load-stores.

2.6. Intel FPGA SDK for OpenCL

- Fixed an issue where some kernels with names longer than 65 characters failed to compile.
- Reduced the compilation time for some OpenCL* designs that contain loops that do not contain memory accesses or that do not contain load-stores.
- Improved speed of `clEnqueueTask()`.
- Fixed an issue related to creating contexts on different threads.
- Fixed some limitations and issues with the `aocl install` and `aocl uninstall` commands:
  - FPGA client driver (FCD) and update of installed packages occur even when the BSP does not provide an installation script. You must then run the `aocl install` command after setting up your board, even when the BSP installs the board driver through means other than the `aocl install` command.
  - The `aocl uninstall` command removes the FCD file.
  - ARM-only: When the FCD is installed, the correct flags are printed by using the `aocl link-config` command.
- Fixed a problem where certain ECC status signals were not connected and reported to users.
- Fixed a problem with the QHD flow. Atom modifications occur only when an atom is modifiable.
- Improved the compilation time for an optimization analysis for very large programs with many loops.
- Fixed segmentation fault that occurred when in the on systems with multiple Intel Programmable Acceleration Card (PAC) with Intel Arria 10 GX FPGA cards.

3. Software Issues Resolved

Table 1. Customer Service Requests Resolved in Intel Quartus Prime Design Suite Version 18.0 Update 1

Customer Service Request Numbers Resolved					
11337784	11378339	11382327	11388730	11389333	11393981
11394545	11394664	11400743	11403198	11403422	11403693
11404005	11409757				

4. Software Patches Included in Update Releases

Table 2. Intel Quartus Prime Pro Edition Software Patches included in Intel Quartus Prime Design Suite Version 18.0 Update 1

Software Version	Patch	Customer Service Request Number
Quartus II V11.0- V15.0 Intel Quartus Prime V15.1- V18.0	Intel SA-00151	
Intel Quartus Prime V18.0	0.24	
Intel Quartus Prime V18.0	0.23	
Intel Quartus Prime V18.0	0.22	
Intel Quartus Prime V18.0	0.16	
Intel Quartus Prime V18.0	0.14	
Intel Quartus Prime V18.0	0.13	
Intel Quartus Prime V18.0	0.12	
Intel Quartus Prime V18.0	0.10	
Intel Quartus Prime V18.0	0.08p	
Intel Quartus Prime V18.0	0.08	
Intel Quartus Prime V18.0	0.07	11345294
Intel Quartus Prime V18.0	0.05	11394545
Intel Quartus Prime V18.0	0.02	
Intel Quartus Prime V17.1.1	1.33	11389010
Intel Quartus Prime V17.1.1	1.31	
Intel Quartus Prime V17.1	0.27	11393981
Intel FPGA SDK for OpenCL V18.0	0.20rte	
Intel FPGA SDK for OpenCL V18.0	0.20	
Intel FPGA SDK for OpenCL V17.1.1	1.31	
Intel FPGA SDK for OpenCL V17.1.1	1.30	
Intel FPGA SDK for OpenCL V17.1.1	1.28	
Intel FPGA SDK for OpenCL V17.1	0.29	

5. Known Issues and Workarounds

Known Issues and Workarounds for Intel Quartus Prime Pro Edition Version 18.0 Update 1

Table 3.

Description	Workaround
When the Signal Tap IP is instantiated in the RTL design, the generated `.stp` file does not match the instance correctly if any input port is not connected or connected to either VCC or GND. When you use the `.stp` file, you get an incorrect waveform display or the data at the trigger position does not match the trigger condition defined.	Recompile the project in full. Finally, regenerate the correct `.stp` file with either the GUI menu or the command `quartus_stp <project name> -c <revision name> --create_signaltap_hdl_file --stp_file=<filename>`.

For information about other known software issues, visit the Intel FPGA Knowledge Base.

Related Information

- Intel FPGA Knowledge Database
- Intel FPGA Documentation: Release Notes
- Intel Quartus Prime and Quartus II Software Support

A. Document Revision History for Intel Quartus Prime Design Suite Update Release Notes

Document Version	Intel Quartus Prime Version	Changes
2018.07.02	18.0.1	• Initial release with Intel Quartus Prime Design Suite version 18.0 update 1 information.