4. Hot Socketing & Power-On Reset

Introduction

Cyclone® II devices offer hot socketing (also known as hot plug-in, hot insertion, or hot swap) and power sequencing support without the use of any external devices. You can insert or remove a Cyclone II board in a system during system operation without causing undesirable effects to the board or to the running system bus.

The hot-socketing feature lessens the board design difficulty when using Cyclone II devices on printed circuit boards (PCBs) that also contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices. With the Cyclone II hot-socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Cyclone II hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also discusses the power-on reset (POR) circuitry in Cyclone II devices. The POR circuitry keeps the devices in the reset state until the $V_{CC}$ is within operating range.

Cyclone II Hot-Socketing Specifications

Cyclone II devices offer hot-socketing capability with all three features listed above without any external components or special design requirements. The hot-socketing feature in Cyclone II devices offers the following:

- The device can be driven before power-up without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
Cyclone II Hot-Socketing Specifications

Devices Can Be Driven before Power-Up

You can drive signals into the I/O pins, dedicated input pins, and dedicated clock pins of Cyclone II devices before or during power-up or power-down without damaging the device. Cyclone II devices support any power-up or power-down sequence (VCCIO and VCCINT) to simplify system level design.

I/O Pins Remain Tri-Stated during Power-Up

A device that does not support hot socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot-socketing situation, the Cyclone II device’s output buffers are turned off during system power-up or power-down. The Cyclone II device also does not drive out until the device is configured and has attained proper operating conditions. The I/O pins are tri-stated until the device enters user mode with a weak pull-up resistor (R) to 3.3V. Refer to Figure 4–1 for more information.

You can power up or power down the VCCIO and VCCINT pins in any sequence. The VCCIO and VCCINT must have monotonic rise to their steady state levels. (Refer to Figure 4–3 for more information.) The power supply ramp rates can range from 100 µs to 100 ms for non “A” devices. Both VCC supplies must power down within 100 ms of each other to prevent I/O pins from driving out. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF. Cyclone II devices meet the following hot-socketing specification.

- The hot-socketing DC specification is |I_IOPIN| < 300 µA.
- The hot-socketing AC specification is |I_IOPIN| < 8 mA for 10 ns or less.

This specification takes into account the pin capacitance but not board trace and external loading capacitance. You must consider additional capacitance for trace, connector, and loading separately.

I_IOPIN is the current at any user I/O pin on the device. The DC specification applies when all VCC supplies to the device are stable in the powered-up or powered-down conditions. For the AC specification, the peak current duration due to power-up transients is 10 ns or less.

A possible concern for semiconductor devices in general regarding hot socketing is the potential for latch-up. Latch-up can occur when electrical subsystems are hot socketed into an active system. During hot socketing, the signal pins may be connected and driven by the active system before
the power supply can provide current to the device’s $V_{CC}$ and ground planes. This condition can lead to latch-up and cause a low-impedance path from $V_{CC}$ to ground within the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

Altera has ensured by design of the I/O buffers and hot-socketing circuitry, that Cyclone II devices are immune to latch-up during hot socketing.

Hot-Socketing Feature Implementation in Cyclone II Devices

The hot-socketing feature turns off the output buffer during power up (either $V_{CCINT}$ or $V_{CCIO}$ supplies) or power down. The hot-socket circuit generates an internal $HOTSCKT$ signal when either $V_{CCINT}$ or $V_{CCIO}$ is below the threshold voltage. Designs cannot use the $HOTSCKT$ signal for other purposes. The $HOTSCKT$ signal cuts off the output buffer to ensure that no DC current (except for weak pull-up leakage current) leaks through the pin. When $V_{CC}$ ramps up slowly, $V_{CC}$ is still relatively low even after the internal $POR$ signal (not available to the FPGA fabric used by customer designs) is released and the configuration is finished. The $CONF\_DONE$, $nCEO$, and $nSTATUS$ pins fail to respond, as the output buffer cannot drive out because the hot-socketing circuitry keeps the I/O pins tristated at this low $V_{CC}$ voltage. Therefore, the hot-socketing circuit has been removed on these configuration output or bidirectional pins to ensure that they are able to operate during configuration. These pins are expected to drive out during power-up and power-down sequences.

Each I/O pin has the circuitry shown in Figure 4–1.
The POR circuit monitors $V_{CCINT}$ voltage level and keeps I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) from the I/O pin to $V_{CCIO}$ keeps the I/O pins from floating. The voltage tolerance control circuit permits the I/O pins to be driven by 3.3 V before $V_{CCIO}$ and/or $V_{CCINT}$ are powered, and it prevents the I/O pins from driving out when the device is not in user mode.

For more information, see the *DC Characteristics & Timing Specifications* chapter in Volume 1 of the *Cyclone II Device Handbook* for the value of the internal weak pull-up resistors.

*Figure 4–2* shows a transistor level cross section of the Cyclone II device I/O buffers. This design ensures that the output buffers do not drive when $V_{CCIO}$ is powered before $V_{CCINT}$ or if the I/O pad voltage is higher than $V_{CCIO}$. This also applies for sudden voltage spikes during hot socketing. The $V_{PAD}$ leakage current charges the voltage tolerance control circuit capacitance.
Power-On Reset Circuitry

Cyclone II devices contain POR circuitry to keep the device in a reset state until the power supply voltage levels have stabilized during power-up. The POR circuit monitors the $V_{CCINT}$ voltage levels and tri-states all user I/O pins until the $V_{CC}$ reaches the recommended operating levels. In addition, the POR circuitry also monitors the $V_{CCIO}$ level of the two I/O banks that contains configuration pins (I/O banks 1 and 3 for EP2C5 and EP2C8, I/O banks 2 and 6 for EP2C15A, EP2C20, EP2C35, EP2C50, and EP2C70) and tri-states all user I/O pins until the $V_{CC}$ reaches the recommended operating levels.

After the Cyclone II device enters user mode, the POR circuit continues to monitor the $V_{CCINT}$ voltage level so that a brown-out condition during user mode can be detected. If the $V_{CCINT}$ voltage sags below the POR trip point during user mode, the POR circuit resets the device. If the $V_{CCIO}$ voltage sags during user mode, the POR circuit does not reset the device.

"Wake-up" Time for Cyclone II Devices

In some applications, it may be necessary for a device to wake up very quickly in order to begin operation. The Cyclone II device family offers the Fast-On feature to support fast wake-up time applications. Devices that support the Fast-On feature are designated with an “A” in the ordering code and have stricter power up requirements compared to non-A devices.
For Cyclone II devices, wake-up time consists of power-up, POR, configuration, and initialization. The device must properly go through all four stages to configure correctly and begin operation. You can calculate wake-up time using the following equation:

\[ \text{Wake-Up Time} = V_{CC} \text{ Ramp Time} + \text{POR Time} + \text{Configuration Time} + \text{Initialization Time} \]

Figure 4–3 illustrates the components of wake up time.

**Figure 4–3. Cyclone II Wake-Up Time**

Note to Figure 4–3:
1. \( V_{CC} \) ramp must be monotonic.

The \( V_{CC} \) ramp time and POR time will depend on the device characteristics and the power supply used in your system. The fast-on devices require a maximum \( V_{CC} \) ramp time of 2 ms and have a maximum POR time of 12 ms.

Configuration time will depend on the configuration mode chosen and the configuration file size. You can calculate configuration time by multiplying the number of bits in the configuration file with the period of the configuration clock. For fast configuration times, you should use Passive Serial (PS) configuration mode with maximum DCLK frequency of 100 MHz. In addition, you can use compression to reduce the configuration file size and speed up the configuration time. The \( t_{CD2UM} \) or \( t_{CD2UMC} \) parameters will determine the initialization time.

For more information on the \( t_{CD2UM} \) or \( t_{CD2UMC} \) parameters, refer to the Configuring Cyclone II Devices chapter in the Cyclone II Device Handbook.
If you cannot meet the maximum $V_{CC}$ ramp time requirement, you must use an external component to hold $n\text{CONFIG}$ low until the power supplies have reached their minimum recommend operating levels. Otherwise, the device may not properly configure and enter user mode.

**Conclusion**

Cyclone II devices are hot socketable and support all power-up and power-down sequences with the one requirement that $V_{CCIO}$ and $V_{CCINT}$ be powered up and down within 100 ms of each other to keep the I/O pins from driving out. Cyclone II devices do not require any external devices for hot socketing and power sequencing.

**Document Revision History**

Table 4–1 shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date &amp; Document Version</th>
<th>Changes Made</th>
<th>Summary of Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>February 2007 v3.1</td>
<td>Added document revision history.</td>
<td>Specified $V_{CCIO}$ and $V_{CCINT}$ supplies must be GND when &quot;not powered&quot;.</td>
</tr>
<tr>
<td></td>
<td>Updated “I/O Pins Remain Tri-Stated during Power-Up” section.</td>
<td>Added clarification about input-tristate behavior.</td>
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<tr>
<td></td>
<td>Updated “Power-On Reset Circuitry” section.</td>
<td>Added information on $V_{CC}$ monotonic ramp.</td>
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<tr>
<td></td>
<td>Added footnote to Figure 4–3.</td>
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<tr>
<td>July 2005 v2.0</td>
<td>Updated technical content throughout.</td>
<td></td>
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<tr>
<td>February 2005 v1.1</td>
<td>Removed ESD section.</td>
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<tr>
<td>June 2004 v1.0</td>
<td>Added document to the Cyclone II Device Handbook.</td>
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