BSDL FAQs

1. **How does Altera verify boundary-scan description language (BSDL) files?**
   Altera BSDL files are verified with industry-standard syntax check from third-party tool such as JTAG Technologies, Goepel Electronic, ASSET InterTech – Agilent Technologies, Corelis and Temento Systems. Altera also performs a hardware test to verify the BSDL files.

2. **Application Note 39 only explains boundary-scan testing for older device families such as MAX®, Stratix™, Stratix GX and Cyclone™ devices. What about newer devices such as MAX II, Stratix II, Stratix II GX, Cyclone II and later?**
   One chapter on IEEE1149.1 (JTAG) BST is included in the device handbook for the newer device family. This applies for all the future Altera device families that support the standard.

3. **What is IEEE 1149.1 standard?**
   This standard defines test logic that can be included in an integrated circuit to provide standardized approaches to
   - Testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate
   - Testing the integrated circuit itself
   - Observing or modifying circuit activity during the component's normal operation

   The test logic consists of a boundary-scan register and other building blocks and is accessed through a Test Access Port (TAP).

4. **What is IEEE 1532 standard?**
   IEEE 1532 describes a series of mandatory and optional boundary-scan instructions and associated data registers that will define a standard methodology for accessing and configuring programmable devices that already support IEEE 1149.1.

5. **What Altera devices support the IEEE 1149.6 standard?**
   Refer to the link for the supported device families for this standard. This standard is only supported on the high-speed serial interface (HSSI) transceivers in Altera devices.
   http://www.altera.com/download/board-layout-test/bsdl/11496/bsd-11496.html

6. **What Altera devices support the IEEE 1532 standard?**
   MAX V, MAX II, MAX 3000, MAX 7000 and Enhance Configuration Device (EPC) families.

7. **What files do I need for IEEE 1532 programming?**
   You need the IEEE 1532 BSDL file from the Altera website and the ISC file generated by Quartus II software (except for EPC devices).

8. **How do I generate ISC file for EPC devices?**
   Download the svf2isc.tcl script from Altera's website. The User Guide that comes together with the tool command language (TCL) script explains the steps to generate the ISC file using the script.

9. **Should I pull nCONFIG low during boundary-scan test?**
   For pre-configured device, Altera recommends pulling nCONFIG to low to ensure the flash memory is reset. After configuration, you should drive to high.

	Pre-configuration	Post-configuration
nCONFIG Pin	Low	High

10. **How do I use Altera's BSDL files?**
    Refer to Application Note 39 for older device families (such as MAX, Stratix, Stratix GX and Cyclone devices). For other newer devices, refer to chapter IEEE 1149.1 (JTAG) Boundary-Scan Testing chapter in the device family handbook.

11. **Do Altera's BSDL files support post-configuration boundary-scan test?**
    Altera's BSDLCustomizer converts pre-configuration BSDL files (downloadable from Altera website) to post-configuration BSDL files. This tool and its User Guide are available for download from
    http://www.altera.com/support/devices/bsdl/bsdl.html
    Altera's BSDLCustomizer is only applicable for device families stated table below.

Device Type	Device Family
Configuration Devices	EPC
CPLDs	MAX 3000, MAX 7000, MAX II
FPGA	Stratix, Stratix GX, Stratix II, Stratix II GX, Stratix III Arria GX, Cyclone, Cyclone II, Cyclone III
ASICs	HardCopy, HardCopy II

    For newer device families that not listed above, the post-configuration BSDL file can be generated in Quartus® II design software version 8.0 and later. Refer to the BSDL File Generation II QII guideline to generate the post-configuration BSDL file.

12. **How do I use the BSDLCustomizer?**
    Refer to the BSDLCustomizer User Guide downloadable from
    http://www.altera.com/support/devices/bsdl/bsdl.html

13. **How do I modify the BSDL files**?
    Refer to the BSDLCustomizer User Guide downloadable from
    http://www.altera.com/support/devices/bsdl/bsdl.html

14. **How do I modify the BSDL file to test LVDS/ differential pins?**
    Refer to the BSDLCustomizer User Guide downloadable from http://www.altera.com/support/devices/bsdl/bsdl.html

15. **Device failed JTAG test using Altera's BSDL file. What can I do before seeking Altera's technical assistance?**
    Please refer to Basic Boundary-Scan Test Troubleshooting Guideline.

16. **MAX devices (MAX7000 and MAX3000) failed post-configuration JTAG boundary-scan test even when the BSDL files are modified using BSDLCustomizer.**
    a. Ensure MAX devices are enabled for JTAG BST support in Quartus II software. Go to Quartus II Assignments>Settings and click on Device & Pin Options, then check "Enable JTAG BST support" under General.
    b. Refer answer for question (15)

17. **JTAG test failed on EXTEST. What can I do to debug?**
    a. Ensure SAMPLE/PRELOAD instruction is done before EXTEST
    b. Refer answer for question (15)

18. **What happens if I drive out a signal on an input pin or vice-versa?**
    Boundary-scan test will fail because an input pin would have its output buffer disabled and output pin would have its input buffer disable. Hence, the value driving in/out will not be able to be detected correctly.

19. **Why are the ASDO and nCSO pins specified as dedicated output pins in certain BSDL files? Can these two pins be specified as I/O pins instead?**
    ASDO and nCSO are specified as output pins in the BSDL files because both the pins are dedicated output pin when the MSEL are connected to set the device in active serial programming.

    If you are using the device in other programming mode, ASDO and nCSO can be used as normal I/O pins. In this case, you can change the BSDL file to specify the ASDO and nCSO pins as I/O pins.

20. **How do I generate the BSDL file for my HardCopy® II device?**
    Download the generic HardCopy II BSDL file from Altera website and use the BSDLcustomizer tool to convert the generic HardCopy II BSDL file to the specific BSDL file for your HardCopy II.

Revision History

Revision	Date	Description of Change
1.01	05/31/2007	-Include revision history -Rename the document to FAQs -Refer user to Basic Boundary-Scan Test Troubleshooting Guideline for question 15.
1.02	07/16/2012	-Update IEEE 1149.6 question -Update post-configuration BSDL file generation question