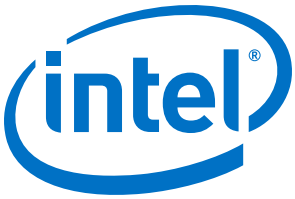

FPGA Interface Manager Data Sheet

Intel FPGA Programmable Acceleration Card D5005

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Contents

1. FPGA Interface Manager Data Sheet for Intel FPGA Programmable Acceleration Card D5005

1.1. Overview

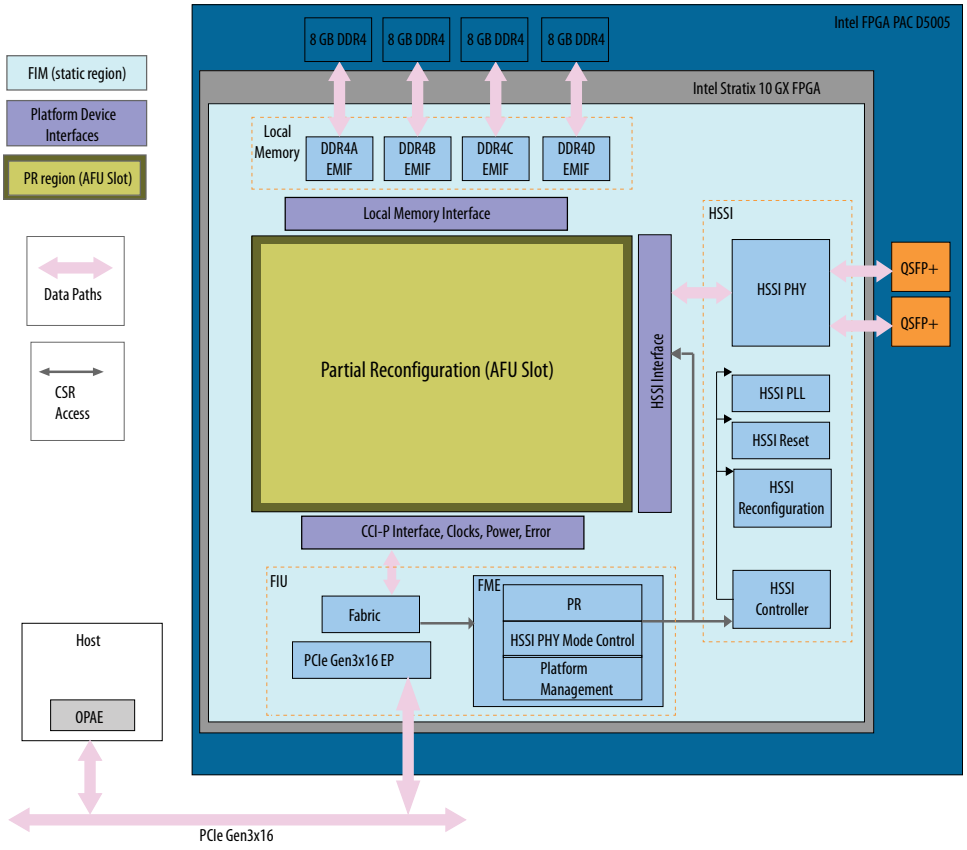
The FPGA Interface Manager (FIM) data sheet provides the key parameters to which you must design your Accelerator Functional Unit (AFU).

The FIM consists of the following:

- FPGA Interface Unit (FIU): The platform interface layer that acts as a bridge between PCIe* and Core Cache Interface (CCI-P).
- Core Cache Interface (CCI-P): standard interface AFUs use to communicate with the host.
- External Memory Interface (EMIF)
- High-Speed Serial Interface (HSSI) for external transceivers

Each of these components have parameter values that must be met by the AFU.

Figure 1. Intel® FPGA PAC D5005



1.2. FIM and AFU Parameter Data

Use the following tables in conjunction with the *Accelerator Functional Unit (AFU) Developer's Guide* and the *Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs Core Cache Interface (CCI-P) Reference Manual* to complete your AFU design.

Related Information

- Accelerator Functional Unit (AFU) Developer's Guide
- Intel Acceleration Stack for Intel Xeon CPU with FPGAs Core Cache Interface (CCI-P) Reference Manual

1.2.1. Memory Interface

Table 1. Local Memory Interface Specifications

Parameter	Value	Notes
Memory Protocol	DDR4-SDRAM	-
AFU Interface Type	Avalon® Memory Mapped Interface (Avalon-MM)	-
Number of Memory Interfaces	4	-

continued...

Parameter	Value	Notes
Density per Memory Interface	8 GB	-
AFU-Accessible Memory Address Bus Width	27-bit	-
AFU-accessible memory Data Width	512-bit	-
DDR Data Width	72-bits (64-data bits + 8 ECC bits)	-
DDR Frequency	1200 MHz maximum	-
Frequency	300 MHz	AFU memory clock frequency.
Maximum Burst Size	128 beats	-

1.2.1.1. SDRAM Signals

This table defines the interface for each of the four DDR4 memories from the viewpoint of the AFU.

Table 2. SDRAM Interface

Signal Name	Direction (AFU viewpoint)	Width	Description
`clk`	input	1	Provides synchronization fo internal logic.
`waitrequest`	input	1	Asserts when AFU is unable to respond to a read or write request.
`readdata`	input	512	Read data sent from AFU to host.
`readdatavalid`	input	1	Used for variable-latency, pipelined read transfers. When asserted, indicates that the `readdata` signal contains valid data.
`burstcount`	output	7	Used to indicate the number of transfers in each burst.
`writedata`	output	512	Asserted to indicate a write transfer.
`address`	output	27	By default, the interconnect translates the byte address into a word address in the slave's address space. From the perspective of the slave, each slave access is for a word of data.
`write`	output	1	Asserted to indicate a write transfer.
`read`	output	1	Asserted to indicate a read transfer.
`byteenable`	output	64	Enables one or more specific byte lanes during transfers on interfaces of width greater than 8 bits. Each bit in byteenable corresponds to a byte in writedata and readdata.

1.2.2. Core Cache Interface (CCI-P) Interface

Table 3. Core Cache Interface (CCI-P) Specifications

Parameter	Value	Notes
Width	512-bit	CCI-P interface width.
Maximum CCI-P Frequency	pClk	-
Host Memory Cache-Line Size	64-byte	-
MMIO access width	32-bit and 64-bit	64-bit accesses are mandatory for Device Feature Header (DFH) enumeration.
MMIO Read Response Timeout	65536 clock cycles	-
Virtual Channels Supported	VH0, VA	Accesses to VH0 and VA are mapped to the PCIe link. Accesses to VH1 or VL0 are mapped to VH0.

Related Information

Intel Acceleration Stack for Intel Xeon CPU with FPGAs Core Cache Interface (CCI-P) Reference Manual

1.2.3. Clocks

Table 4. Clock Specifications

Parameter	Value	Notes
pClk	250 MHz	Primary interface clock. All CCI-P interface signals are synchronous to this clock.
pClkDiv2	125 MHz	Synchronous and in phase with pClk. 0.5x the pClk clock frequency.
pClkDiv4	62.5 MHz	Synchronous and in phase with pClk. 0.25x the pClk clock frequency.
uClk_usr Min	10 MHz	Minimum user-defined clock. This clock is not synchronous with the pClk. You can adjust this clock using OPAE.
uClk_usr Default	312.5 MHz	Default user-defined clock. This clock is not synchronous with the pClk. You can adjust this clock using OPAE.
uClk_usr Max	600 MHz	Minimum user-defined clock. This clock is not synchronous with the pClk. You can adjust this clock using OPAE.
uClk_usrDiv2 Min	10 MHz	Minimum user defined clock that is synchronous with uClk_usr and 0.5x the frequency. *Note:* You can use OPAE to set the frequency to a value that is not synchronous with the uClk_usr.
uClk_usrDiv2 Default	156.25 MHz	User defined clock that is synchronous with uClk_usr and 0.5x the frequency. *Note:* You can use OPAE to set the frequency to a value that is not synchronous with the uClk_usr.
uClk_usrDiv2 Max	600 MHz	Maximum user defined clock that is synchronous with uClk_usr and 0.5x the frequency.

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Parameter	Value	Notes
		Note: You can use OPAE to set the frequency to a value that is not synchronous with the `uClk_usr`.

1.2.4. Reset

Table 5. Reset Specifications

Subsystem	Parameter	Value	Notes
Resets	Min Reset Width	512 `pClk` cycles	Minimum number of `pClk` clock cycles the FIM holds the AFU in reset.

Related Information

Clocks on page 6

1.2.5. Networking Interface

Table 6. Network Interface Specifications

Parameter	Value	Notes
Rate Supported	8x10GbE	-
Layers Supported	PHY	Physical Coding Sublayer (PCS) + Physical Medium Attachment (PMA) Sublayer

For more information about the Networking Interface for the Intel FPGA PAC D5005, please contact your Intel support representative to obtain the *Networking Interface for Open Programmable Acceleration Engine User Guide*.

1.2.5.1. Clock Signals

The clocks of the PR HSSI Interface synchronize the unified data interface between the MAC IP and the HSSI PHY. The signal directions listed for HSSI ports are from the perspective of the FIM. The signals listed below are identical for both QSFP28 interfaces.

Table 7. Clock Signals

Port Name	Width	Direction	Description
`f2a_tx_clkout`	4	Output	Reserved.
`f2a_tx_parallel_clk_x1`	4	Output	The fPLL generates a 156.25MHz in the HSSI PHY from a 644.53125MHz QSFP28 external reference clock. Only `f2a_tx_parallel_clk_x1[0]` is used, while `f2a_tx_parallel_clk_x1[3:1]` are reserved. The `f2a_tx_parallel_clk_x1` and `f2a_rx_parallel_clk_x1` are identical clocks driven by the same source, which also drives the `rx_coreclkin` and `tx_coreclkin` inputs of all 4 channels of the Native PHY IP cores. All transmit data from the MAC to the HSSI PHY is synchronous to `f2a_tx_parallel_clk_x1[0]` and `f2a_rx_parallel_clk_x1[0]`.

continued...

Port Name	Width	Direction	Description
			All receive data to the MAC from the HSSI PHY is synchronous to f2a_tx_parallel_clk_x1[0] and f2a_rx_parallel_clk_x1[0].
f2a_tx_parallel_clk_x2	4	Output	The fPLL generates a 312.5MHz in the HSSI PHY from a 644.53125MHz QSFP28 external reference clock. Only f2a_tx_parallel_clk_x2[0] is used, while f2a_tx_parallel_clk_x2[3:1] are reserved. The f2a_tx_parallel_clk_x2 and f2a_rx_parallel_clk_x2 are identical clocks driven by the same source.
f2a_rx_clkout	4	Output	Reserved.
f2a_rx_parallel_clk_x1	4	Output	Same signal as f2a_tx_parallel_clk_x1.
f2a_rx_parallel_clk_x2	4	Output	Same signal as f2a_tx_parallel_clk_x2.

1.2.5.2. Data Interface and Signals

The HSSI unified data interface conforms to the Intel Stratix® 10 FPGA Transceiver Native PHY IP core with enhanced PCS in 10GBase-R mode. It consists of generic parallel data and encoding control interfaces for transmit and receive that are mapped to specific signaling behavior as outlined in the *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*. The unified data interface also includes flow control ports to manage passing data to and from the HSSI PHY interface.

The table below provides a cross reference from the hssi:raw_pr unified data interface signals to the Intel Stratix 10 FPGA Transceiver Native PHY IP core with enhanced PCS signal set. The HSSI PHY IP is configured in Configuration-3, PMA width-32, FPGA Fabric width-66, making the gearbox ratio 32:66. The TX Core FIFO is configured in Phase Compensation mode. The RX Core FIFO is configured in 10GBase-R mode. The Simplified Data Interface is disabled. The Double-Rate Transfer is disabled. For detailed information on these signals, refer to the PCS-Core Interface Ports: Enhanced PCS.

Table 8. Data Signals

Port Name	Width	Direction	Clock Domain	Native PHY IP Port Name
Transmit and Receive Data and Encoding Control Ports				
a2f_tx_parallel_data	4*80	Input	f2a_tx_parallel_clk_x1[0]	tx_parallel_data
f2a_rx_parallel_data	4*80	Output	f2a_rx_parallel_clk_x1[0]	rx_parallel_data
Flow Control Ports				
f2a_tx_fifo_empty	4	Output	Reserved	
f2a_tx_fifo_full	4	Output	Reserved	
f2a_tx_fifo_pempty	4	Output	Reserved	
f2a_tx_fifo_pfull	4	Output	Reserved	
a2f_rx_bitslip	4	Input	Reserved	

continued...

Port Name	Width	Direction	Clock Domain	Native PHY IP Port Name
f2a_rx_fifo_empty	4	Output	Reserved	
f2a_rx_fifo_full	4	Output	Reserved	
f2a_rx_fifo_pempty	4	Output	Reserved	
f2a_rx_fifo_pfull	4	Output	Reserved	
a2f_rx_fifo_rd_en	4	Input	Reserved	

Related Information

Intel Stratix 10 Stratix 10 L-Tile and H-Tile Transceiver PHY User Guide

1.2.5.3. Control and Status Signals

The PR HSSI Interface provides signals for HSSI PHY PCS status and transceiver loopback control. The signal behavior conforms to the Intel Stratix 10 FPGA Transceiver Native PHY IP core with enhanced PCS. The below table cross references the HSSI port names to the Native PHY IP port names.

Table 9. Control and Status Signals

Port Name	Width	Direction	Clock Domain	Native PHY IP Port Name	Reference
f2a_tx_ready	4	Output	Use synchronizers to cross clock domains to your preferred clock (100MHz)	tx_ready	Transceiver PHY Reset Controller Intel Stratix 10 FPGA IP Interfaces
f2a_rx_ready	4	Output	Use synchronizers to cross clock domains to your preferred clock (100MHz)	rx_ready	Transceiver PHY Reset Controller Intel Stratix 10 FPGA IP Interfaces
a2f_rx_serial lpbken	4	Input	Asynchronous	rx_seriallpbken	PMA, Calibration, and Reset Ports
a2f_channel_r eset	4	Input	Asynchronous	N/A	Transceiver PHY Reset Controller Intel Stratix 10 FPGA IP Interfaces

1.2.6. FPGA Interface Manager (FIM) Resource Utilization

Table 10. FPGA Core Fabric Resource Utilization by the FIM

Parameter	FIM Utilization Total	Device Total	Percentage of Resources Used by FIM	Notes
ALMs	35492	933120	4%	Adaptive Logic Modules blocks.
M20Ks	117	11721	1%	Memory blocks with 20K bits.
DSPs	0	5760	0%	Digital Signal Processing blocks.

1.3. Revision History for FPGA Interface Manager Data Sheet for Intel FPGA PAC D5005

Document Version	Acceleration Stack Version	Changes
2019.08.05	2.0 (compatible with Intel Quartus® Prime Pro Edition18.1.2)	Initial release.