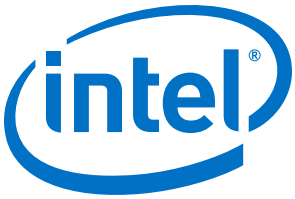

Intel® FPGA Programmable Acceleration Card D5005 Data Sheet

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Contents

1. Introduction

The Intel FPGA Programmable Acceleration Card D5005 (Intel® FPGA PAC D5005) is a PCI Express* Gen 3 x16 compliant card designed to accelerate data center applications.

This datasheet for the Intel FPGA PAC shows electrical, mechanical, compliance, and other key specifications. This datasheet assists data center operators and system integrators to properly deploy the Intel FPGA PAC into their servers. It also documents the FPGA power envelope, connectivity speeds to memory, and network connectivity, so that accelerator function unit (AFU) developers can properly design and test their IP.

The Intel FPGA PAC is supported by the Intel Acceleration Stack for Intel Xeon® CPU with FPGAs. The Acceleration Stack provides a common developer interface to both application and accelerator function developers and includes drivers, Application Programming Interfaces (APIs) and an FPGA Interface Manager (FIM).

Along with acceleration libraries and development tools, the Acceleration Stack saves development time and enables code re-use across multiple Intel FPGA form-factor products, allowing the developer to focus on the unique value-addition of their solution. Developers can use the Accelerator Functional Unit (AFU) Developer's User Guide to get started.

Intel validates each Intel FPGA PAC to support large scale deployments requiring FPGA acceleration.

This platform is targeted for market-specific acceleration in applications such as:

- Finance
- Data Analytics
- Video Transcoding
- Genomics
- Cyber-Security
- High-Performance Computing
- Artificial Intelligence

Note: Throughout this document, any mention of Intel FPGA PAC or Intel FPGA PAC D5005 shall specifically refer to the Intel FPGA Programmable Acceleration Card D5005.

2. Overview

This chapter provides an overview of the Intel FPGA PAC and describes the architecture and components.

2.1. Intel FPGA PAC D5005 Specifications

Figure 1. Conceptual Block Diagram

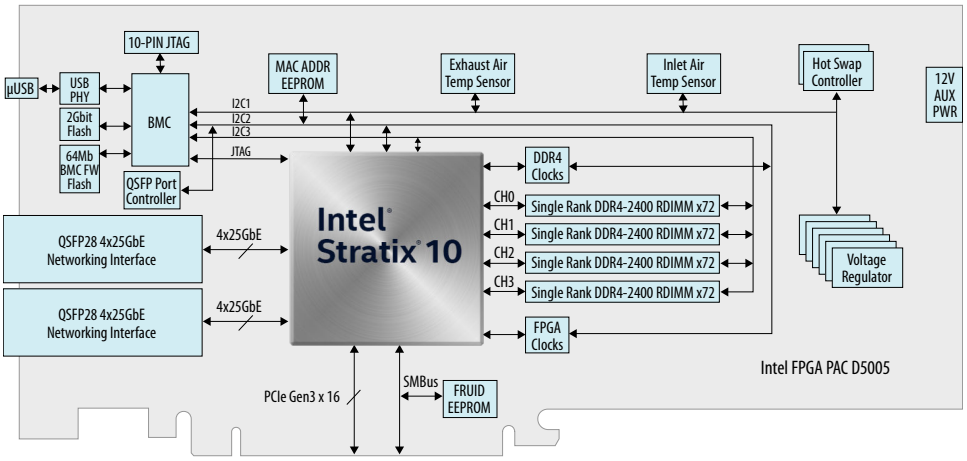


Table 1. Specifications Table

Specification	Value
Power	215 W (Under sufficient cooling capabilities) (1)
Cooling Requirement	Passively cooled. Requires server air flow.
Weight	1 Kilogram
Form Factor	¾ Length, Full height, Dual-slot PCIe* 3.0 CEM specification compliant
Networking Interfaces	Dual QSFP28 Ports: 2x100G
Memory Interfaces	4x 8GB DDR4-2400 with ECC
Management Port	Micro-USB
FPGA Device	1SX280HN2F43E2VG

Note: Initially 1x10G and 4x10G networking capability is supported on each QSFP28 port. Additional configurations will be supported in future releases.

(1) 65 W from the 12 V slot and 150 W from 12 V 2x4 pin auxiliary power connector. 10 W from the 3.3 V slot is not used.

2.2. Intel FPGA PAC Components

2.2.1. Intel Stratix® 10 FPGA

The Intel Stratix® 10 FPGAs feature industry-leading programmable logic built on 14 nm process technology that integrate a rich feature set of embedded peripherals, embedded high-speed transceivers, hard memory controllers and IP protocol controllers. Variable-precision digital signal processing (DSP) blocks integrated with hardened floating point (IEEE 754-compliant) enable the Intel Stratix 10 FPGAs to deliver floating point performance of up to 10 TFLOPS. Intel Stratix 10 FPGAs have a comprehensive set of power-saving features. Combined, these features allow developers to build versatile set of acceleration solutions.

When developing the accelerator function for the Intel FPGA PAC, select the 1SX280HN2F43E2VG device.

2.2.2. Power

Given a specific airflow, the Intel FPGA PAC D5005 can dissipate up to 189 W of power, of which 137 W comes from the FPGA. If the airflow is increased, the Intel FPGA PAC D5005 may be able to dissipate more power up to 215 W; however, you shall bear the responsibility of thermal validation of these conditions.

The Thermal Design Power (TDP) (215 W) is based on the maximum current, per the PCIe specification of 5.4 A from the 12 V-PCIe slot and 12.5 A from the 12 V-Auxiliary 2x4 PCIe power connector and requires optimized cooling conditions. The card TDP is limited to 189 W under the Thermal and Airflow requirement conditions.

As a developer or solution provider, you must design with the AFU to stay within these power guides. If the AFU exceeds this limit or the limit provided by the qualified server vendor, Board Management Controller (BMC) safeguards will shut down the Intel FPGA PAC. Typical server BMC safeguards will likely shut down the server as well. Functionality and reliability of the server and the Intel FPGA PAC are not supported for AFUs that exceed the specification.

The Intel FPGA PAC source power must be provided from both to the 12 V-PCIe slot and the 12V-Auxiliary 2x4 power connector.

The Intel FPGA PAC D5005 is designed to operate under the following conditions:

- No 12 V PCIe slot power, No 12 V Auxiliary Connector Power - PAC OFF
- Only 12 V PCIe slot power, No 12 V Auxiliary Connector Power - PAC OFF
- No 12 V PCIe Slot Power, only 12 V Auxiliary Connector power available - PAC ON, but limited by the total available power from 12V Aux power connector
- 12 V PCIe slot power and 12 V Auxiliary Power Connector available - PAC ON, normal operation up to maximum power capabilities of the PAC card design

The 12 V-Auxiliary power connector pin assignment defined by the PCIe specification is shown below:

Figure 2. Power Connector

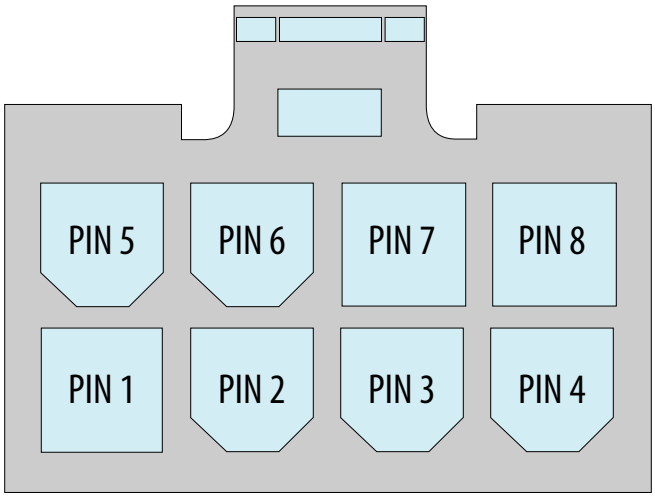


Table 2. 2x4 Auxiliary Power Connector Pin-Out Assignment

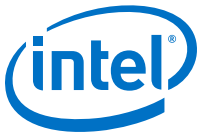
Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Sense1
5	Ground
6	Sense0
7	Ground
8	Ground

2.2.3. PCIe Interface

The Intel FPGA PAC supports up to PCI Express Gen 3 data rates of 8 GT/s .

Table 3. PCIe ID and Power/Thermal Budget

Intel FPGA PAC	PCIe Vendor ID (VID)	PCIe Device ID (DID)	PCIe Sub-Vendor ID (SVID)	PCIe Sub-Device (SDID)
Intel FPGA Programmable Acceleration Card D5005	0x8086	0x0B2B	0x8086	0x0000



2.2.4. DDR4 SDRAM

The Intel FPGA PAC has four banks of Double Data Rate 4 Synchronous Dynamic Random-Access Memory (DDR4 SDRAM). Each bank is populated with 8 GB DDR4 RDIMM modules for a total of 32 GB. The banks are configured as single rank standard RDIMM modules arranged as 72-bit per bank. The memory width is organized as 64 data bits plus 8 ECC bits. Each DDR4 bank operates up to 1200 MHz (DDR4-2400).

Table 4. Memory Table

Supported Manufacturers	**Micron**
Manufacturer Part Number	MTA9ASF1G72PZ-2G9E1
Type	8 GB 288-pin DDR4 RDIMM
Configuration	1 Gb x 72
Rank	Single Rank
Error detection and correction (ECC)	Yes
Data rate	2400 MT/s

2.2.5. Network Interface

The Intel FPGA PAC has two QSFP28 cages on the I/O panel each of which supports up to 100G Ethernet. The Intel FPGA PAC supports Short Reach (SR) QSFP28 class 1-7 (up to 5 W) optical transceivers and Direct Attached Copper (DAC) cables up to 3 m in length.

Note: Current Release supports 1x10 Gbps and 4x10 Gbps operation. Other network interface support configurations will be available in a future release.

2.2.6. Field Replaceable Unit Identification EEPROM

A Field Replaceable Unit Identification (FRUID) EEPROM (Microchip 24AA024-I/SN) located at default SMBUS address `0xA0` is connected to the SMBUS of the PCIe interface. This FRUID EEPROM is powered by the host server's PCIe 3.3 V auxiliary power provided at the PCIe slot connector. This allows the FRUID EEPROM to be readable even when 12 V power to the slot is not provided by the host server.

This FRUID contains board specific information that identify the card installed into the PCIe slot. The FRUID contains the following information:

- Board Manufacturer
- Board Model Number
- Board Serial Number
- Location of Manufacture
- Date of Manufacture

2.2.7. MAC Address EEPROM

A secondary EEPROM (ST-Microelectronics M24128-BWMN6TP) is used to store the starting MAC address and the count (8) of total MAC addresses for the two network interface ports. Each port contains four unique MAC address information (total of eight MAC address for each Intel FPGA PAC). This information can be read by the BMC and FPGA device.

Note: The starting MAC Address for each board is also provided on the label on the back side of the PCB board. The eight MAC addresses are sequentially incremented from the starting MAC address provided.

2.2.8. Flash Memory

There are two QSPI flash memories. BMC Firmware Flash (8 MB) and FPGA Configuration Flash (2 Gb) used to store the FPGA Interface Manager (FIM) on the Intel FPGA PAC.

2.2.9. Control and Support

The following features are available on the Intel FPGA PAC for configuration, control and support:

- PCIe Gen 3 x16
- Board Management Controller (BMC)
- Intel FPGA Download Cable II
- Intel MAX® 10 JTAG

Note: Refer to Board Management Controller on page 9 for additional infromation.

3. Board Management Controller

A Board Management Controller (BMC) resides on the Intel FPGA PAC. The BMC is responsible for controlling, monitoring and giving access to low-level access to board features. The Intel MAX 10 BMC interfaces with on-board sensors, the FPGA and the flash, and it controls power-on/power-off sequences, FPGA configuration and telemetry data polling. The BMC communicates using the Platform Level Data Model (PLDM) version 1.1.1 protocol. The firmware that runs on the external Nios® firmware Quad SPI flash is field upgradeable over PCIe using the remote system update feature.

Features of the BMC

- FPGA configuration and reconfiguration
- Remote System Update: Intel MAX 10 BMC FPGA update image, Intel Stratix 10 FPGA user image and Nios firmware image
- Monitors telemetry data (board temperature, voltage and current)
- Reports telemetry data to host BMC via Platform Level Data Model (PLDM) over MCTP SMBus or Standard I^2C
- Supports PLDM over MCTP SMBus via PCIe SMBus. 0xCE is a 8-bit slave address. Raw 7-bit slave address is 0x67
- Supports Standard I^2C via PCIe SMBus. The I^2C slave address is 0xBC (8-bit)
- Provides protective action when readings are outside of critical thresholds
- Intel FPGA Download Cable functionality for the board
- Power up / down sequencing and fault detection with automatic shut-down protection
- Controls programmable FPGA and DDR4 SDRAM clocks for performance throttling if desired
- Provides low-level access to board features
- Interfaces with sensors, FPGA, flash and QSFPs
- Controls power and resets on the board

Refer to the Intel FPGA PAC D5005 Board Management Controller User Guide for more information.

Related Information

Intel FPGA PAC D5005 Board Management Controller User Guide

3.1. Health Monitoring Features

The Intel FPGA PAC incorporates health monitoring sensors that allow the host server to read telemetry data from the board such as voltage, current, power, temperatures and network status information from various components on the board. These sensors reside on one of three I^2C busses that are connected to the Board Management Controller (BMC) and FPGA device.

Table 5. Available Sensors and their I^2C Bus Number

Sensor Name	I^2C Bus Number	7-bit I^2C Slave Address	Description
12V PCIe Input Power	1	0x42	Maxim® 16545BGPF+T device
12V Aux Input Power	1	0x40	Maxim 16545BGPF+T device
3.3V Power	1	0x43	Enpirion® EM2121H01QI device
VCCERAM Power	1	0x44	Enpirion EM2121L01QI device
VCCR_GXB Power	1	0x45	Enpirion EM2121L01QI device
VCCT_GXB Power	1	0x46	Enpirion EM2121L01QI device
1.8V FPGA Power	1	0x47	Enpirion EM2121H01QI device
VCC Core Power	AVS bus	-	Intersil® ISL68137IRBZ-TR5781 device
Inlet Air Temperature	1	0x4C	Texas Instruments® TMP11ADGKR local sensor
Exhaust Air Temperature	1	0x4D	Texas Instruments TMP11BDGKR local sensor
FPGA Core Die Temperature	1	0x4C	Texas Instruments TMP11ADGKR Remote sensor
FPGA Xcvr Die Temperature	1	0x4D	Texas Instruments TMP11BDGKR Remote sensor
Network Port Controller	2	0x0F	Texas Instruments FPC202RHUR Port Controller
Network Port0 QSFP	2	0x78	QSFP Optical Module
Network Port1 QSFP	2	0x7C	QSFP Optical Module
DIMM0 Temperature	3	0x18	Micron® MTA9ASF1G72PZ-2G9E1 RDIMM module

continued...

Sensor Name	I²C Bus Number	7-bit I²C Slave Address	Description
DIMM1 Temperature	3	0x19	Micron MTA9ASF1G72PZ-2G9E1 RDIMM module
DIMM2 Temperature	3	0x1A	Micron MTA9ASF1G72PZ-2G9E1 RDIMM module
DIMM3 Temperature	3	0x1B	Micron MTA9ASF1G72PZ-2G9E1 RDIMM module

Note: The FPGA VCC Core power has a dedicated AVSbus that is separate from any of the I²C busses.

Note: The QSFP Network ports reside behind the network port controller. See the controller datasheet (Texas Instruments FPC202RHUR) for more information.

Note: The FPGA design can read these sensors directly or through the Board Management Controller using standard PLDM commands and report their status to the host server.

Table 6. Thresholds with Sensor Information

Name	Specification Values	Lower Non-Recoverable (LNR)	Lower Critical (LC)	Lower Non-Critical (LNC)	Upper Non-Critical (UNC)	Upper Critical (UC)	Upper Non-Recoverable (UNR)
Board Power Rail							
12 V Aux Hot Swap Current	12.5 A max				12.5 A	13.2 A	14 A
12 V Aux Hot Swap Voltage	12 V +/-10%	9.6 V	10.2 V	10.5 V	13.2 V	13.5 V	14 V
12 V Aux Hot Swap Temperature	0 °C to 125 °C				118 °C	120 °C	125 °C
12 V PCIe Hot Swap Current	5.5 A max				5.5 A	5.8 A	6 A
12 V PCIe Hot Swap Voltage	12 V +/-10%	9.6 V	10.2 V	10.5 V	13.2 V	13.5 V	14 V
12 V PCIe Hot Swap Temperature	0 °C to 125 °C				118 °C	120 °C	125 °C
3.3 V Regulator Current	20 A max				20 A	22 A	23 A
3.3 V Regulator Voltage	3.3 V +/-5%				3.4 V	3.6 V	3.9 V
3.3 V Regulator Temperature	125 °C max				118 °C	120 °C	125 °C

continued...

Name	Specification Values	Lower Non-Recoverable (LNR)	Lower Critical (LC)	Lower Non-Critical (LNC)	Upper Non-Critical (UNC)	Upper Critical (UC)	Upper Non-Recoverable (UNR)
Board Power Rail							
1.8 V Regulator Current	20 A max				20 A	22 A	23 A
1.8 V Regulator Voltage	1.8 V +/-5%	1.55 V	1.6 V	1.7 V	1.9 V	1.98 V	2.04 V
1.8 V Regulator Temperature	125 °C max				118 °C	120 °C	125 °C
VCCERAM Regulator Current	20 A max				20 A	22 A	23 A
VCCERAM Regulator Voltage	0.9 V +/-30mV	0.7 V	0.8 V	0.85 V	0.95 V	0.99 V	1.08 V
VCCERAM Regulator Temperature	125 °C max				118 °C	120 °C	125 °C
VCCR_GXB Regulator Current	20 A max				20 A	22 A	23 A
VCCR_GXB Regulator Voltage	1.12 V +/-3%	1 V	1.05 V	1.08 V	1.15 V	1.2 V	1.35 V
VCCR_GXB Regulator Temperature	125 °C max				118 °C	120 °C	125 °C
VCCT_GXB Regulator Current	20 A max				20 A	22 A	23 A
VCCT_GXB Regulator Voltage	1.12 V +/-2%	1 V	1.05 V	1.08 V	1.15 V	1.2 V	1.35 V
VCCT_GXB Regulator Temperature	125 °C max				118 °C	120 C	125 C
FPGA Core Regulator Voltage	0.80 V–0.94 V +/-30 mV				0.99 V	1.05 V	1.15 V
FPGA Core Regulator Current	150 A max				150 A	160 A	170 A
FPGA Core Regulator Temperature	-40 °C to 125 °C				115 °C	120 °C	125 °C
FPGA Core Die Temperature	0 °C to 100 °C				90 °C	95 °C	100 °C

continued...

Name	Specification Values	Lower Non-Recoverable (LNR)	Lower Critical (LC)	Lower Non-Critical (LNC)	Upper Non-Critical (UNC)	Upper Critical (UC)	Upper Non-Recoverable (UNR)
Board Power Rail							
FPGA Transceiver Die Temperature	0 °C to 100 °C				90 °C	95 °C	100 °C
QSFP Port 0 Temperature	0 °C to 70 °C max				70 °C	80 °C	90 °C
QSFP Port 1 Temperature	0 °C to 70 °C max				70 °C	80 °C	90 °C
DDR4 Module 0 Temperature	0 °C to 95 °C				85 °C	90 °C	95 °C
DDR4 Module 1 Temperature	0 °C to 95 °C				85 °C	90 °C	95 °C
DDR4 Module 2 Temperature	0 °C to 95 °C				85 °C	90 °C	95 °C
DDR4 Module 3 Temperature	0 °C to 95 °C				85 °C	90 °C	95 °C

3.2. Supported PLDM/MCTP Commands

Refer to the Intel FPGA PAC D5005 Board Management Controller User Guide for more information.

Related Information

Intel FPGA PAC D5005 Board Management Controller User Guide

4. FPGA Interface Manager

The FPGA Interface Manager (FIM) contains the FPGA logic to support the accelerators, including the PCIe IP core, the Core Cache Interface protocol (CCI-P) fabric, the on-board DDR memory interface and management engine. Specific features of the FIM are listed in the following documents:

- Intel Acceleration Stack Quick Start Guide for Intel FPGA Programmable Acceleration Card D5005
- OPAE Intel FPGA Linux Device Driver Architecture Guide

The 2 Gb flash memory stores the FPGA Interface Manager (FIM) which provides a common user interface for placement of accelerator functions. In addition, the FIM allows dynamic downloading of new accelerator functions and updates to the FIM.

4.1. Updating the FIM

The FIM image in flash memory can be updated using the following methods:

- The primary method is for the FIM to be updated over PCIe via the OPAE command `fpgaflash`. This loads the FIM image into the on-board flash memory. Upon power up, the board loads the image from flash onto the FPGA.
- Directly configure the FPGA via JTAG through the USB port. This use case should only be used if the FIM image gets corrupted or erased.

5. System Compatibility

This chapter describes the platforms and Linux distribution targeted for the Intel FPGA PAC validation.

Note: OEM partners validate server platforms.

Table 7. Operating System Compatibility

Operating System Name	Operating System Family
Red Hat Enterprise Linux (RHEL) 7.6	RHEL

Note: The above mentioned operating systems are Linux Kernel 3.10.

Table 8. Ordering Part Number (OPN) Table

OPN	Description
BD-ACD-1SX280H2DES	Engineering Sample
BD-ACD-D5005-1	Production Board

6. Power Requirements

The Intel FPGA PAC supports a total power of 215 W. Intel has conducted thermal validation up to 189 W. For any power levels above 189 W, you are responsible for conducting thermal validation at increased power levels.

As the developer or solution provider, you must ensure that the workload does not exceed this limit, or the limit provided by the qualified server vendor. Functionality and reliability of the server is not supported for workloads that exceed the specification.

The Intel FPGA PAC source power must be provided from both the 12 V-PCIe slot and the 12 V-Auxiliary 2 x 4 power connector.

The Intel FPGA PAC D5005 is designed to operate under the following conditions:

- No 12 V PCIe slot power, No 12 V Auxiliary Connector Power - PAC OFF
- Only 12 V PCIe slot power, No 12 V Auxiliary Connector Power - PAC OFF
- No 12 V PCIe Slot Power, only 12 V Auxiliary Connector power available - PAC ON, but limited by the total available power from 12V Aux power connector
- 12 V PCIe slot power and 12 V Auxiliary Power Connector available - PAC ON, normal operation up to maximum power capabilities of the PAC card design

7. Mechanical Information

Intel FPGA PAC D5005 Dimensions

- Dual-slot PCIe card
- PCIe×16 mechanical with hockey stick card retainer
- 3/4-length with included full-length PCIe server extension mounting bracket
- PCB thickness 0.062 inches
- Card Weight is 1 Kg.

Note: All dimensions in mm.

Figure 3. Intel FPGA PAC D5005 Dimensions

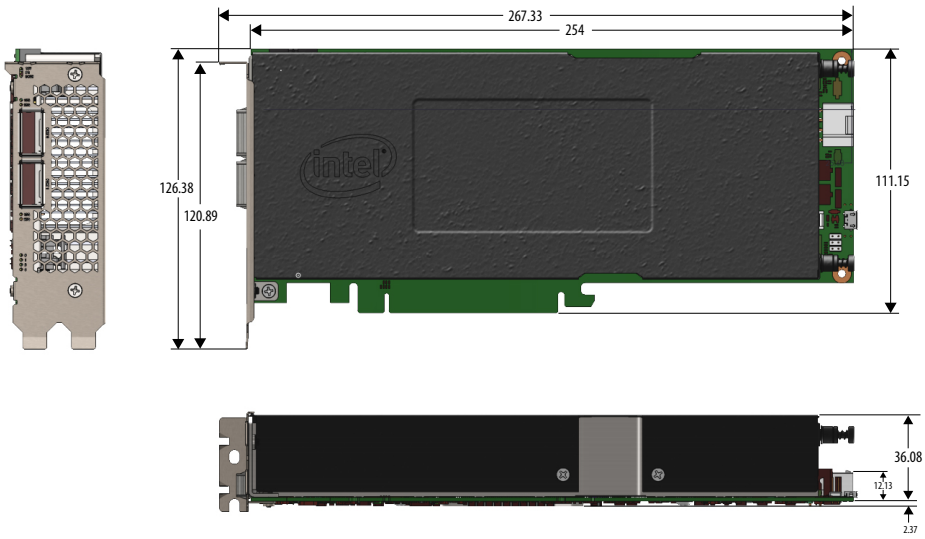
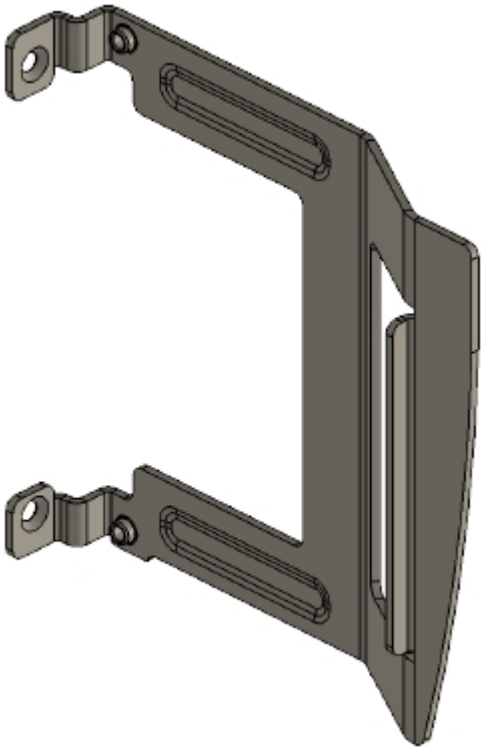


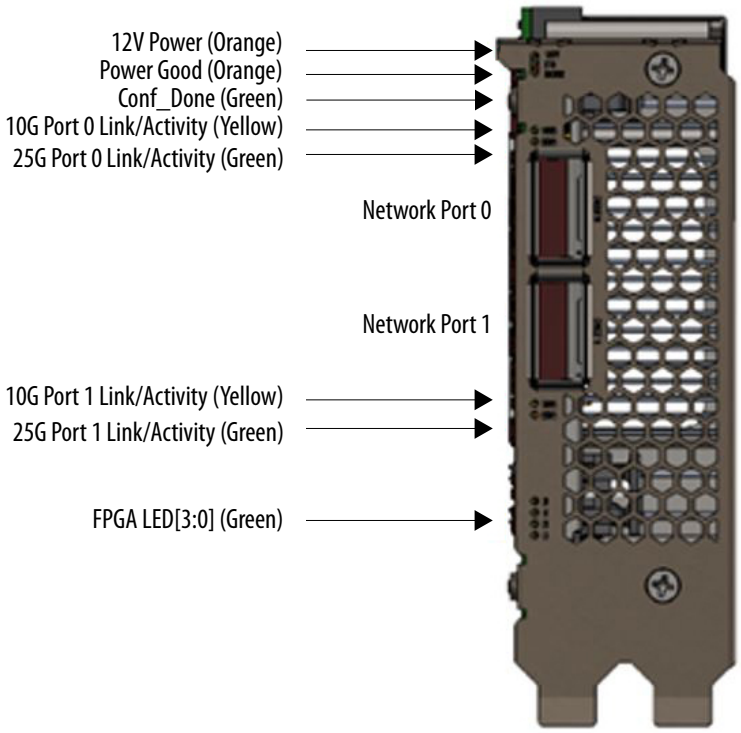
Figure 4. Extension Mounting Bracket

Figure 5. Non-coplanar Extension Bracket



Ports and Status LEDs Definition

Figure 6. Ports and LEDs



Port Description

- Network Port 0 – QSFP28 port capable of accepting 40 G/100 G SR optical module or 3 m DAC cable
- Network Port 1 – QSFP28 port capable of accepting 40 G/100 G SR optical module or 3 m DAC cable

LED Description

- 12V – Orange LED. LED is on when 12 V power is present
- PG – Orange LED. LED is on when all power on the board is present
- DONE – Green LED. On indicates that the FPGA FIM is successfully loaded. This LED does not change states when AFUs are loaded.
- Port 0 10 G – Yellow LED. On when port 0 channels are linked at either 10 GbE or 40 GbE. Off when link is down. Blinking when there is either 10 GbE or 40 GbE network activity on the port.
- Port 0 25 G – Green LED. On when port 0 channels are linked at either 25 GbE or 1000 GbE. Off when link is down. Blinking when there is either 25 GbE or 100 GbE network activity on the port.

- Port 1 10 G – Yellow LED. On when port 1 channels are linked at either 10 GbE or 40 GbE. Off when link is down. Blinking when there is either 10 GbE or 40 GbE network activity on the port.
- Port 1 25 G – Green LED. On when port 1 channels are linked at either 25 GbE or 1000 GbE. Off when link is down. Blinking when there is either 25 GbE or 100 GbE network activity on the port.
- FPGA LED [3:0] - Green LED. These LEDs are connected directly to the FPGA for customer defined usage.

8. Thermal and Airflow Requirements

The Intel FPGA PAC D5005 has been thermally validated to 189 W for the entire card under provided flow characteristics. The FPGA junction temperature must not exceed 100 °C. The temperature of the QSFP28 modules must meet the module vendor's specification, usually 70 °C or 85 °C.

Table 9. Thermal Specifications

Parameter	Value
Operating Temperature	0 °C – 45 °C
Storage Temperature	-40 °C to 65 °C
Storage Humidity	5% to 85% RH with a 35 °C (95 °F) maximum dew point

Please note the following:

- The BMC continuously monitors the FPGA junction temperature and will automatically shut down the when the FPGA junction temperature reaches 100 °C.
- AFU Developers should use the Intel Stratix 10 PowerPlay Early Power Estimator and the Quartus Prime Power Analyzer to estimate the FPGA power consumption.

Related Information

- Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition
  The Intel Quartus Prime Pro Edition software provides a complete design environment for FPGA and SoC designs. The Power Analyzer is described in the Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition.
- Early Power Estimator for Intel Stratix 10 FPGAs User Guide
  This user guide describes the Early Power Estimator (EPE) for Intel Stratix 10 FPGA. This user guide provides guidelines for using the EPE, and details about thermal analysis and the factors contributing to FPGA power consumption.

8.1. Thermal Cooling Requirements

The Intel FPGA PAC has been thermally validated up to 189 W for the entire card. System airflow to the Intel FPGA PAC must be provided to keep the FPGA junction temperature below its 100 °C maximum specification. The temperature of the QSFP modules must also meet the module vendor's specification, usually 70 °C or 85 °C. The following table shows the airflow requirement for the Intel FPGA PAC during operation.

Table 10. Description of Terms

Term	Description
Linear Feet per Minute (LFM)	Air velocity is calculated by dividing the volumetric flow rate by the cross-sectional area of the flow passage.
T_{LA}	The measured ambient temperature locally surrounding the FPGA. The ambient temperature should be measured just upstream of a passive heatsink or at fan inlet for an active heatsink.

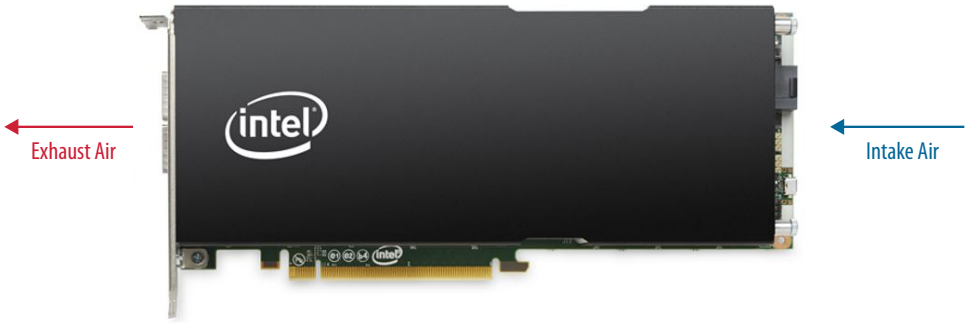
Table 11. Thermal Specifications

Local Air Inlet Temperature (°C)	Required Flow Rate (CFM)
30	14.2
35	16.7
40	20.0
45	25.0
50	33.3

8.2. Airflow Requirements

The recommended airflow direction is from the side of the 12 V auxiliary power connector (intake air side) to the I/O panel (exhaust air side).

Figure 7. Intel FPGA PAC D5005 Airflow Pattern



A. Intel FPGA Programmable Acceleration Card D5005 Pin Assignments

A.1. FPGA Device

The FPGA device that is installed onto the Intel FPGA Programmable Acceleration Card D5005 is an Intel Stratix 10 1SX280HN2F43E2VG.

A.2. PCIe Interface

A PCIe 3.0 compliant x16 interface is connected directly to the FPGA. The FPGA pin number assignment is provided below.

Table 12. PCI Express Interface to FPGA Pin Assignments

Pin Name	FPGA Pin Number	Description
PCIE_EDGE_100M_P	AM34	PCIE 100MHz clock AM34. Bank 1D
PCIE_EDGE_100M_N	AM33	PCIE 100MHz clock AM33. Bank 1D
PCIE_TX_P0	AV29	PCIe TX0 to FPGA RX0 input. Bank 1C
PCIE_TX_N0	AV30	PCIe TX0 to FPGA RX0 input. Bank 1C
PCIE_TX_P1	AY29	PCIe TX1 to FPGA RX1 input. Bank 1C
PCIE_TX_N1	AY30	PCIe TX1 to FPGA RX1 input. Bank 1C
PCIE_TX_P2	BB29	PCIe TX2 to FPGA RX2 input. Bank 1C
PCIE_TX_N2	BB30	PCIe TX2 to FPGA RX2 input. Bank 1C
PCIE_TX_P3	AW32	PCIe TX3 to FPGA RX3 input. Bank 1C
PCIE_TX_N3	AW31	PCIe TX3 to FPGA RX3 input. Bank 1C
PCIE_TX_P4	BA31	PCIe TX4 to FPGA RX4 input. Bank 1C
PCIE_TX_N4	BA32	PCIe TX4 to FPGA RX4 input. Bank 1C
PCIE_TX_P5	AY34	PCIe TX5 to FPGA RX5 input. Bank 1C
PCIE_TX_N5	AY33	PCIe TX5 to FPGA RX5 input. Bank 1C
PCIE_TX_P6	AU35	PCIe TX6 to FPGA RX6 input. Bank 1D
PCIE_TX_N6	AU36	PCIe TX6 to FPGA RX6 input. Bank 1D
PCIE_TX_P7	AW36	PCIe TX7 to FPGA RX7 input. Bank 1D
PCIE_TX_N7	AW35	PCIe TX7 to FPGA RX7 input. Bank 1D
PCIE_TX_P8	AR35	PCIe TX8 to FPGA RX8 input. Bank 1D

continued...

Pin Name	FPGA Pin Number	Description
PCIE_TX_N8	AR36	PCIe TX8 to FPGA RX8 input. Bank 1D
PCIE_TX_P9	AN35	PCIe TX9 to FPGA RX9 input. Bank 1D
PCIE_TX_N9	AN36	PCIe TX9 to FPGA RX9 input. Bank 1D
PCIE_TX_P10	AT37	PCIe TX10 to FPGA RX10 input. Bank 1D
PCIE_TX_N10	AT38	PCIe TX10 to FPGA RX10 input. Bank 1D
PCIE_TX_P11	AP38	PCIe TX11 to FPGA RX11 input. Bank 1D
PCIE_TX_N11	AP37	PCIe TX11 to FPGA RX11 input. Bank 1D
PCIE_TX_P12	AL35	PCIe TX12 to FPGA RX12 input. Bank 1E
PCIE_TX_N12	AL36	PCIe TX12 to FPGA RX12 input. Bank 1E
PCIE_TX_P13	AM38	PCIe TX13 to FPGA RX13 input. Bank 1E
PCIE_TX_N13	AM37	PCIe TX13 to FPGA RX13 input. Bank 1E
PCIE_TX_P14	AK38	PCIe TX14 to FPGA RX14 input. Bank 1E
PCIE_TX_N14	AK37	PCIe TX14 to FPGA RX14 input. Bank 1E
PCIE_TX_P15	AJ36	PCIe TX15 to FPGA RX15 input. Bank 1E
PCIE_TX_N15	AJ35	PCIe TX15 to FPGA RX15 input. Bank 1E
PCIE_RX_P0	BB33	PCIe RX0 from FPGA TX0 output. Bank 1C
PCIE_RX_N0	BB34	PCIe RX0 from FPGA TX0 output. Bank 1C
PCIE_RX_P1	BA35	PCIe RX1 from FPGA TX1 output. Bank 1C
PCIE_RX_N1	BA36	PCIe RX1 from FPGA TX1 output. Bank 1C
PCIE_RX_P2	BB37	PCIe RX2 from FPGA TX2 output. Bank 1C
PCIE_RX_N2	BB38	PCIe RX2 from FPGA TX2 output. Bank 1C
PCIE_RX_P3	AY37	PCIe RX3 from FPGA TX3 output. Bank 1C
PCIE_RX_N3	AY38	PCIe RX3 from FPGA TX3 output. Bank 1C
PCIE_RX_P4	BA40	PCIe RX4 from FPGA TX4 output. Bank 1C
PCIE_RX_N4	BA39	PCIe RX4 from FPGA TX4 output. Bank 1C
PCIE_RX_P5	AV37	PCIe RX5 from FPGA TX5 output. Bank 1C
PCIE_RX_N5	AV38	PCIe RX5 from FPGA TX5 output. Bank 1C
PCIE_RX_P6	AW40	PCIe RX6 from FPGA TX6 output. Bank 1D
PCIE_RX_N6	AW39	PCIe RX6 from FPGA TX6 output. Bank 1D
PCIE_RX_P7	AV42	PCIe RX7 from FPGA TX7 output. Bank 1D
PCIE_RX_N7	AV41	PCIe RX7 from FPGA TX7 output. Bank 1D
PCIE_RX_P8	AU40	PCIe RX8 from FPGA TX8 output. Bank 1D
PCIE_RX_N8	AU39	PCIe RX8 from FPGA TX8 output. Bank 1D
PCIE_RX_P9	AT42	PCIe RX9 from FPGA TX9 output. Bank 1D

continued...

Pin Name	FPGA Pin Number	Description
PCIE_RX_N9	AT41	PCIe RX9 from FPGA TX9 output. Bank 1D
PCIE_RX_P10	AR40	PCIe RX10 from FPGA TX10 output. Bank 1D
PCIE_RX_N10	AR39	PCIe RX10 from FPGA TX10 output. Bank 1D
PCIE_RX_P11	AP42	PCIe RX11 from FPGA TX11 output. Bank 1D
PCIE_RX_N11	AP41	PCIe RX11 from FPGA TX11 output. Bank 1D
PCIE_RX_P12	AN40	PCIe RX12 from FPGA TX12 output. Bank 1E
PCIE_RX_N12	AN39	PCIe RX12 from FPGA TX12 output. Bank 1E
PCIE_RX_P13	AM42	PCIe RX13 from FPGA TX13 output. Bank 1E
PCIE_RX_N13	AM41	PCIe RX13 from FPGA TX13 output. Bank 1E
PCIE_RX_P14	AL40	PCIe RX14 from FPGA TX14 output. Bank 1E
PCIE_RX_N14	AL39	PCIe RX14 from FPGA TX14 output. Bank 1E
PCIE_RX_P15	AK42	PCIe RX15 from FPGA TX15 output. Bank 1E
PCIE_RX_N15	AK41	PCIe RX15 from FPGA TX15 output. Bank 1E

A.3. DDR4 Memory Configuration

The Intel FPGA PAC D5005 has four banks of DDR4-SDRAM memory identified as DIMM 0 - 3. Each DIMM is populated with 8 GB each of DDR4 RDIMM modules. The banks are configured as single rank standard RDIMM modules arranged as 72-bit per bank. The memory width is organized as 64 data bits plus 8 ECC bits. Each DDR4 bank operates up to 1200 MHz (DDR4-2400).

Table 13. Supported DDR4 Memory Configuration

DDR4 Memory	
Supported Manufacturers	Micron
Manufacturer Part Number	MTA9ASF1G72PZ-2G9E1
Type	8GB 288-pin DDR4 RDIMM
Configuration	1 Gb x 72
Rank	Single Rank
Error detection and correction (ECC)	Yes
Data rate	2400 MT/s

The FPGA pin assignment for each DIMM interface is shown below. Use these pin assignments for your Intel Quartus® Prime designs.

Table 14. DIMM 0 Interface to FPGA Pin Assignments

Signal Name	FPGA Pin Number
DDR4_CH0_1V8_EVENT_N	AF10
DDR4_CH0_A0	AT4

continued...

Signal Name	FPGA Pin Number
DDR4_CH0_A1	AT5
DDR4_CH0_A10	AT2
DDR4_CH0_A11	AT1
DDR4_CH0_A12	AN2
DDR4_CH0_A13	AN5
DDR4_CH0_A14	AM5
DDR4_CH0_A15	AM2
DDR4_CH0_A16	AM3
DDR4_CH0_A17	AM4
DDR4_CH0_A2	AR2
DDR4_CH0_A3	AR1
DDR4_CH0_A4	AR3
DDR4_CH0_A5	AR4
DDR4_CH0_A6	AP1
DDR4_CH0_A7	AN1
DDR4_CH0_A8	AP4
DDR4_CH0_A9	AP3
DDR4_CH0_ACTN	AR7
DDR4_CH0_ALERTN	AP6
DDR4_CH0_BA0	AL4
DDR4_CH0_BA1	AL1
DDR4_CH0_BG0	AL2
DDR4_CH0_BG1	AR9
DDR4_CH0_CKE	AT6
DDR4_CH0_CKN	AP11
DDR4_CH0_CKP	AP10
DDR4_CH0_CSN	AR8
DDR4_CH0_DQ[0]	AF1
DDR4_CH0_DQ[1]	AH6
DDR4_CH0_DQ[10]	AK4
DDR4_CH0_DQ[11]	AJ4
DDR4_CH0_DQ[12]	AK1
DDR4_CH0_DQ[13]	AH1
DDR4_CH0_DQ[14]	AK3

continued...

Signal Name	FPGA Pin Number
DDR4_CH0_DQ[15]	AJ1
DDR4_CH0_DQ[16]	AL12
DDR4_CH0_DQ[17]	AK11
DDR4_CH0_DQ[18]	AL9
DDR4_CH0_DQ[19]	AK8
DDR4_CH0_DQ[2]	AH3
DDR4_CH0_DQ[20]	AL14
DDR4_CH0_DQ[21]	AK14
DDR4_CH0_DQ[22]	AL7
DDR4_CH0_DQ[23]	AK9
DDR4_CH0_DQ[24]	AH13
DDR4_CH0_DQ[25]	AG7
DDR4_CH0_DQ[26]	AJ10
DDR4_CH0_DQ[27]	AJ8
DDR4_CH0_DQ[28]	AJ13
DDR4_CH0_DQ[29]	AG8
DDR4_CH0_DQ[3]	AG2
DDR4_CH0_DQ[30]	AJ9
DDR4_CH0_DQ[31]	AH8
DDR4_CH0_DQ[32]	AU4
DDR4_CH0_DQ[33]	AU5
DDR4_CH0_DQ[34]	AU3
DDR4_CH0_DQ[35]	AV2
DDR4_CH0_DQ[36]	AV7
DDR4_CH0_DQ[37]	AV8
DDR4_CH0_DQ[38]	AU2
DDR4_CH0_DQ[39]	AV3
DDR4_CH0_DQ[4]	AF2
DDR4_CH0_DQ[40]	AY7
DDR4_CH0_DQ[41]	AW10
DDR4_CH0_DQ[42]	AV11
DDR4_CH0_DQ[43]	AW8
DDR4_CH0_DQ[44]	AY6
DDR4_CH0_DQ[45]	AW11

continued...

Signal Name	FPGA Pin Number
DDR4_CH0_DQ[46]	AV12
DDR4_CH0_DQ[47]	AW9
DDR4_CH0_DQ[48]	AU8
DDR4_CH0_DQ[49]	AT12
DDR4_CH0_DQ[5]	AH7
DDR4_CH0_DQ[50]	AT9
DDR4_CH0_DQ[51]	AT7
DDR4_CH0_DQ[52]	AU7
DDR4_CH0_DQ[53]	AT10
DDR4_CH0_DQ[54]	AU9
DDR4_CH0_DQ[55]	AR12
DDR4_CH0_DQ[56]	BA2
DDR4_CH0_DQ[57]	AY4
DDR4_CH0_DQ[58]	AW3
DDR4_CH0_DQ[59]	BA5
DDR4_CH0_DQ[6]	AH2
DDR4_CH0_DQ[60]	AY2
DDR4_CH0_DQ[61]	AW4
DDR4_CH0_DQ[62]	AY3
DDR4_CH0_DQ[63]	BB5
DDR4_CH0_DQ[64]	AM7
DDR4_CH0_DQ[65]	AM8
DDR4_CH0_DQ[66]	AN13
DDR4_CH0_DQ[67]	AN12
DDR4_CH0_DQ[68]	AN6
DDR4_CH0_DQ[69]	AN7
DDR4_CH0_DQ[7]	AG3
DDR4_CH0_DQ[70]	AM9
DDR4_CH0_DQ[71]	AM10
DDR4_CH0_DQ[8]	AK2
DDR4_CH0_DQ[9]	AJ3
DDR4_CH0_ODT	AP8
DDR4_CH0_PAR	AP5
DDR4_CH0_RESETN	AP9

continued...

Signal Name	FPGA Pin Number
DDR4_CH0_X4_DQS11N	AU12
DDR4_CH0_X4_DQS11P_DBI10N	AU13
DDR4_CH0_X4_DQS13N	AP13
DDR4_CH0_X4_DQS13P_DBI12N	AR13
DDR4_CH0_X4_DQS15N	AW6
DDR4_CH0_X4_DQS15P_DBI14N	AW5
DDR4_CH0_X4_DQS17N	AM13
DDR4_CH0_X4_DQS17P_DBI16N	AM12
DDR4_CH0_X4_DQS1N	AF4
DDR4_CH0_X4_DQS1P_DBI0N	AG4
DDR4_CH0_X4_DQS3N	AJ5
DDR4_CH0_X4_DQS3P_DBI2N	AJ6
DDR4_CH0_X4_DQS5N	AK13
DDR4_CH0_X4_DQS5P_DBI4N	AK12
DDR4_CH0_X4_DQS7N	AH12
DDR4_CH0_X4_DQS7P_DBI6N	AH11
DDR4_CH0_X4_DQS9N	AV1
DDR4_CH0_X4_DQS9P_DBI8N	AW1
DDR4_CH0_X8_DQS0N	AG5
DDR4_CH0_X8_DQS0P	AH5
DDR4_CH0_X8_DQS10N	AU10
DDR4_CH0_X8_DQS10P	AV10
DDR4_CH0_X8_DQS12N	AR11
DDR4_CH0_X8_DQS12P	AT11
DDR4_CH0_X8_DQS14N	BB4
DDR4_CH0_X8_DQS14P	BA4
DDR4_CH0_X8_DQS16N	AN11
DDR4_CH0_X8_DQS16P	AN10
DDR4_CH0_X8_DQS2N	AK7
DDR4_CH0_X8_DQS2P	AK6
DDR4_CH0_X8_DQS4N	AL10
DDR4_CH0_X8_DQS4P	AL11
DDR4_CH0_X8_DQS6N	AJ11
DDR4_CH0_X8_DQS6P	AH10

continued...

Signal Name	FPGA Pin Number
DDR4_CH0_X8_DQS8N	AV5
DDR4_CH0_X8_DQS8P	AV6
LVDS_DDR4_CH0_CLK_N	AL6
LVDS_DDR4_CH0_CLK_P	AL5

Table 15. DIMM 1 Interface to FPGA Pin Assignments

Signal Name	FPGA Pin Number
DDR4_CH1_1V8_EVENT_N	AG10
DDR4_CH1_A0	H1
DDR4_CH1_A1	J1
DDR4_CH1_A10	K3
DDR4_CH1_A11	J3
DDR4_CH1_A12	J4
DDR4_CH1_A13	K6
DDR4_CH1_A14	J6
DDR4_CH1_A15	H3
DDR4_CH1_A16	G3
DDR4_CH1_A17	H5
DDR4_CH1_A2	L2
DDR4_CH1_A3	K2
DDR4_CH1_A4	F2
DDR4_CH1_A5	F1
DDR4_CH1_A6	L1
DDR4_CH1_A7	K1
DDR4_CH1_A8	G2
DDR4_CH1_A9	H2
DDR4_CH1_ACTN	L5
DDR4_CH1_ALERTN	L4
DDR4_CH1_BA0	H6
DDR4_CH1_BA1	G4
DDR4_CH1_BG0	G5
DDR4_CH1_BG1	M10
DDR4_CH1_CKE	M4
DDR4_CH1_CKN	L7
DDR4_CH1_CKP	L6

continued...

Signal Name	FPGA Pin Number
DDR4_CH1_CSN	M5
DDR4_CH1_DQ[0]	H10
DDR4_CH1_DQ[1]	H11
DDR4_CH1_DQ[10]	A6
DDR4_CH1_DQ[11]	E7
DDR4_CH1_DQ[12]	E6
DDR4_CH1_DQ[13]	D6
DDR4_CH1_DQ[14]	C6
DDR4_CH1_DQ[15]	A7
DDR4_CH1_DQ[16]	J8
DDR4_CH1_DQ[17]	G7
DDR4_CH1_DQ[18]	J9
DDR4_CH1_DQ[19]	F6
DDR4_CH1_DQ[2]	G10
DDR4_CH1_DQ[20]	F5
DDR4_CH1_DQ[21]	H7
DDR4_CH1_DQ[22]	H8
DDR4_CH1_DQ[23]	F7
DDR4_CH1_DQ[24]	C2
DDR4_CH1_DQ[25]	D3
DDR4_CH1_DQ[26]	B2
DDR4_CH1_DQ[27]	B3
DDR4_CH1_DQ[28]	E1
DDR4_CH1_DQ[29]	D1
DDR4_CH1_DQ[3]	F9
DDR4_CH1_DQ[30]	C3
DDR4_CH1_DQ[31]	D4
DDR4_CH1_DQ[32]	R4
DDR4_CH1_DQ[33]	R1
DDR4_CH1_DQ[34]	T2
DDR4_CH1_DQ[35]	R3
DDR4_CH1_DQ[36]	N3
DDR4_CH1_DQ[37]	P3
DDR4_CH1_DQ[38]	T1

continued...

Signal Name	FPGA Pin Number
DDR4_CH1_DQ[39]	R2
DDR4_CH1_DQ[4]	J10
DDR4_CH1_DQ[40]	N5
DDR4_CH1_DQ[41]	P4
DDR4_CH1_DQ[42]	N8
DDR4_CH1_DQ[43]	P10
DDR4_CH1_DQ[44]	N6
DDR4_CH1_DQ[45]	P5
DDR4_CH1_DQ[46]	N7
DDR4_CH1_DQ[47]	N10
DDR4_CH1_DQ[48]	U4
DDR4_CH1_DQ[49]	T4
DDR4_CH1_DQ[5]	J11
DDR4_CH1_DQ[50]	U5
DDR4_CH1_DQ[51]	T9
DDR4_CH1_DQ[52]	U2
DDR4_CH1_DQ[53]	R9
DDR4_CH1_DQ[54]	T5
DDR4_CH1_DQ[55]	U3
DDR4_CH1_DQ[56]	R13
DDR4_CH1_DQ[57]	N11
DDR4_CH1_DQ[58]	R14
DDR4_CH1_DQ[59]	T11
DDR4_CH1_DQ[6]	H12
DDR4_CH1_DQ[60]	T12
DDR4_CH1_DQ[61]	N12
DDR4_CH1_DQ[62]	T10
DDR4_CH1_DQ[63]	R12
DDR4_CH1_DQ[64]	K14
DDR4_CH1_DQ[65]	K13
DDR4_CH1_DQ[66]	L9
DDR4_CH1_DQ[67]	L11
DDR4_CH1_DQ[68]	M13
DDR4_CH1_DQ[69]	M14

continued...

Signal Name	FPGA Pin Number
DDR4_CH1_DQ[7]	F10
DDR4_CH1_DQ[70]	L10
DDR4_CH1_DQ[71]	K9
DDR4_CH1_DQ[8]	B5
DDR4_CH1_DQ[9]	A5
DDR4_CH1_ODT	M8
DDR4_CH1_PAR	K4
DDR4_CH1_RESETN	M9
DDR4_CH1_X4_DQS11N	P6
DDR4_CH1_X4_DQS11P_DBI10N	R6
DDR4_CH1_X4_DQS13N	R8
DDR4_CH1_X4_DQS13P_DBI12N	R7
DDR4_CH1_X4_DQS15N	P11
DDR4_CH1_X4_DQS15P_DBI14N	R11
DDR4_CH1_X4_DQS17N	K12
DDR4_CH1_X4_DQS17P_DBI16N	K11
DDR4_CH1_X4_DQS1N	H13
DDR4_CH1_X4_DQS1P_DBI0N	J13
DDR4_CH1_X4_DQS3N	E8
DDR4_CH1_X4_DQS3P_DBI2N	E9
DDR4_CH1_X4_DQS5N	E2
DDR4_CH1_X4_DQS5P_DBI4N	E3
DDR4_CH1_X4_DQS7N	B4
DDR4_CH1_X4_DQS7P_DBI6N	A4
DDR4_CH1_X4_DQS9N	M2
DDR4_CH1_X4_DQS9P_DBI8N	N2
DDR4_CH1_X8_DQS0N	G9
DDR4_CH1_X8_DQS0P	G8
DDR4_CH1_X8_DQS10N	P8
DDR4_CH1_X8_DQS10P	P9
DDR4_CH1_X8_DQS12N	T7
DDR4_CH1_X8_DQS12P	T6
DDR4_CH1_X8_DQS14N	N13
DDR4_CH1_X8_DQS14P	P13

continued...

Signal Name	FPGA Pin Number
DDR4_CH1_X8_DQS16N	L12
DDR4_CH1_X8_DQS16P	M12
DDR4_CH1_X8_DQS2N	B7
DDR4_CH1_X8_DQS2P	C7
DDR4_CH1_X8_DQS4N	E4
DDR4_CH1_X8_DQS4P	F4
DDR4_CH1_X8_DQS6N	D5
DDR4_CH1_X8_DQS6P	C5
DDR4_CH1_X8_DQS8N	N1
DDR4_CH1_X8_DQS8P	P1
LVDS_DDR4_CH1_CLK_N	K7
LVDS_DDR4_CH1_CLK_P	K8

Table 16. DIMM 2 Interface to FPGA Pin Assignments

Signal Name	FPGA Pin Number
DDR4_CH2_1V8_EVENT_N	AE11
DDR4_CH2_A0	AM25
DDR4_CH2_A1	AN25
DDR4_CH2_A10	AR23
DDR4_CH2_A11	AR24
DDR4_CH2_A12	AY21
DDR4_CH2_A13	BB19
DDR4_CH2_A14	BA19
DDR4_CH2_A15	AW21
DDR4_CH2_A16	AV21
DDR4_CH2_A17	BB20
DDR4_CH2_A2	AP24
DDR4_CH2_A3	AP25
DDR4_CH2_A4	AL24
DDR4_CH2_A5	AM24
DDR4_CH2_A6	AL26
DDR4_CH2_A7	AL25
DDR4_CH2_A8	AP23
DDR4_CH2_A9	AN23
DDR4_CH2_ACTN	AR22

continued...

Signal Name	FPGA Pin Number
DDR4_CH2_ALERTN	AY23
DDR4_CH2_BA0	BA20
DDR4_CH2_BA1	AW20
DDR4_CH2_BG0	AV20
DDR4_CH2_BG1	BA22
DDR4_CH2_CKE	AV23
DDR4_CH2_CKN	AV22
DDR4_CH2_CKP	AU22
DDR4_CH2_CSN	AT22
DDR4_CH2_DQ[0]	AL17
DDR4_CH2_DQ[1]	AL19
DDR4_CH2_DQ[10]	AJ26
DDR4_CH2_DQ[11]	AK23
DDR4_CH2_DQ[12]	AL20
DDR4_CH2_DQ[13]	AH24
DDR4_CH2_DQ[14]	AJ25
DDR4_CH2_DQ[15]	AL21
DDR4_CH2_DQ[16]	AT17
DDR4_CH2_DQ[17]	AR16
DDR4_CH2_DQ[18]	AT16
DDR4_CH2_DQ[19]	AP18
DDR4_CH2_DQ[2]	AM17
DDR4_CH2_DQ[20]	AU17
DDR4_CH2_DQ[21]	AP19
DDR4_CH2_DQ[22]	AT19
DDR4_CH2_DQ[23]	AR19
DDR4_CH2_DQ[24]	AY17
DDR4_CH2_DQ[25]	AY16
DDR4_CH2_DQ[26]	AU18
DDR4_CH2_DQ[27]	AY18
DDR4_CH2_DQ[28]	AV18
DDR4_CH2_DQ[29]	AW16
DDR4_CH2_DQ[3]	AK17
DDR4_CH2_DQ[30]	AW18

continued...

Signal Name	FPGA Pin Number
DDR4_CH2_DQ[31]	BA17
DDR4_CH2_DQ[32]	BB24
DDR4_CH2_DQ[33]	BA26
DDR4_CH2_DQ[34]	AV27
DDR4_CH2_DQ[35]	AY27
DDR4_CH2_DQ[36]	BA24
DDR4_CH2_DQ[37]	AY26
DDR4_CH2_DQ[38]	AV26
DDR4_CH2_DQ[39]	AW26
DDR4_CH2_DQ[4]	AK19
DDR4_CH2_DQ[40]	AW24
DDR4_CH2_DQ[41]	AT26
DDR4_CH2_DQ[42]	AT24
DDR4_CH2_DQ[43]	AU24
DDR4_CH2_DQ[44]	AY24
DDR4_CH2_DQ[45]	AU25
DDR4_CH2_DQ[46]	AT25
DDR4_CH2_DQ[47]	AR27
DDR4_CH2_DQ[48]	AT29
DDR4_CH2_DQ[49]	AR29
DDR4_CH2_DQ[5]	AM20
DDR4_CH2_DQ[50]	AP30
DDR4_CH2_DQ[51]	AN30
DDR4_CH2_DQ[52]	AP28
DDR4_CH2_DQ[53]	AR28
DDR4_CH2_DQ[54]	AT30
DDR4_CH2_DQ[55]	AT31
DDR4_CH2_DQ[56]	AM28
DDR4_CH2_DQ[57]	AL29
DDR4_CH2_DQ[58]	AN28
DDR4_CH2_DQ[59]	AP26
DDR4_CH2_DQ[6]	AN17
DDR4_CH2_DQ[60]	AL27
DDR4_CH2_DQ[61]	AM29

continued...

Signal Name	FPGA Pin Number
DDR4_CH2_DQ[62]	AN27
DDR4_CH2_DQ[63]	AM27
DDR4_CH2_DQ[64]	AN22
DDR4_CH2_DQ[65]	AN20
DDR4_CH2_DQ[66]	AM22
DDR4_CH2_DQ[67]	AR21
DDR4_CH2_DQ[68]	AM23
DDR4_CH2_DQ[69]	AP20
DDR4_CH2_DQ[7]	AM19
DDR4_CH2_DQ[70]	AN21
DDR4_CH2_DQ[71]	AP21
DDR4_CH2_DQ[8]	AL22
DDR4_CH2_DQ[9]	AJ23
DDR4_CH2_ODT	BB23
DDR4_CH2_PAR	AW23
DDR4_CH2_RESETN	AY22
DDR4_CH2_X4_DQS11N	AW25
DDR4_CH2_X4_DQS11P_DBI10N	AV25
DDR4_CH2_X4_DQS13N	AM30
DDR4_CH2_X4_DQS13P_DBI12N	AL30
DDR4_CH2_X4_DQS15N	AK30
DDR4_CH2_X4_DQS15P_DBI14N	AK29
DDR4_CH2_X4_DQS17N	AT20
DDR4_CH2_X4_DQS17P_DBI16N	AT21
DDR4_CH2_X4_DQS1N	AK18
DDR4_CH2_X4_DQS1P_DBI0N	AJ19
DDR4_CH2_X4_DQS3N	AK24
DDR4_CH2_X4_DQS3P_DBI2N	AJ24
DDR4_CH2_X4_DQS5N	AR17
DDR4_CH2_X4_DQS5P_DBI4N	AR18
DDR4_CH2_X4_DQS7N	AV17
DDR4_CH2_X4_DQS7P_DBI6N	AV16
DDR4_CH2_X4_DQS9N	BB27
DDR4_CH2_X4_DQS9P_DBI8N	BA27

continued...

Signal Name	FPGA Pin Number
DDR4_CH2_X8_DQS0N	AJ18
DDR4_CH2_X8_DQS0P	AH18
DDR4_CH2_X8_DQS10N	AU27
DDR4_CH2_X8_DQS10P	AT27
DDR4_CH2_X8_DQS12N	AR30
DDR4_CH2_X8_DQS12P	AP29
DDR4_CH2_X8_DQS14N	AK27
DDR4_CH2_X8_DQS14P	AK28
DDR4_CH2_X8_DQS16N	AU20
DDR4_CH2_X8_DQS16P	AU19
DDR4_CH2_X8_DQS2N	AK21
DDR4_CH2_X8_DQS2P	AK22
DDR4_CH2_X8_DQS4N	AN18
DDR4_CH2_X8_DQS4P	AM18
DDR4_CH2_X8_DQS6N	BB17
DDR4_CH2_X8_DQS6P	BB18
DDR4_CH2_X8_DQS8N	BA25
DDR4_CH2_X8_DQS8P	BB25
LVDS_DDR4_CH2_CLK_N	AW19
LVDS_DDR4_CH2_CLK_P	AY19

Table 17. DIMM 3 Interface to FPGA Pin Assignments

Signal Name	FPGA Pin Number
DDR4_CH3_1V8_EVENT_N	AE12
DDR4_CH3_A0	M28
DDR4_CH3_A1	N28
DDR4_CH3_A10	L27
DDR4_CH3_A11	M27
DDR4_CH3_A12	J29
DDR4_CH3_A13	J28
DDR4_CH3_A14	K28
DDR4_CH3_A15	H31
DDR4_CH3_A16	H30
DDR4_CH3_A17	H28
DDR4_CH3_A2	R26

continued...

Signal Name	FPGA Pin Number
DDR4_CH3_A3	P26
DDR4_CH3_A4	P28
DDR4_CH3_A5	R27
DDR4_CH3_A6	K26
DDR4_CH3_A7	K27
DDR4_CH3_A8	N26
DDR4_CH3_A9	N27
DDR4_CH3_ACTN	L29
DDR4_CH3_ALERTN	P30
DDR4_CH3_BA0	H27
DDR4_CH3_BA1	G27
DDR4_CH3_BG0	F27
DDR4_CH3_BG1	N30
DDR4_CH3_CKE	M30
DDR4_CH3_CKN	L30
DDR4_CH3_CKP	K31
DDR4_CH3_CSN	M29
DDR4_CH3_DQ[0]	N23
DDR4_CH3_DQ[1]	P23
DDR4_CH3_DQ[10]	J24
DDR4_CH3_DQ[11]	J25
DDR4_CH3_DQ[12]	G24
DDR4_CH3_DQ[13]	H25
DDR4_CH3_DQ[14]	L24
DDR4_CH3_DQ[15]	K24
DDR4_CH3_DQ[16]	E26
DDR4_CH3_DQ[17]	D26
DDR4_CH3_DQ[18]	D25
DDR4_CH3_DQ[19]	C25
DDR4_CH3_DQ[2]	M22
DDR4_CH3_DQ[20]	F26
DDR4_CH3_DQ[21]	F25
DDR4_CH3_DQ[22]	A24
DDR4_CH3_DQ[23]	A25

continued...

Signal Name	FPGA Pin Number
DDR4_CH3_DQ[24]	B23
DDR4_CH3_DQ[25]	G23
DDR4_CH3_DQ[26]	E23
DDR4_CH3_DQ[27]	B22
DDR4_CH3_DQ[28]	D23
DDR4_CH3_DQ[29]	F24
DDR4_CH3_DQ[3]	M23
DDR4_CH3_DQ[30]	A21
DDR4_CH3_DQ[31]	A22
DDR4_CH3_DQ[32]	D11
DDR4_CH3_DQ[33]	D9
DDR4_CH3_DQ[34]	F12
DDR4_CH3_DQ[35]	G12
DDR4_CH3_DQ[36]	E12
DDR4_CH3_DQ[37]	D10
DDR4_CH3_DQ[38]	E11
DDR4_CH3_DQ[39]	F11
DDR4_CH3_DQ[4]	P24
DDR4_CH3_DQ[40]	H16
DDR4_CH3_DQ[41]	L17
DDR4_CH3_DQ[42]	F17
DDR4_CH3_DQ[43]	F16
DDR4_CH3_DQ[44]	H17
DDR4_CH3_DQ[45]	K17
DDR4_CH3_DQ[46]	E16
DDR4_CH3_DQ[47]	G17
DDR4_CH3_DQ[48]	K16
DDR4_CH3_DQ[49]	L15
DDR4_CH3_DQ[5]	N22
DDR4_CH3_DQ[50]	P16
DDR4_CH3_DQ[51]	N16
DDR4_CH3_DQ[52]	J16
DDR4_CH3_DQ[53]	L16
DDR4_CH3_DQ[54]	P15

continued...

Signal Name	FPGA Pin Number
DDR4_CH3_DQ[55]	R16
DDR4_CH3_DQ[56]	H15
DDR4_CH3_DQ[57]	F15
DDR4_CH3_DQ[58]	G13
DDR4_CH3_DQ[59]	G14
DDR4_CH3_DQ[6]	L22
DDR4_CH3_DQ[60]	J15
DDR4_CH3_DQ[61]	G15
DDR4_CH3_DQ[62]	E13
DDR4_CH3_DQ[63]	D13
DDR4_CH3_DQ[64]	C21
DDR4_CH3_DQ[65]	D21
DDR4_CH3_DQ[66]	J21
DDR4_CH3_DQ[67]	H21
DDR4_CH3_DQ[68]	F22
DDR4_CH3_DQ[69]	E22
DDR4_CH3_DQ[7]	M24
DDR4_CH3_DQ[70]	H22
DDR4_CH3_DQ[71]	G22
DDR4_CH3_DQ[8]	G25
DDR4_CH3_DQ[9]	H26
DDR4_CH3_ODT	K30
DDR4_CH3_PAR	P29
DDR4_CH3_RESETN	P31
DDR4_CH3_X4_DQS11N	N18
DDR4_CH3_X4_DQS11P_DBI10N	M18
DDR4_CH3_X4_DQS13N	N15
DDR4_CH3_X4_DQS13P_DBI12N	M15
DDR4_CH3_X4_DQS15N	D14
DDR4_CH3_X4_DQS15P_DBI14N	D15
DDR4_CH3_X4_DQS17N	F21
DDR4_CH3_X4_DQS17P_DBI16N	E21
DDR4_CH3_X4_DQS1N	K22
DDR4_CH3_X4_DQS1P_DBI0N	K23

continued...

Signal Name	FPGA Pin Number
DDR4_CH3_X4_DQS3N	M25
DDR4_CH3_X4_DQS3P_DBI2N	L25
DDR4_CH3_X4_DQS5N	C26
DDR4_CH3_X4_DQS5P_DBI4N	C27
DDR4_CH3_X4_DQS7N	E24
DDR4_CH3_X4_DQS7P_DBI6N	D24
DDR4_CH3_X4_DQS9N	C11
DDR4_CH3_X4_DQS9P_DBI8N	C10
DDR4_CH3_X8_DQS0N	R24
DDR4_CH3_X8_DQS0P	T23
DDR4_CH3_X8_DQS10N	M17
DDR4_CH3_X8_DQS10P	N17
DDR4_CH3_X8_DQS12N	P18
DDR4_CH3_X8_DQS12P	R17
DDR4_CH3_X8_DQS14N	F14
DDR4_CH3_X8_DQS14P	E14
DDR4_CH3_X8_DQS16N	H23
DDR4_CH3_X8_DQS16P	J23
DDR4_CH3_X8_DQS2N	P25
DDR4_CH3_X8_DQS2P	N25
DDR4_CH3_X8_DQS4N	B25
DDR4_CH3_X8_DQS4P	B24
DDR4_CH3_X8_DQS6N	C22
DDR4_CH3_X8_DQS6P	C23
DDR4_CH3_X8_DQS8N	C8
DDR4_CH3_X8_DQS8P	D8
LVDS_DDR4_CH3_CLK_N	E27
LVDS_DDR4_CH3_CLK_P	D27

A.4. Network Interface

The Intel FPGA Programmable Acceleration Card D5005 has two network interfaces implemented as 2 QSFP28 cages on the I/O panel. Each interface supports dual 100 GbE (4 x 25 Gbps), 40 GbE (4 x 10 Gbps), and 10 Gbps interfaces. The Intel FPGA PAC supports Short Reach (SR) QSFP28 class 1-7 (up to 5 W) optical transceivers and Direct Attached Copper (DAC) cables up to 3 m in length.

A list of validated optical modules is shown below. This list is updated as more manufacturers modules are validated by Intel.

Table 18. Validated Optical Modules

Validated Optical Modules	100G QSFP28	40G QSFP28
Manufacturer	Intel	Intel
Manufacturer Part Number	SPTSBP2CLCKS	QSFP-40G-SR4

Table 19. Network Port 0 and Port 1 Interface to FPGA Pin Assignments

Signal Name	FPGA Pin Number	Description
FPGA_ZQSFP0_TX3_P	AC40	FPGA to Port 0 Transmit 3P. Bank 1F
FPGA_ZQSFP0_TX3_N	AC39	FPGA to Port 0 Transmit 3N. Bank 1F
FPGA_ZQSFP0_TX2_P	AF42	FPGA to Port 0 Transmit 2P. Bank 1F
FPGA_ZQSFP0_TX2_N	AF41	FPGA to Port 0 Transmit 2N. Bank 1F
FPGA_ZQSFP0_TX1_P	AD42	FPGA to Port 0 Transmit 1P. Bank 1F
FPGA_ZQSFP0_TX1_N	AD41	FPGA to Port 0 Transmit 1N. Bank 1F
FPGA_ZQSFP0_TX0_P	AG40	FPGA to Port 0 Transmit 0P. Bank 1F
FPGA_ZQSFP0_TX0_N	AG39	FPGA to Port 0 Transmit 0N. Bank 1F
ZQSFP0_FPGA_RX3_P	AC36	Port 0 to FPGA Receive 3P. Bank 1F
ZQSFP0_FPGA_RX3_N	AC35	Port 0 to FPGA Receive 3N. Bank 1F
ZQSFP0_FPGA_RX2_P	AD38	Port 0 to FPGA Receive 2P. Bank 1F
ZQSFP0_FPGA_RX2_N	AD37	Port 0 to FPGA Receive 2N. Bank 1F
ZQSFP0_FPGA_RX1_P	AB38	Port 0 to FPGA Receive 1P. Bank 1F
ZQSFP0_FPGA_RX1_N	AB37	Port 0 to FPGA Receive 1N. Bank 1F
ZQSFP0_FPGA_RX0_P	AG36	Port 0 to FPGA Receive 0P. Bank 1F
ZQSFP0_FPGA_RX0_N	AG35	Port 0 to FPGA Receive 0N. Bank 1F
FPGA_ZQSFP1_TX3_P	A36	FPGA to Port 1 Transmit 3P. Bank 1N
FPGA_ZQSFP1_TX3_N	A35	FPGA to Port 1 Transmit 3N. Bank 1N
FPGA_ZQSFP1_TX2_P	C40	FPGA to Port 1 Transmit 2P. Bank 1N
FPGA_ZQSFP1_TX2_N	C39	FPGA to Port 1 Transmit 2N. Bank 1N
FPGA_ZQSFP1_TX1_P	B38	FPGA to Port 1 Transmit 1P. Bank 1N
FPGA_ZQSFP1_TX1_N	B37	FPGA to Port 1 Transmit 1N. Bank 1N
FPGA_ZQSFP1_TX0_P	F38	FPGA to Port 1 Transmit 0P. Bank 1N
FPGA_ZQSFP1_TX0_N	F37	FPGA to Port 1 Transmit 0N. Bank 1N
ZQSFP1_FPGA_RX3_P	D30	Port 1 to FPGA Receive 3P. Bank 1N
ZQSFP1_FPGA_RX3_N	D29	Port 1 to FPGA Receive 3N. Bank 1N
ZQSFP1_FPGA_RX2_P	B30	Port 1 to FPGA Receive 2P. Bank 1N

continued...

Signal Name	FPGA Pin Number	Description
ZQSFP1_FPGA_RX2_N	B29	Port 1 to FPGA Receive 2N. Bank 1N
ZQSFP1_FPGA_RX1_P	A28	Port 1 to FPGA Receive 1P. Bank 1N
ZQSFP1_FPGA_RX1_N	A27	Port 1 to FPGA Receive 1N. Bank 1N
ZQSFP1_FPGA_RX0_P	C32	Port 1 to FPGA Receive 0P. Bank 1N
ZQSFP1_FPGA_RX0_N	C31	Port 1 to FPGA Receive 0N. Bank 1F

A.5. Clock Control

Two I^2C programmable clock sources are provided to the FPGA for driving the DDR4 DIMM interface and FPGA core logic. Each clock source has four outputs that are programmed to default frequencies at power-on. The default frequencies can be changed as needed. The table below defines each clock source.

Table 20. DDR4 Clock Source (I^2C Bus 2, Slave Address 0xD0)

Output Number	Output Name	Default Frequency	FPGA Pin Number	Description
1	LVDS_DDR4_CH0_CLK_P	150MHz	AL5	FPGA Bank 3B. IDT 5P49V5901 device.
	LVDS_DDR4_CH0_CLK_N		AL6	
2	LVDS_DDR4_CH1_CLK_P	150MHz	K8	FPGA Bank 3K. IDT 5P49V5901 device.
	LVDS_DDR4_CH1_CLK_N		K7	
3	LVDS_DDR4_CH2_CLK_P	150MHz	AY19	FPGA Bank 2B. IDT 5P49V5901 device.
	LVDS_DDR4_CH2_CLK_N		AW19	
4	LVDS_DDR4_CH3_CLK_P	150MHz	D27	FPGA Bank 2M. IDT 5P49V5901 device.
	LVDS_DDR4_CH3_CLK_N		E27	

Table 21. FPGA Clock Source (I^2C Bus 2, Slave Address 0xD4)

Output Number	Output Name	Default Frequency	FPGA Pin Number	Description
1	LVDS_FPGA_CLK3D_0P	83.25MHz	AE6	FPGA Bank 3D. IDT 5P49V5901 device.
	LVDS_FPGA_CLK3D_0N		AD6	
2	LVDS_FPGA_CLK3D_1P	100MHz	AD8	FPGA Bank 3D. IDT 5P49V5901 device.
	LVDS_FPGA_CLK3D_1N		AD9	
3	LVDS_FPGA_CLK3I_0P	125MHz	AA4	FPGA Bank 3I. IDT 5P49V5901 device.
	LVDS_FPGA_CLK3I_0N		Y4	
4	LVDS_FPGA_CLK3I_1P	133MHz	W5	FPGA Bank 3I. IDT 5P49V5901 device.
	LVDS_FPGA_CLK3I_1N		V5	

Each QSFP Network port also have dedicated clock drivers that are not programmable. Their frequency is fixed at 644.53125MHz as shown in the table below.

Table 22. Network Port 0 Clock Source (Fixed Frequency)

Output Name	Default Frequency	FPGA Pin Number	Description
QSFP0_644.53125MHZ_P	644.53125MHz	AD34	LVDS, FPGA BANK 1F.
QSFP0_644.53125MHZ_N		AD33	

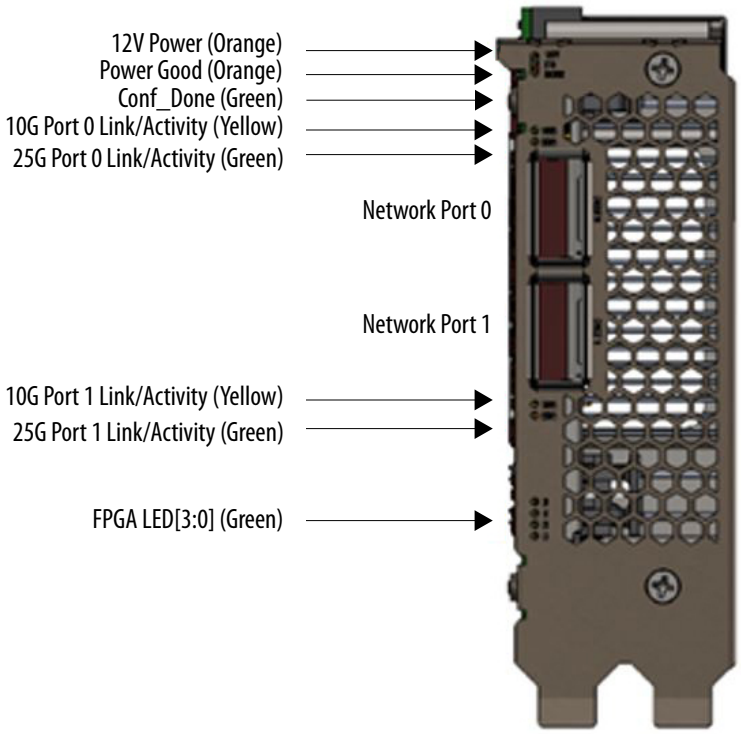
Table 23. Network Port 1 Clock Source (Fixed Frequency)

Output Name	Default Frequency	FPGA Pin Number	Description
QSFP1_644.53125MHZ_P	644.53125MHz	H34	LVDS, FPGA BANK 1N.
QSFP1_644.53125MHZ_N		H33	

A.6. Status LEDs

Various status LEDs are provided at the front panel to indicate the Intel FPGA PAC operating condition. The I/O panel status LED indicators are defined below.

Figure 8. Status LEDs



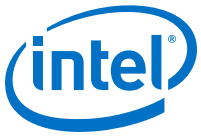


Table 24. I/O Panel Definition

LED Name	Description
12V	Orange LED. On when 12V power source is present. Off if 12V power source is not present.
PG	Orange LED. On when board power is present. Off if board power is not present.
DONE	Green LED. On indicates that the FPGA FIM is successfully loaded. This LED does not change states when AFUs are loaded.
Port 0 10G	Yellow LED. On when port 0 channels are linked at either 10 GbE or 40 GbE. Off when link is down. Blinking when there is either 10 GbE or 40 GbE network activity on the port.
Port 0 25G	Green LED. On when port 0 channels are linked at either 25 GbE or 1000 GbE. Off when link is down. Blinking when there is either 25 GbE or 100 GbE network activity on the port.
Port 1 10G	Yellow LED. On when port 1 channels are linked at either 10 GbE or 40 GbE. Off when link is down. Blinking when there is either 10 GbE or 40 GbE network activity on the port.
Port 1 25G	Green LED. On when port 1 channels are linked at either 25 GbE or 1000 GbE. Off when link is down. Blinking when there is either 25 GbE or 100 GbE network activity on the port.
FPGA LED 3	Green LED. Connected to FPGA for workload usage. State of LED is defined by the configured workload.
FPGA LED 2	Green LED. Connected to FPGA for workload usage. State of LED is defined by the configured workload.
FPGA LED 1	Green LED. Connected to FPGA for workload usage. State of LED is defined by the configured workload.
FPGA LED 0	Green LED. Connected to FPGA for workload usage. State of LED is defined by the configured workload.

B. Safety and Regulatory Information

B.1. Regulatory Compliance

Regulatory Model Number: BD-ACD-D5005

United States Federal Communications Commission (FCC) Class A User Information

The Class A Product: Intel FPGA Programmable Acceleration Card D5005 complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept the interference received, including interference that may cause undesired operation.

Attention: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with other instrcutions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference is at his/her own expense.

Caution: If this device is changed or modified without permission from Intel, the user may void his or her authority to operate the equipment.

VCCI Class A Statement

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Canada EMC Compliance Statement

This Class A digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.

European Community Manufacturer Declaration

CE

Belgium (French)

Par la présente, Intel Corporation déclare que la carte Intel FPGA Programmable Acceleration Card D5005 est conforme aux directives 2014/30/UE, 2014/35/UE et 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Le texte intégral en anglais de la déclaration européenne de conformité est disponible à l'adresse suivante : https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Denmark

Intel Corporation erklærer hermed, at Intel FPGA Programmable Acceleration Card D5005 overholder direktiverne 2014/30/EU, 2014/35/EU og 2011/65/EU.

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Den fulde tekst for EUs overensstemmelseserklæring findes på engelsk på følgende adresse: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

The Netherlands

Intel Corporation verklaart hierbij dat Intel FPGA Programmable Acceleration Card D5005 in overeenstemming is met de richtlijnen 2014/30/EU, 2014/35/EU en 2011/65/EU.

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De volledige Engelse tekst van de EU-conformiteitsverklaring is hier beschikbaar: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Germany

Hiermit erklärt die Intel Corporation, dass die Intel FPGA Programmable Acceleration Card D5005 den Richtlinien 2014/30/EU, 2014/35/EU und 2011/65/EU entspricht.

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Die vollständige EU-Konformitätserklärung ist in englischer Sprache unter der folgenden URL einsehbar: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Sweden

Härmed intygar Intel Corporation att Intel FPGA Programmable Acceleration Card D5005 överensstämmer med direktiven 2014/30/EU, 2014/35/EU och 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Den fullständiga engelska texten för EU-överensstämmelsen finns på följande internetadress: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Finland

Intel Corporation vakuuttaa täten, että Intel FPGA Programmable Acceleration Card D5005 on direktiivien 2014/30/EU, 2014/35/EU ja 2011/65/EU määräysten mukainen.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

EU-vaatimustenmukaisuusvakuutuksen koko englanninkielinen teksti on saatavilla osoitteessa: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Ireland

Hereby, Intel Corporation declares that the Intel FPGA Programmable Acceleration Card D5005 is in compliance with Directives 2014/30/EU, 2014/35/EU and 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

The full text of the EU declaration of conformity is available at the following URL: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Portugal

A Intel Corporation declara, por este meio, que a Intel FPGA Programmable Acceleration Card D5005 cumpre as Diretivas 2014/30/UE, 2014/35/UE e 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Pode consultar o texto da declaração de conformidade da UE na íntegra, disponível em inglês através do seguinte URL: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Spain

Por la presente, Intel Corporation declara que Intel FPGA Programmable Acceleration Card D5005 cumple las directivas 2014/30/UE, 2014/35/UE y 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

El texto completo (en inglés) de la declaración de conformidad de la UE está disponible en la siguiente URL: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

France

Par la présente, Intel Corporation déclare que la carte Intel FPGA Programmable Acceleration Card D5005 est conforme aux directives 2014/30/UE, 2014/35/UE et 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Le texte intégral en anglais de la déclaration européenne de conformité est disponible à l'adresse suivante : https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Italy

Con il presente documento, Intel Corporation dichiara che la scheda di accelerazione programmabile Intel FPGA Programmable Acceleration Card D5005 è conforme alle direttive 2014/30/EU, 2014/35/EU e 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Il testo completo della dichiarazione di conformità UE in lingua inglese è disponibile al seguente indirizzo: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

United Kingdom

Hereby, Intel Corporation declares that the Intel FPGA Programmable Acceleration Card D5005 is in compliance with Directives 2014/30/EU, 2014/35/EU and 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

The full text of the EU declaration of conformity is available at the following URL: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Poland

Firma Intel Corporation niniejszym oświadcza, że karta Intel FPGA Programmable Acceleration Card D5005 jest zgodna z dyrektywami 2014/30/UE, 2014/35/UE i 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Pełny tekst deklaracji zgodności z wymogami UE w języku angielskim jest dostępny na stronie: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

End-of-Life/ Product Recycling

Product recycling and end-of-life take-back systems and requirements vary by country.

Contact the retailer or distributor of this product for information about product recycling and/or take-back.

Regulatory Markings

D33025
RoHS

R-R-CPU-BD-ACD-D5005

CAN ICES-3 (A)/NMB-3(A)

C. Revision History

Table 25. Revision History of the Intel FPGA Programmable Acceleration Card D5005 Data Sheet

Document Version	Changes
2019.09.12	Updated: • Power on page 5 • Power Requirements on page 16 • Mechanical Information on page 17 • Status LEDs on page 46
2019.05.13	Initial Release